PM5344

GENERATING LOP DURING OUT OF RANGE POINTER CONDITIONS

APPLICATION NOTE

ISSUE 2: SEPTEMBER 1997

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1 OVERVIEW

This application note addresses the "LOP Not Declared" errata listed in the SPTX data sheet. This error condition can lock up the SPTXs' internal pointer interpreter state machine into a dormant state where the SPTX does not declare the LOP condition. This application note describes PMC-Sierra's recommended circuit that will guarantee LOP detection when the upstream NE asserts an out of range pointer that does not imitate a pointer justification for greater than seven continuous frames.

2 POINTER MANIPULATOR

Under certain conditions the SPTXs' pointer interpreter state machine can lock up into a state where it is no longer able to declare the LOP alarm. This condition is caused by asserting a static out of range pointer into the SPTX's RECEIVE BUS that happens to look like an increment or a decrement compared to the previous good pointer processed by the SPTX. When this condition occurs for two consecutive frames, the SPTX will enter a dormant state from which it cannot exit unless the incoming pointer changes to a value other than the one it received during lockup.

As an example of the lockup behaviour, assume the SPTX is processing normally while receiving a pointer of 602 decimal, or binary 1001011010. Next, let us assume that the SPTX receives a pointer of 783 decimal, or binary 1100001111. This represents an invalid pointer that happens to look like a decrement (majority of the 'D' bits are inverted) and the SPTX will internally process it as if it was a real decrement event. During the next frame the SPTX continues to receive a pointer of 783 decimal value. Again, it looks like a decrement event compared to a pointer of 601 decimal. If the incoming pointer remains locked at 783 decimal, the SPTX will lock up after the second decrement event and will not exit until the pointer changes its value.

The "Out of Range Pointer Manipulation Logic" shown in figure 1 detects an out of range pointer value that occurs over a multiple number of consecutive frames. After the second consecutive occurrence of an out of range pointer, this circuitry modifies the second pointer on the data stream (prior to connection to the SPTX) to assume one of two possible values, PTR1 or PTR2. The value of PTR1 is binary xxxxxx1110xxxxxx and the value of PTR2 is binary xxxxxx1101xxxxxx, where "x" represents whatever value was in the original pointer. In a string of out of range pointer values the pointers PTR1 and PTR2 will be substituted in alternate sequence in place of the received out of range pointer value. As an example, if the received pointer value contains the sequence 783, 783, 783, 783, 783, 320, 783, 783, 783 then the modified data will be 783, PTR1, PTR2, PTR1, PTR2, 320, 783, PTR1, PTR2.

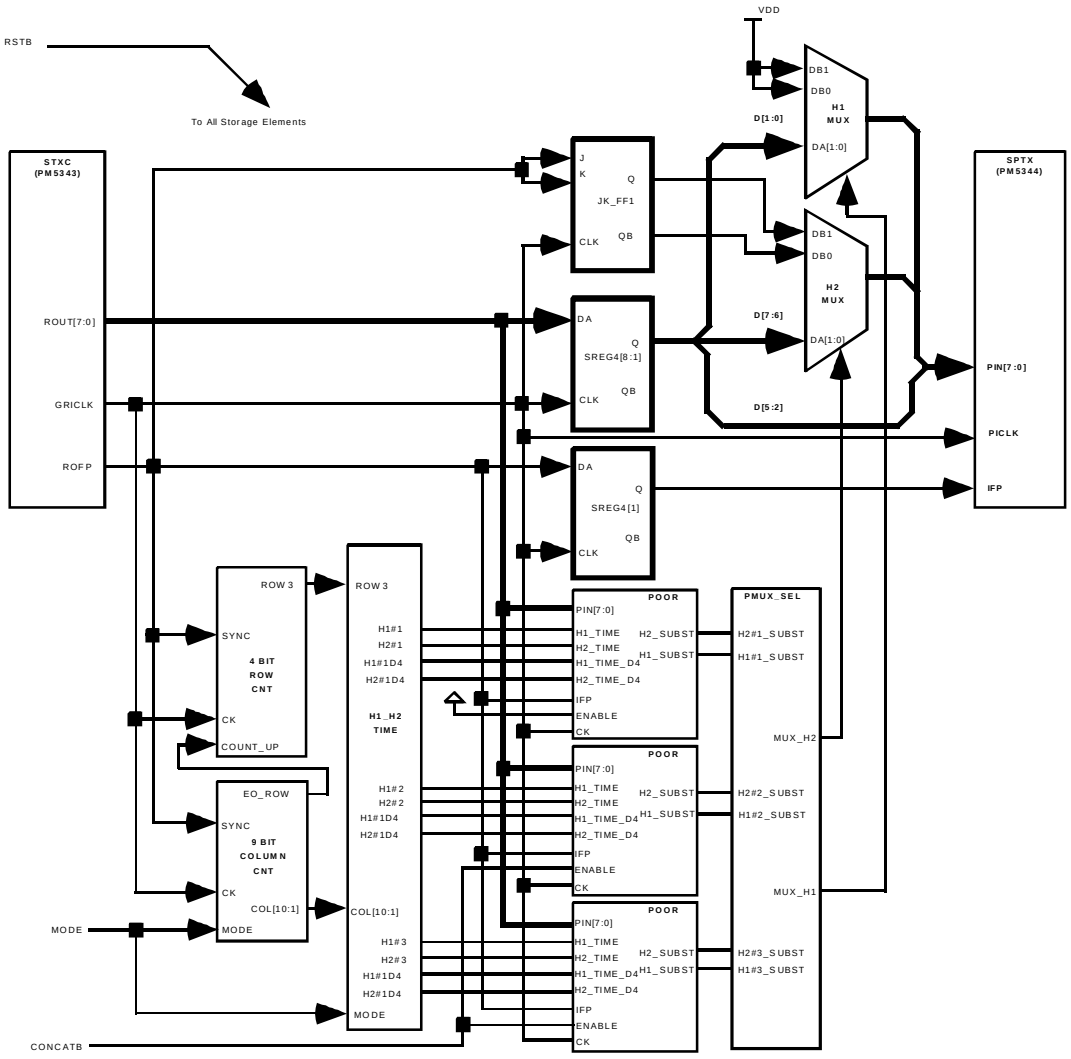
The out of range pointer value is generated by the JK_FF1 and the multiplexer logic H1 MUX and H2 MUX. The multiplexer select control is controlled by the "ROW CNT", "COLUMN CNT", "H1_H2 TIME", "POOR" and "PMUX_SEL" blocks.

The SREG4[8:1] block is a 4 stage shift register for an 8 bit wide bus. This shift register takes into account the delay required to decode the multiplexer selection

control. Similarly, the SREG4[1] block is a 4 stage shift register required to delay the frame pulse for alignment with the 4 bit shift register of the data bus.

Each of the main blocks comprised in this circuitry is described in detail below.

Figure 1 - Out Of Range Pointer Manipulation Logic



2.1 STXC PM5343

The STXC block represents a device that generates the out of range pointer values on its ROUT[7:0] outputs. The ROFP and GRICLK are the accompanying frame pulse and clock outputs.

2.2 4 Bit Row Counter

This counter is a 4 bit counter counting from 0 to 8 and represent the row number of a SONET/SDH frame. The counter is synchronized to zero by the SYNC input connection to the ROFP frame pulse of the STXC and after a count incrementing event from count 8. The ROW3 output indicates when the 4th row of the SONET/SDH frame is valid.

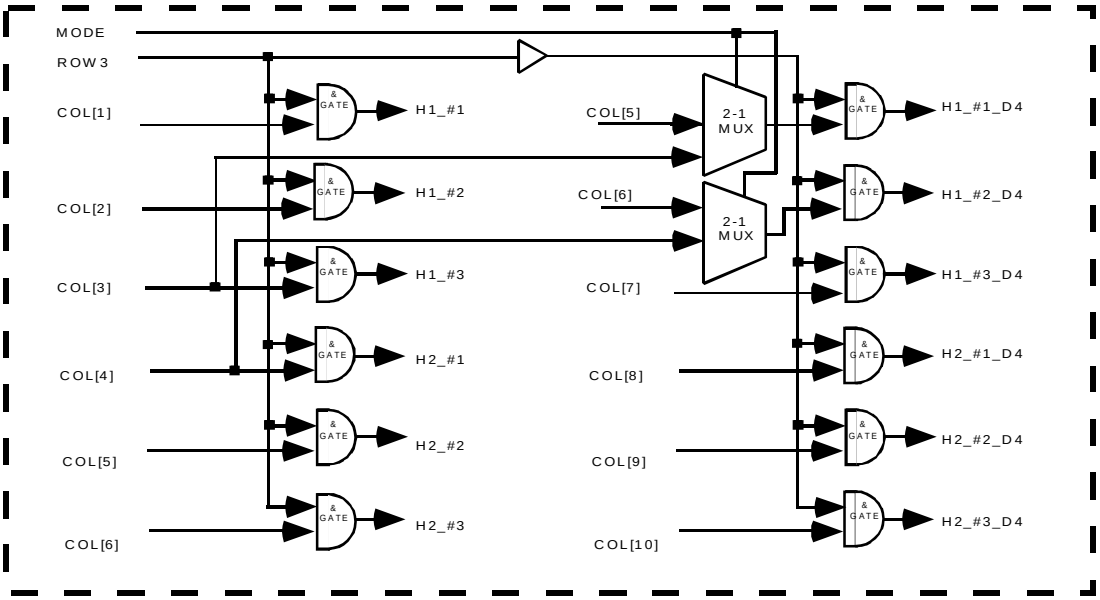
2.3 9 Bit Column Counter

This counter identifies the column within the SONET/SDH frame being output from the STXC block. For a STS-3/3c (STM-1) frame the column counter counts from 0 to 269 and for an STS-1 (STM-0) frame the column counter counts 0 to 89. The synchronization of this counter occurs during the SYNC input being logic 1. Since ROFP occurs during the 10th column of an STS-3/3c frame or during the 4th column of an STS-1 frame the counter synchronizes (on the rising edge) to a count of 10 or 4, depending upon the mode of operation. The MODE input controls the counting range of this counter. The outputs of this block (COL[10:0]) indicate the column identification, ranging from column 0 to column 10.

2.4 H1_H2 TIME

This block decodes the time at which the H1 and H2 bytes (and their delayed versions) become valid on the data bus. Fig. 2 shows the functionality of this block. When the MODE input is logic one, for STS-3/3c or STM-1 operation, the two multiplexers select COL[5] and COL[6] respectively.

Figure 2 - H1_H2 Time Decoder



The remaining logic is simply an AND decode of the column number with ROW3.

The output H1#1 represents the byte time of the H1 byte of the first interleaved STS-1 in the STS-3/3c SONET frame. The output H2#1 represents the byte time of the H2 byte of the first interleaved STS-1 in the STS-3/3c SONET frame. The output H1#2 represents the byte time of the H1 byte of the second interleaved STS-1 in the STS-3/3c SONET frame. The output H2#2 represents the byte time of the H2 byte of the second interleaved STS-1 in the STS-3/3c SONET frame. The output H1#3 represents the byte time of the H1 byte of the third interleaved STS-1 in the STS-3/3c SONET frame. The output H2#3 represents the byte time of the H2 byte of the third interleaved STS-1 in the STS-3/3c SONET frame.

The output H1#1D4 represents the 4 cycle delayed byte time of the H1 byte of the first interleaved STS-1 in the STS-3/3c SONET frame. The output H2#1D4 represents the 4 cycle delayed byte time of the H2 byte of the first interleaved STS-1 in the STS-3/3c SONET frame. The output H1#2D4 represents the 4 cycle delayed byte time of the H1 byte of the second interleaved STS-1 in the STS-3/3c SONET frame. The output H2#2D4 represents the 4 cycle delayed byte time of the H2 byte of the second interleaved STS-1 in the STS-3/3c SONET frame. The output H2#3D4 represents the 4 cycle delayed byte time of the H2 byte of the third interleaved STS-1 in the STS-3/3c SONET frame. The

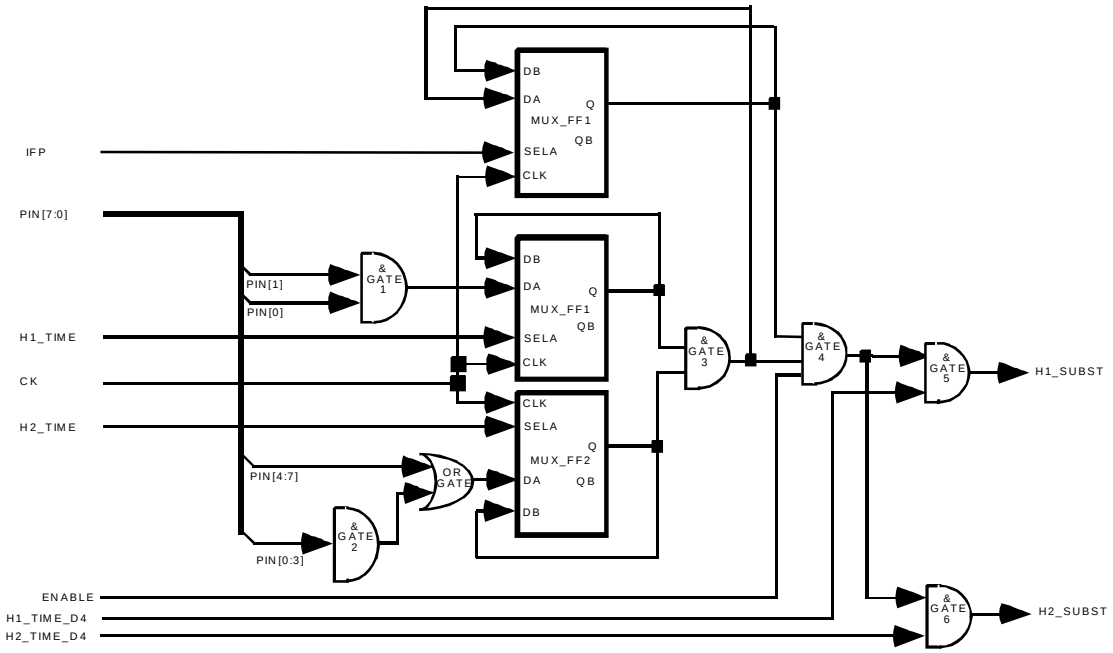
output H2#3D4 represents the 4 cycle delayed byte time of the H2 byte of the third interleaved STS-1 in the STS-3/3c SONET frame.

2.5 POOR (Pointer Out Of Range)

This block decodes the pointer out of range indication. Fig. 3 shows the logic of this block. The AND "GATE 1" detects that the H1 byte contains a value of binary xxxxxx11 in the data present on the data bus. The AND "GATE 2" and the OR gate detects that the H2 bytes contains a value of at least 15 (decimal) on the data bus. These decodes are stored by the "MUX_FF1" and "MUX_FF2" respectively. The update of "MUX_FF1" occurs during the H1 byte time and the update of "MUX_FF2" occurs during the H2 byte time. When both "MUX_FF1" and "MUX_FF2" contain a logic 1 the pointer received on the data bus was greater than 783 and this is detected by the output of AND gate "GATE3". The storage of this is captured by "MUX_FF3" when IFP is logic 1. Therefore, the output of "MUX_FF3" indicates whether the previous frame contained an out of range pointer.

The H1_SUBST output indicates (when logic 1) the substitution of the H1 byte by a binary xxxxxx11 value into the data stream, where "x" represents a value originally present on the data bus. The H2_SUBST output indicates (when logic 1) the substitutution of the H2 byte by a binary value of either 10xxxxxx or 01xxxxxx into the data stream.

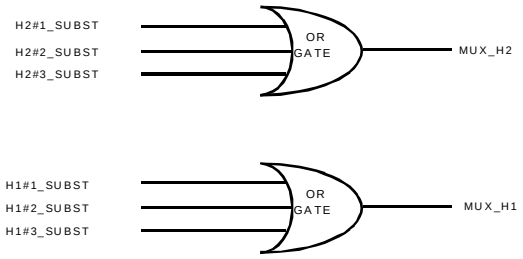
Figure 3 - POOR (Pointer Out Of Range) Decoder



2.6 PMUX_SEL

This block decodes which pointer bytes to substitute. When MUX_H1 is logic one, the H1 bytes are substituted, when MUX_H2 is logic 1 then the H2 bytes are substituted.

Figure 4 - Multiplexer Select Control



When the H1 byte is substituted, only the two LSB's of the data byte are substituted by the H1 MUX block at the top level. When the H2 byte is substituted, only the two MSB's of the byte are substituted by the H2 MUX block at the top level.

3 REFERENCES

1. PMC-Sierra data book PM5344 (SPTX), May, 1995.

NOTES

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