

**PM5946**



**S/UNI-LITE  
OPTICAL REFERENCE  
DESIGN  
(SORD)**

**Issue 2: September 25, 1995**

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**List of Changes**

The following changes have been made to the issue 1 of the document:

**Document Changes**

- Added the section "List of Changes" Page 1.
- Added the section titled "*How does layout affect high speed return current?*" Page 10.
- Modified the section titled "*What about reverse-biasing the capacitors during reset?*" Page 13.
- Added the section titled "*How to drive the RRCLK+/- & TRCLK+/- inputs using one oscillator?*" Page 14.
- Added the section titled "*How accurate should the on board reference clock be?*" Page 16.
- Modified the block diagram on page 17 to reflect the schematic changes.
- Updated the Appendix C "Material List".
- Updated S/UNI-LITE register address map
- Updated Reference to latest S/UNI-LITE datasheet

**Schematic Changes**

- Changed oscillator Y1 from CMOS to TTL
- Added U1 (74xxx541) and termination resistors to buffer Y1
- Added decoupling cap C17 for transistor Q1
- Added two SMA connectors on board for testing purposes
- Added additional layout notes on the schematics

**Layout Changes**

- Placed the added parts and routed the connections
- Rerouted the power trace to the transistor Q1
- Moved decoupling caps C24 & C9 closer to TXVDD pin of the S/UNI-LITE
- Moved "+" sign of C20 to the correct pad.
- Moved via under C35 elsewhere
- Move the decoupling cap C33 inward, away from the edge connector
- Moved the decoupling cap C40 to allow more space for the power trace

## **1. OVERVIEW**

The PM5946 SORD daughter board contains the PMC PM5346 S/UNI-LITE-155 (SATURN User Network Interface), and optical PMD in a complete optical ATM (Asynchronous Transfer Mode) physical interface. The S/UNI-LITE is an ATM physical layer processor for a SONET STS-3C transmission system. The SORD daughter board is configured, monitored, and powered through a 100 pin edge connector. The motherboard provides all of the software and decoding logic necessary to directly access all of the registers on the SORD board.

The SORD line side interface uses any 9-pin duplex SC receptacle. The optical Transceiver PMD device runs at 155.52 MHz. On the receive side, the receive optical PMD is ac-coupled to the S/UNI-LITE's bit serial input. On the transmit side, the S/UNI-LITE's CMOS data outputs are ac-coupled, attenuated, level shifted and then connect directly to the optical Transceiver PMD device.

The SORD drop side interface uses a 100 pin edge connector. The 22V10 PLD is used to handle the Generic Flow Control and Alarm conditions.

## **2. DESIGN CONSIDERATIONS**

### ***What are the main concerns of using PECL over ECL?***

As ECL uses the upper rail of the supply as the reference for the I/O and internal switching, a negative supply with the ground being the reference was a natural choice, as it is easier to keep the ground plane quiet than the power rail. Since ECL requires a negative power supply and most designers mixing TTL/CMOS with ECL only want a single supply, PECL (positive ECL) became a common choice. PECL operates the same as ECL but now has the noisier +5 Volt rail as the reference. PECL devices are differential; the noise on the inputs will be common mode noise and will not affect a differential input, but it will affect the internal reference, especially if the power supplying the transmitting device is not in common with the receiver. The S/UNI-LITE does not have true differential inputs. Therefore, the inputs are affected by common mode noise. They are CMOS inputs which accept PECL level swings.

### ***What PECL termination scheme is the best to use?***

"Termination" applies to terminating a signal propagating down a transmission line to the characteristic impedance of line. If the line is not terminated to it's characteristic impedance, there will be reflection back down the line. The amount of reflection at the load (receiver) is given by the load reflection coefficient:

$$\rho_L = (R_T - Z_0) / (R_T + Z_0)$$

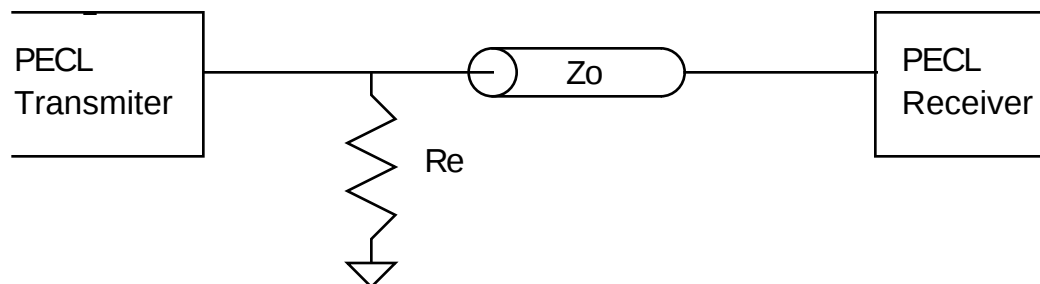
where  $R_T$  is the load impedance and  $Z_0$  is the characteristic impedance of the line. The amount of reflection at the source (transmitter) is given by the source reflection coefficient:

$$\rho_S = (R_S - Z_0) / (R_S + Z_0)$$

where  $R_S$  is the source impedance and  $Z_0$  is the characteristic impedance of the line. The reflected signal propagates back and forth until the "ringing" dies out.

There are 4 basic types of terminations used for PECL (or ECL). They are open line termination, series termination, parallel termination, and Thévenin parallel termination. Since PECL (or ECL) signals only drive high, external biasing is need to pull the PECL signal low. This biasing has to be incorporated into the termination scheme.

Unterminated lines (open line) should only be used for very short line lengths (less than 1/4 of an inch), or for low frequency signals. A unterminated line is shown below with resistor **Re** used to pull the PECL signal low:

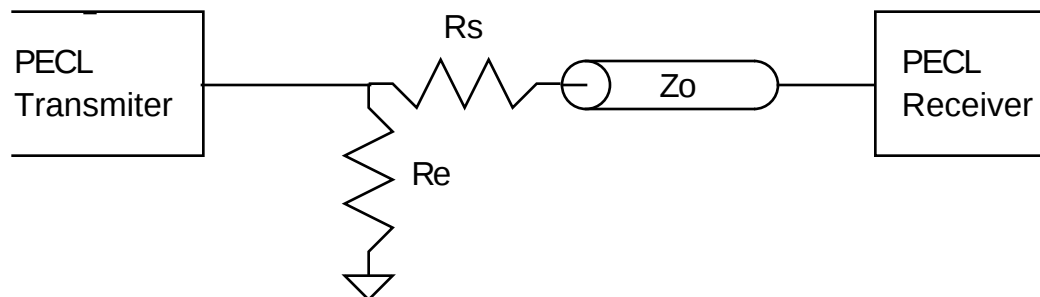


The maximum line length equation is given by:

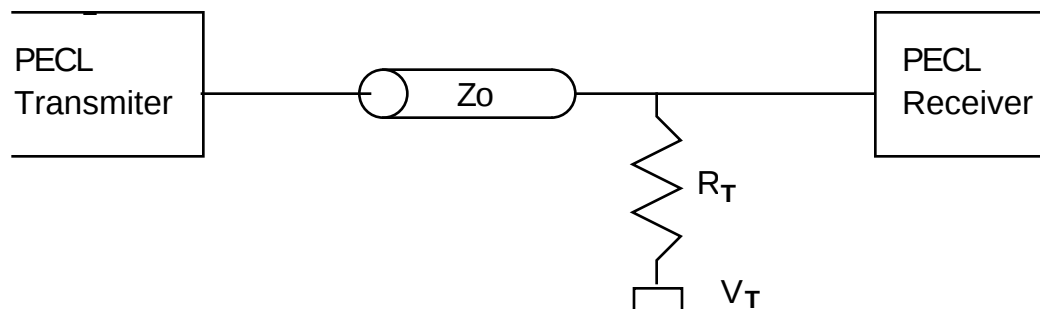
$$L_{\max} = 0.5 * (\sqrt{(C_D / C_O)^2 + (t_R / T_{PD})^2}) - C_D / C_O$$

where **L** = line length, **t<sub>R</sub>** = rise time, **T<sub>PD</sub>** = propagation delay per unit length, **C<sub>O</sub>** = capacitance per unit length, and **C<sub>D</sub>** = the distributed capacitance. The above equation assures that the undershoot will be limited to 15% of the full logic swing.

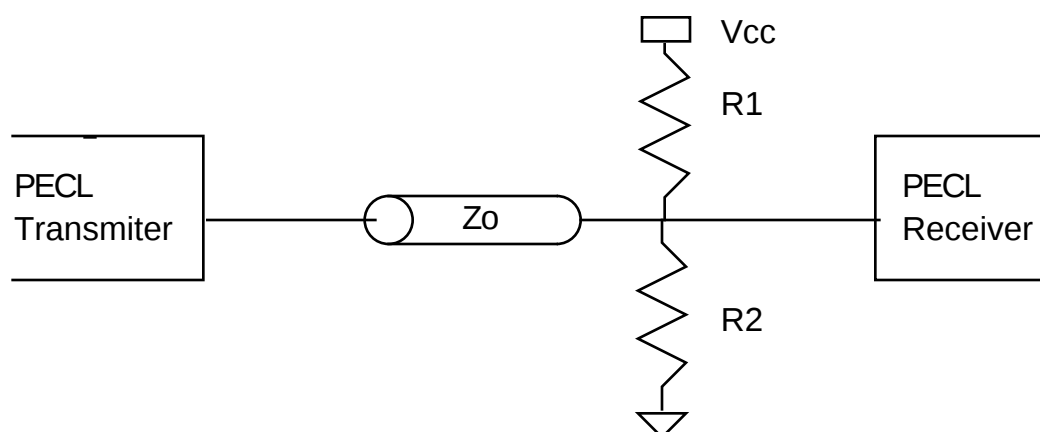
Series terminated lines can be used when the interconnect distances are long or there are discontinuities in the characteristic impedance lines. A series resistor at the output of the driver reduces the voltage swing of the logic signal in half. The 1/2 amplitude signal propagates down the transmission line. At the end of the characteristic impedance line, the voltage doubles since the reflection coefficient is unity due to the unterminated line. The half amplitude swing along the transmission line reduces crosstalk, but if the distance between the end of the transmission line and the receiver input is not kept short as in **L<sub>max</sub>** above, the reflection is added to the signal and propagates back to the transmitter. A series terminated line is shown below where **R<sub>s</sub>** is equal to the characteristic impedance of the line **Z<sub>o</sub>** minus the output impedance of the driving gate:



Parallel terminated lines offer the best terminations for speed and power consumption. The receiver end of the transmission line terminates and biases the signal. The terminating resistor is the same value as the characteristic impedance of the transmission line. Unfortunately this requires another voltage supply as the terminating voltage (**V<sub>T</sub>**) is **V<sub>CC</sub> - 2 Volts**. A parallel terminated line is shown below where **R<sub>T</sub>** equals **Z<sub>o</sub>**:



Thévenin terminated lines terminate the lines to the characteristic impedance and sets the terminating ( $V_T$ ) voltage. A Thévenin equivalent parallel termination is shown below:



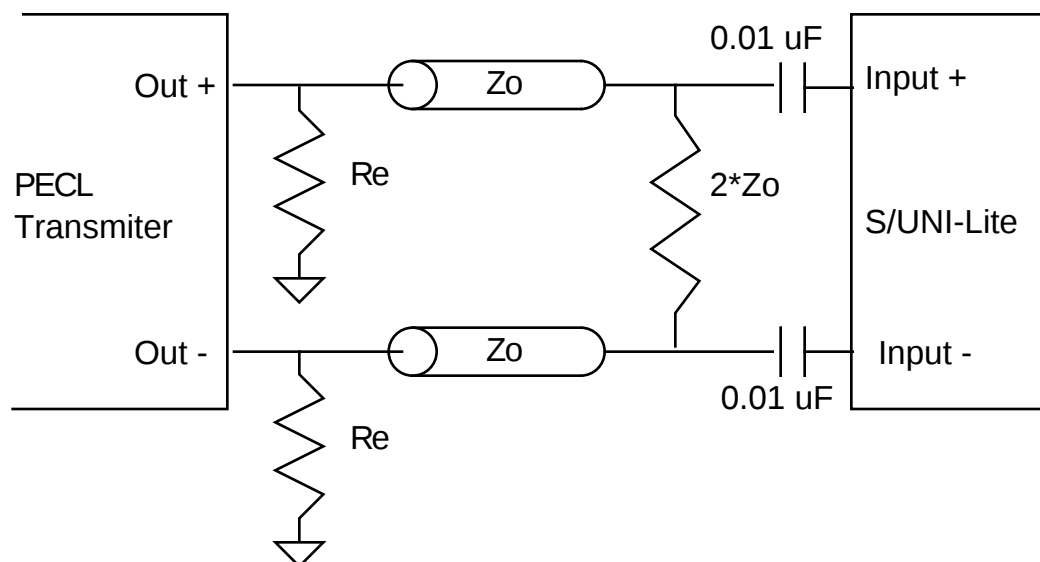
The resistors  $R_1$  and  $R_2$  in parallel must equal  $Z_o$  and the voltage at the input must pull the output of the transmitting gate to  $V_{cc} - 2$  Volts. Working out the equations for PECL +5 Volt supply for  $V_{cc}$  gives:

$$R_2 = 2.5 * Z_o$$

$$R_1 = R_2 * 2/3$$

Note that the above examples show only one of the differential inputs. With the Thévenin termination care must be taken so that the  $V_{cc}$  and grounds of the differential signals are taken in close proximity of each other or the noise on  $V_{cc}$  and ground will not be in common with each other. Also it is not necessary to use PECL (or ECL) transmitter and receivers to drive characteristic impedance lines.

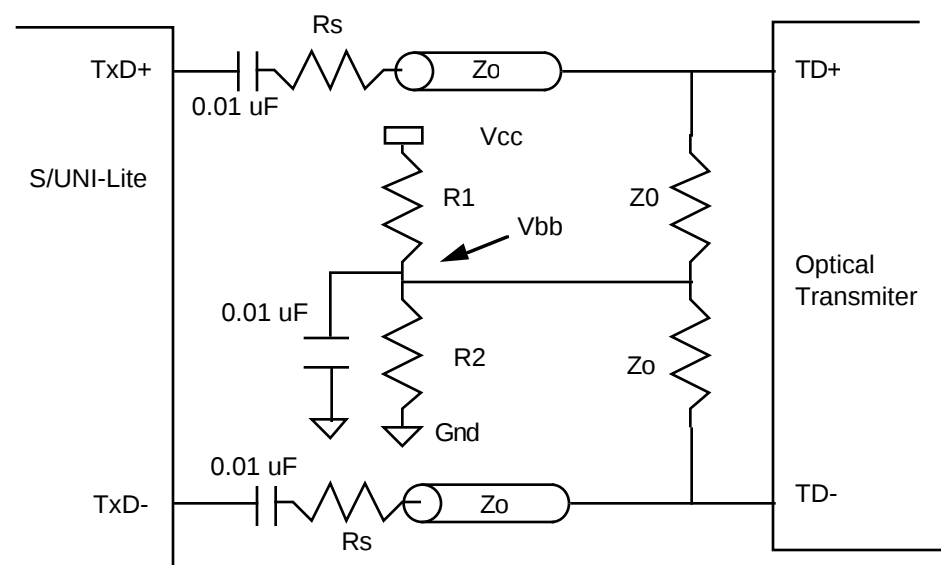
Since the S/UNI-LITE's PECL (pseudo ECL) inputs are internally self-biased, a hybrid of the parallel termination can be used which has minimum current draw and the terminating voltage ( $V_T$ ) is not required. By AC-coupling into the S/UNI-LITE, the S/UNI-LITE sets the internal switching threshold. A resistor  $2 * Z_o$  is placed between the differential outputs at the terminating end as shown below to terminate the line:



The **Re** resistors are used to pull the PECL outputs low.

### How to convert the S/UNI-LITE CMOS outputs to PECL levels?

The S/UNI-LITE high speed CMOS outputs have to be AC-coupled, attenuated, level shifted and terminated into a PECL optical transmitter input. This can be done with a CMOS to PECL converter like a Motorola MC10H352. A more cost effective way is shown below:



The TxD+/- outputs are AC-coupled and then the series resistor **R<sub>s</sub>** is used to attenuate the CMOS levels to PECL levels. The **V<sub>pp</sub>** input (voltage requirement of PECL input) swing is given by the equation below with **R<sub>out</sub>** (approximately 25

ohms) being the output impedance of the S/UNI-LITE drivers. For  $V_{pp} = 800$  mVolts of swing,  $R_s$  is approximately 240 ohms.

$$V_{pp} = (Z_o / ((R_s + R_{out}) + Z_o)) * V_{cc}$$

The  $V_{bb}$  voltage (3.7 volts for PECL) is generated by a voltage divider network which is set to the switching threshold of the optical transmitter:

$$V_{bb} = V_{cc} * R_2 / (R_2 + R_1)$$

### ***What can be done to minimize power supply transient voltages?***

High current draw during IC switching causes power supply transients  $\Delta I$  due to the inductance of the power lines. Large voltages appear on the power rails due to the transient current flowing through these power line inductances. The magnitude of the noise voltage can be reduced by minimizing the inductance of the power lines and by decreasing the magnitude of the transient currents. The power line inductance can be minimized by using a power plane. The transient currents on the power rails can be minimized by supplying the power from an alternate source such as a decoupling capacitor near the circuit that is drawing the current.

The decoupling capacitance and the inductance of the wiring between the capacitor and the power pin determine the noise voltage at the power pin. Bulk decoupling capacitors are used to supply the bulk DC current and the high frequency decoupling capacitors are used to supply all the transient current that is required when the circuit is switching.

### ***What values should the decoupling capacitor be?***

The bulk decoupling value should be 10 times the value of all the decoupling capacitance combined and should be located where the power comes in. Capacitors with low internal inductance should be used such as a tantalum electrolytic. Stay away from aluminum electrolytic as their inductances are an order of magnitude larger than the tantalum capacitor. A ferrite bead (or 1 to 10  $\mu H$  inductor) can be used before the bulk capacitor to keep the power supply transient noise from entering the circuit.

The power pin decoupling capacitor must be able to supply all the switching current. The minimum capacitance can be calculated by:

$$C = \Delta I * \Delta t / \Delta V$$

The transient voltage drop  $\Delta V$  in the supply voltage is caused by the transient current  $\Delta I$  occurring over time  $\Delta t$ . Using decoupling capacitors that are too large should be avoided. Since all capacitors have some inductance in series with the capacitance there will be a self-resonance at a certain frequency, at which point there is a low impedance path to ground. The self-resonant frequency is given by the equation:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Note that the larger the capacitance (for the same inductance) the lower the resonant frequency. If the capacitor is too large, the self-resonance will be too low to be an effective bypass but if the capacitor is not large enough, there will be insufficient current to supply the transient current during switching. The smallest value capacitor to satisfy the above equations should be used. It is rarely necessary that a capacitor larger than 0.01  $\mu\text{F}$  be used.

### ***Where should the decoupling capacitors be placed?***

The decoupling capacitor should be placed as close to the IC power pin as possible reduce the wiring inductance. There are 5 sources of inductance: the inductance of the capacitor, the inductance of the wiring between the capacitor and the IC power pin, the power pin lead inductance inside the IC, the ground pin lead inductance inside the IC, and the ground inductance between the IC pin and ground. The capacitor inductance is negligible if the correct capacitor is used. There is no control over the lead frame inductance. To keep the inductance low, both the power lead and the ground lead should be keep as short as possible (less than 1.5 inches). The inductance for a trace is given by:

$$L = 0.005 \ln(2\pi h/w) \mu\text{H/inch}$$

where  $\ln$  is the inverse log,  $h$  is the height between power or ground lead and the ground plane and  $w$  is the width of the power or ground lead. Note that doubling the width of the trace or reducing  $h$  will only decrease  $L$  approximately by 20 %, but decreasing the length by 50% will decrease the inductance by 50%. A typical board has about 15 nH of inductance per inch.

### ***What can be done to minimize ground noise?***

Return currents and power supply transients during high current consumption produce most of the ground noise. Since ground noise cannot be controlled by decoupling capacitors, the only way to minimizing the effect of ground noise is to minimize ground impedance. The best way to minimize ground impedance is to use a ground plane. It is not advisable to use ferrite beads in the ground path as this will inhibit the return currents from leaving and raise the ground noise level.

### ***What to do with unused (CMOS) inputs?***

All unused inputs should be connected to their inactive state to prevent unintentional switching which produces noise generation and power consumption. For the CMOS inputs the inactive low state can be connected to ground and the inactive high state can be connected to the power rail ( $V_{cc}$ ) through a series resistor (4.7k).

***Is it necessary to isolate the analog from the digital?***

The digital CMOS circuits have high immunity to external noise (approximately  $0.3 \times V_{cc}$ ) whereas a small amount of external noise coupled into the analog circuits can be devastating. The analog circuits operate on low voltage swings (600 mVolts for the S/UNI-LITE PECL inputs) as compared to the large (5 Volt) of the CMOS inputs. The CMOS circuits can also generate a lot of switching noise, especially when a large number of circuits are running synchronously all timed to the same system clock.

In the S/UNI-LITE, if the analog power and grounds are not isolated from each other it is unlikely that the S/UNI-LITE will be able to do clock and data recovery without any bit errors. Without isolation, it is also unlikely that the transmitter of the S/UNI-LITE will be able to meet the 0.01 U.I. rms. specified by Bellcore. Therefore, it is necessary to isolate the digital from the analog otherwise the analog performance can be degraded to a point of non-conformance.

***Is it necessary to isolate the transmit analog from the receive analog?***

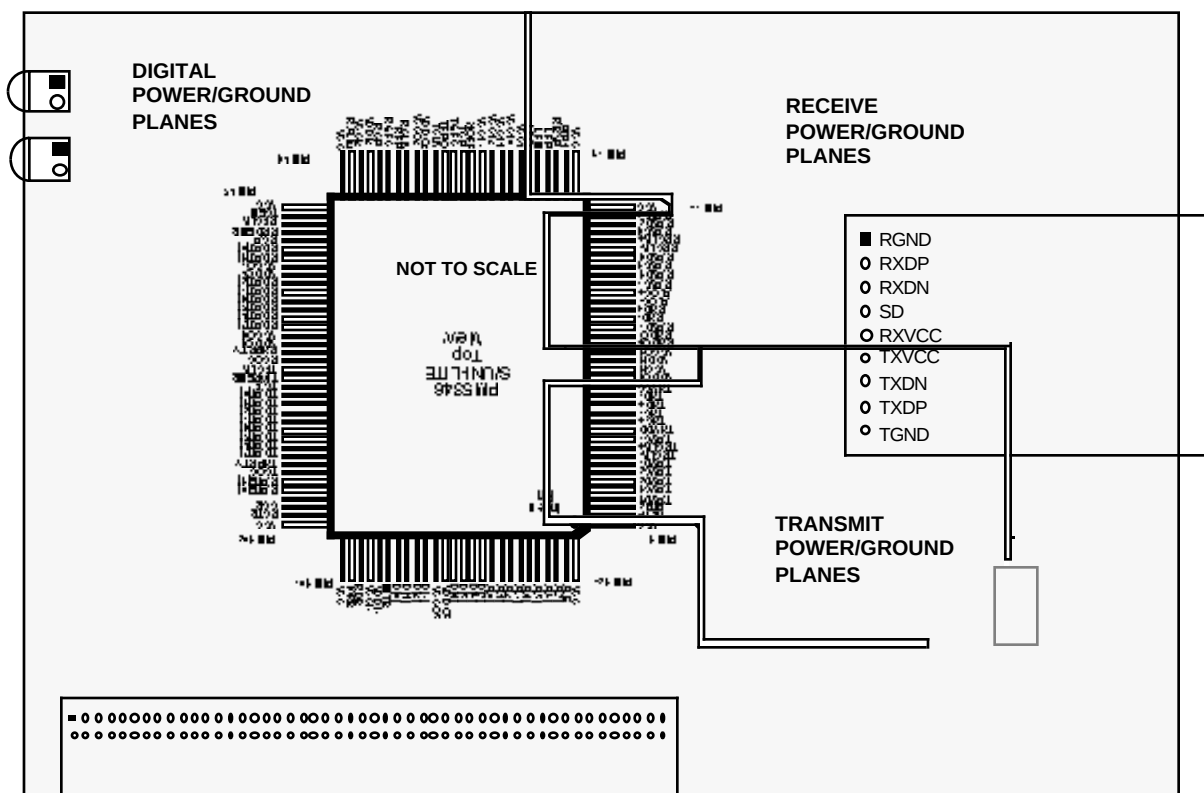
Any noise on the S/UNI-LITE receive analog power and ground inputs or on the PECL inputs will impact the internal PLL's ability to recovery the clock from the incoming data. Added noise will degrade jitter tolerance and add jitter to the recovered clock. It is also important to keep the analog optical receiver in common with the receiver portion of the S/UNI-LITE, especially the grounds. The S/UNI-LITE PECL inputs are internally self-biased between  $V_{cc}$  and ground and are AC-coupled. Since the inputs are not true differential inputs, if the S/UNI-LITE's ground and power are in common with the optical receiver the common mode noise on the input signal is also common to the biasing reference. It is especially important to keep the ground plane between the optical receiver in common with the RAVS inputs of the S/UNI-LITE.

On the transmit side of the S/UNI-LITE a 155.52 MHz clock is synthesized from a 19.44 MHz reference clock. Any added noise on the power or ground inputs impacts the resulting 155.52 MHz clock. The added noise will increase the intrinsic jitter of the transmitter. The power and ground of the optical transmitter can be in common with the analog transmit power and ground of the S/UNI-LITE.

***How to isolate the analog from the digital and the transmit from the receive?***

Since only one ground plane and one power plane is normally available, the transmit, receive, and digital power and grounds can be isolated by channels cut into the respective planes. The power and grounds should be brought from a quiet part of the board, usually where the power and grounds enter the board. Ferrite beads can also be used on the receive and transmit analog powers to prevent digital noise from entering analog circuits of the S/UNI-LITE, the PECL oscillator, and the optical transceiver.

It is important to keep the receive analog power and analog ground of the S/UNI-LITE and the receive portion of the optical transceiver power and ground common to each other.



### ***How does layout affect high speed return current?***

At low speeds return current follows the path of least resistance back to the driver. At high speeds, however, the return current follows the path of least inductance which lies on the plane directly under the signal trace, as the total loop area between the outgoing and returning paths is minimized. In other words, the high-speed return current follows a path that is almost the "mirror image" of the signal trace on the plane underneath the trace. This tight coupling provides good flux cancellation so that common-mode current is reduced. Therefore, high speed traces should not cross cuts or heavily perforated areas (where tight spacing through-hole components reside) on the power and ground planes, as any cuts on these planes may interrupt the return currents, causing them to seek alternative paths back to the driver. The different routes taken by the outgoing and return currents will both induce common-mode noise on other nearby signal traces. In addition, by routing high speed signals over continuous power planes, the return current paths of these signals are known and other signals will not cross over these return currents, reducing the possibility of noise coupling. Detailed discussions on high-speed design are provided by the references.

***When should ferrite beads be used?***

Ferrite beads are mainly used on power rails to pass DC current but to attenuated the higher frequency noise that is riding on the DC rail. The impedance of Ferrite beads increases with frequency. At DC the ferrite bead is like a short but at higher frequency the impedance of a ferrite bead can increase to over 100 ohms (depending on the bead and frequency). Ferrite beads attenuate high frequency noise from the power supply from getting into a circuit, but they also stop high frequency noise from leaving the circuit. It is important, therefore, to use proper bypass decoupling when using ferrite beads.

Ferrite beads should be avoided on CMOS I/O power pins as the high current switching of the CMOS circuits causes a  $\Delta I/\Delta t$  noise to be introduced into the power rail. Ferrite beads should also be avoided on the ground bus as this inhibits the return currents.

Ferrite beads can be used on the S/UNI-LITE analog power pins as they draw very little current. The ferrite beads isolate all the receive inputs from each other. As the noise frequencies and levels are different in every design, it is hard to decide if beads are necessary and at what frequency should they be effective. However, it is harder to insert a ferrite bead after the board is built than it is to short out the bead if it is not needed.

The S/UNI-LITE analog power pin RAVD2 generates a 311 MHz oscillation. If there is no ferrite bead on this input, the 311 MHz signal can get into the other analog power pins and performance can be affected.

Ferrite beads can be used on the optical receiver as the receiver portion draws very little current. Ferrite beads can also be used on the optical transmitter power rails as the transmitter drives a differential PECL pair which draws constant current. Most optical module vendors recommend using ferrite beads on both the receive and transmit power rails.

PECL (ECL) circuits draw constant current regardless of the frequency of operation as opposed to CMOS, which only draws current during switching.

***Is it necessary to de-couple every power pin of the S/UNI-LITE?***

The S/UNI-LITE can generate a lot of simultaneous switching noise, especially if the drop side clock frequencies of the transmit and receive are synchronous. It is important to decouple every power pin so that the switching currents can be satisfied and thereby reduce the amount of noise introduced into the power plane.

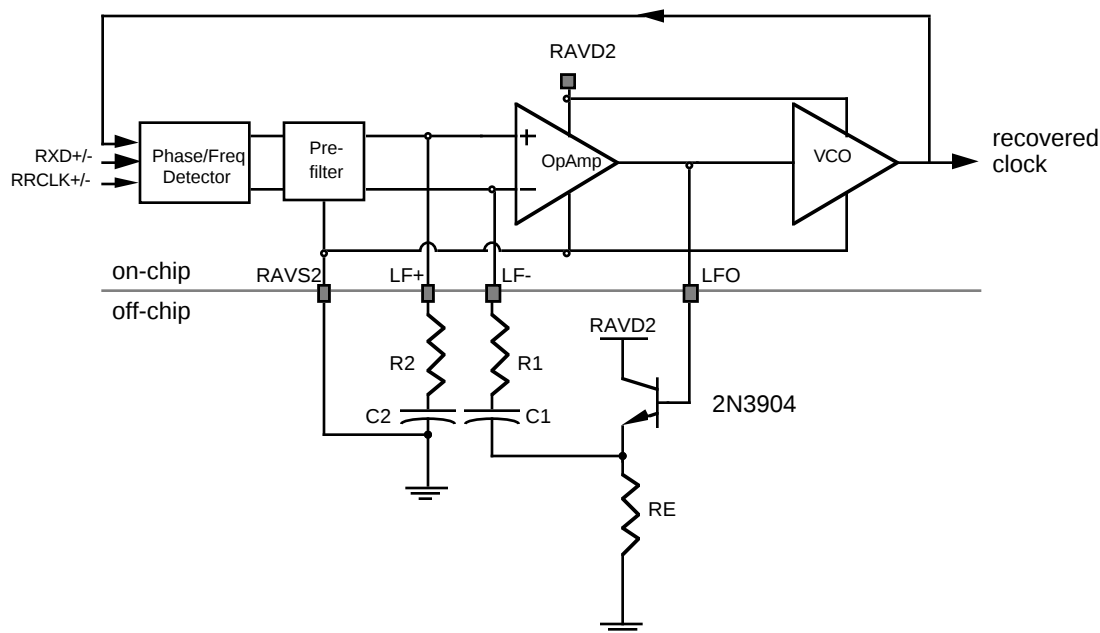
***What loop filter components should be used?***

The internal op-amp in the S/UNI-LITE's clock recovery unit (CRU) has a frequency-dependent output resistance. All amplifiers exhibit this, but the CRU's op-amp

displays a significant output resistance (approximately  $200\Omega$ ) in a frequency band that affects some signal components which feed through the PLL.

This increase in output resistance is seen in series with the external loop filter passives which set the jitter tolerance and transfer characteristics of the CRU. This effectively unbalances the loop filter signal paths, decreasing jitter tolerance.

To balance the signal paths,  $R_2$  has to be equal to  $R_2 + R_{out}$ , where  $R_{out}$  is the output resistance of the op-amp. If the output resistance of the op-amp is approximately  $200\Omega$ ,  $R_2$  would have to be at least  $200\Omega$ . However, to meet TR-NWT-000253 jitter transfer mask,  $R_2$  must be less than  $95\Omega$ . Therefore, the jitter transfer mask cannot be met unless the output resistance of the op-amp is reduced. This can be accomplished with the emitter-follower which buffers the op-amp and presents a reduced output resistance.



The recommended passive loop filter components are given in Table 1. The recommended transistor is a 2N3904 NPN transistor.

| Line Rate<br>(Mbit/s) | R1<br>( $\Omega \pm 1\%$ ) | R2<br>( $\Omega \pm 1\%$ ) | C1, C2<br>min ( $\mu\text{F}$ ) | RE<br>( $\Omega \pm 1\%$ ) | Transfer<br>Function BW<br>(kHz) |
|-----------------------|----------------------------|----------------------------|---------------------------------|----------------------------|----------------------------------|
| 155.52                | 68.1                       | 90.9                       | 4.7                             | 100                        | 80                               |
| 51.84                 | 68.1                       | 90.9                       | 15                              | 100                        | 27                               |

Table 1: Recommended Component Values

The capacitors determine the amount of "peaking" in the jitter transfer curve. "Peaking" refers to jitter amplification by the CRU. The smaller the resistor values, the larger the capacitor value needed to keep the jitter peaking below the 0.1 dB level in the specifications. Using capacitors larger than those recommended will not have any adverse affect on the performance of the S/UNI-LITE. The capacitor values can be  $\pm 10\%$ . Additionally, jitter transfer peaking increases as the line rate decreases. Therefore, the capacitors need to be increased in proportion to the decrease in line rate (i.e. half the rate requires twice the capacitance).

Since the S/UNI-LITE is a terminating device, it is not a requirement in most applications to meet jitter transfer mask. In this case the transistor can be removed and the loop filter components in Table 2 below can be used. The loop filter values were chosen to achieve maximum jitter tolerance performance in the LAN.

| Line Rate<br>(Mbit/s) | R1<br>( $\Omega$ ) | R2<br>( $\Omega$ ) | C20,<br>C21<br>min ( $\mu$ F) | Transfer<br>Function BW<br>(kHz) |
|-----------------------|--------------------|--------------------|-------------------------------|----------------------------------|
| 155.52                | 200                | 412                | 0.15                          | 450                              |
| 51.84                 | 200                | 412                | 0.47                          | 150                              |
| 25.92                 | 200                | 412                | 1.0                           | 75                               |
| 12.96                 | 200                | 412                | 2.2                           | 37.5                             |

Table 2: Recommended Component Values without Transistor

A 0.47  $\mu$ F capacitor is recommended so that the same loop filter values can be used for both the 155.52 Mbit/s and the 51.84 Mbit/s rates. If only a 155.52 Mbit/s line rate is used, the capacitor value can be reduced to 0.15  $\mu$ F and the jitter transfer peaking will still be below the 0.1 dB level. The capacitor values are the minimum recommended values; larger values of capacitance can be used on any of the line rates.

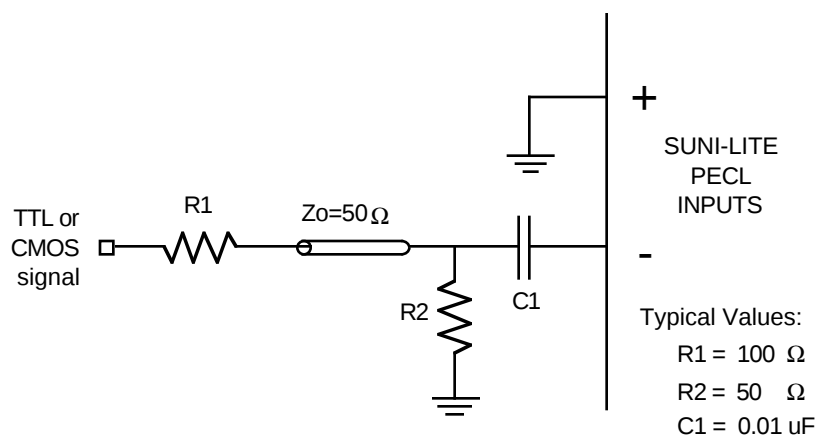
PMC document PMC-950139 has a more in-depth discussion of meeting the WAN Interface jitter transfer requirements with the S/UNI-LITE.

### ***What about reverse-biasing the capacitors during reset?***

The capacitors should be non-polarized because when the S/UNI-LITE is held in reset, the capacitors are reverse-biased at approximately 2.0V. Also, for some process extremes, the capacitors may operate with a dc reverse-bias of up to 1.0V. If polarized capacitors are used, one should ensure that the capacitors can tolerate a reverse bias of 2 Volts.

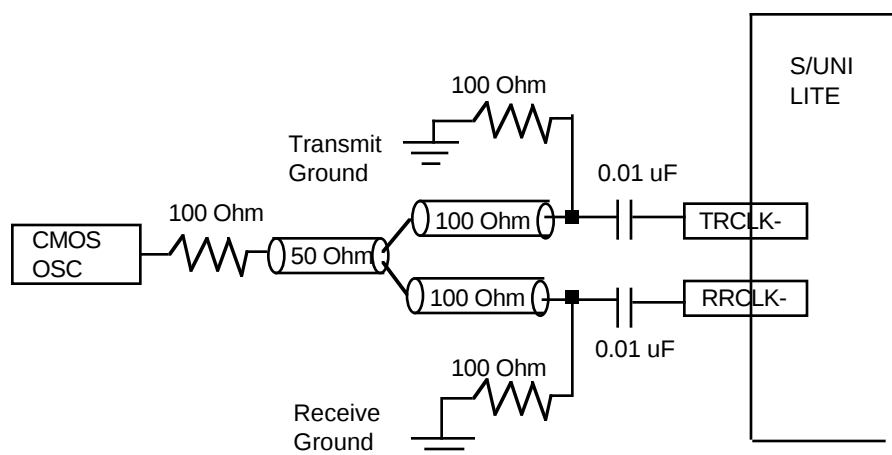
### ***How to drive the RRCLK+/- & TRCLK+/- inputs using one oscillator?***

In some applications it may be more cost effective or technically desirable to drive the RRCLK+/- and TRCLK+/- inputs with single ended TTL or CMOS signals. The following diagram demonstrates how.



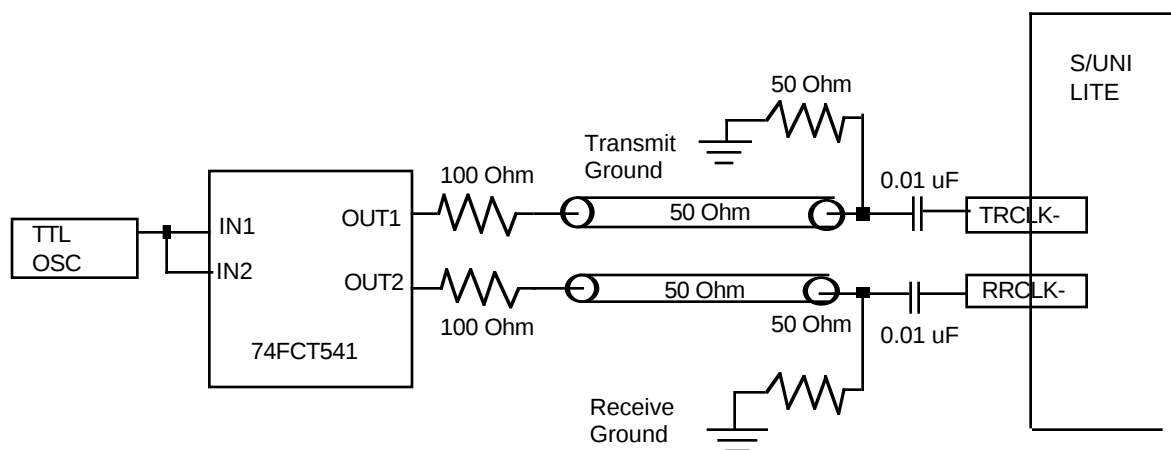
If a single TTL or CMOS oscillator is used to drive these inputs, the RRCLK- and TRCLK- inputs can be used while RRCLK+ and TRCLK+ signals are connected to their respective grounds. The single clock signal must be properly terminated. One may be tempted to connect the clock trace to either RRCLK- or TRCLK- and then run the trace to the other input and terminate at the far end. The concern is that, since the transmit and receive grounds are isolated by channels cut into the ground plane, potential difference between transmit and receive grounds will affect one of the reference clock inputs. For example, if the reference clock is terminated to the receive ground, the TRCLK input (which references to the transmit ground) will require the clock swing to be large enough to accommodate the ground difference and become more sensitive to noise than the RRCLK input. A second problem may arise if the clock signal trace crosses the cuts in the ground plane (i.e. from transmit ground island to receive ground island). In that case ground return current from the receive side cannot follow the signal trace back to the driver. Instead, it will seek an alternative path of least inductance. Consequently, this ground current will induce common-mode noise on signals nearby.

One solution may be to run a 50 ohm clock trace to the vicinity of the RRCLK- & TRCLK- inputs and then split into two 100 ohm traces. Each one of these two traces will be connected to the RRCLK- or TRCLK- input and terminated to the receive or transmit analog ground respectively. The following diagram illustrates this solution:



The drawback of the above solution is that, based on the layer setup described in Appendix F, the width of an 100 Ohm trace is less than 3 mil. This width may be difficult for board manufacturer to fabricate accurately. Inaccuracy in trace impedance will cause the signals to be improperly terminated.

The following diagram illustrates how to use a single TTL level oscillator to drive the RRCLK- & TRCLK- signals via a 74FCT541 buffer. The TRCLK+ and RRCLK+ signals are connected to their respective grounds.



The TTL oscillator should be placed as close to the buffer as possible as it is unterminated. The reason for using the TTL oscillator is to match the 74FCT541's TTL input level. A CMOS oscillator connected to these TTL inputs will cause duty cycle distortion on the output clock as TTL and CMOS signals switch at different thresholds. When a different oscillator and buffer pair is used, it is important to match the output level of the oscillator to the input level of the buffer in order to avoid duty cycle distortion.

The third alternative of using a single clock to drive both the RRCLK- and TRCLK- inputs is to use a PECL oscillator which has two outputs, each of which can be connected to RRCLK- or TRCLK- and terminated accordingly. RRCLK+ and TRCLK+ are both tied to their respective grounds. However, PECL oscillators tend to be more expensive than the combined costs of a TTL oscillator and a buffer.

### ***How accurate should the on board reference clock be?***

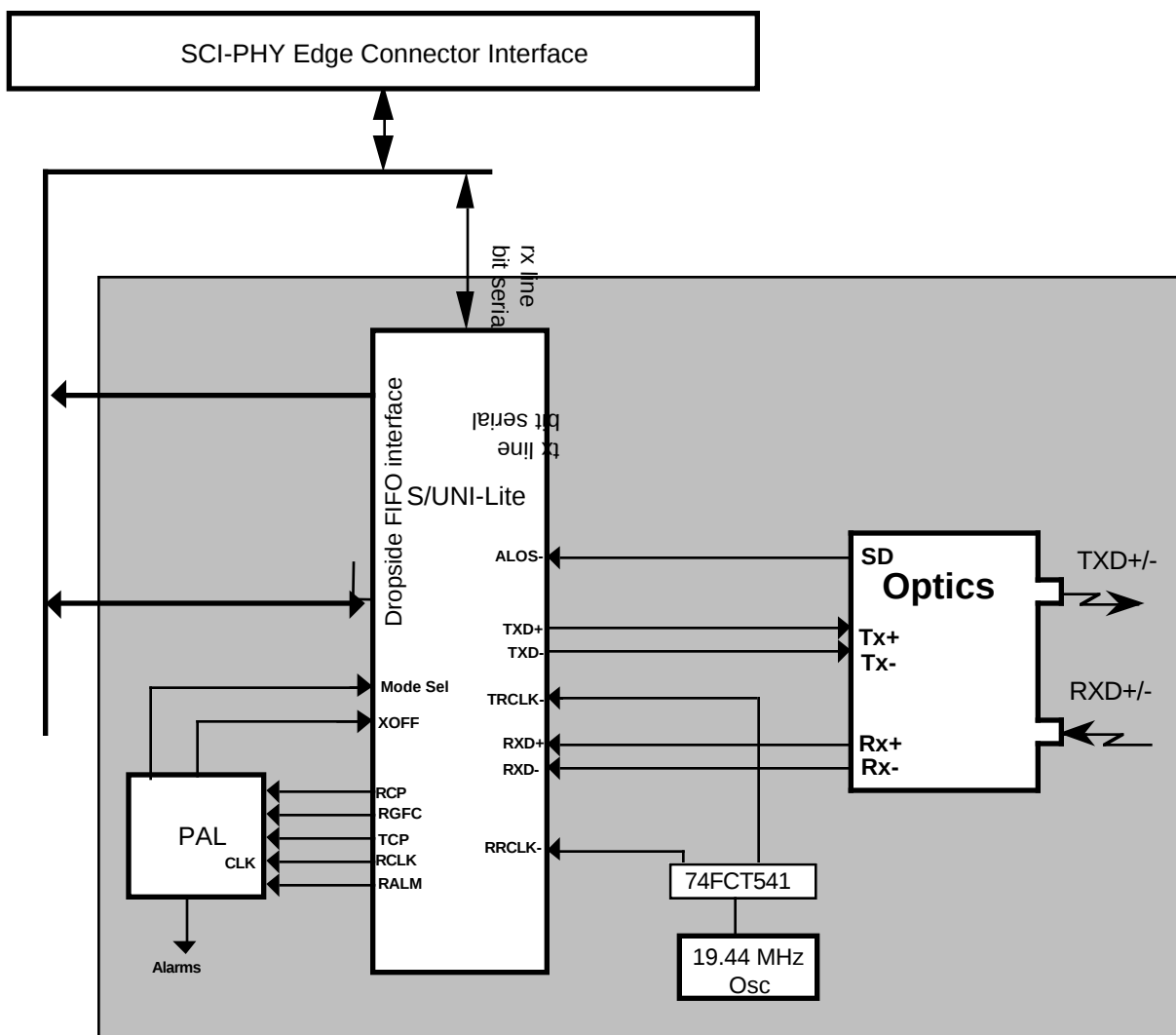
The on board reference clock is required to provide an alternative timing reference in the event that the primary timing reference becomes unavailable. For example, if the network equipment (NE) is configured for line timing mode in which the transmitted signals are timed from the clock derived from the received signal, the alternative timing reference allows the NE to provide the capability to switch to the secondary clock if the incoming signal becomes unsuitable to derive the clock from. For interfacing between WAN equipment, or between private and public ATM equipment, the Bellcore specification TR-NWT-00253, Issue 2, December 1991, Section 5.4.1, requires the accuracy of the on board reference clock to be +/- 20 ppm or better. In an interface between private ATM user devices and private ATM network equipment, the ATM Forum specification "ATM Physical Medium Interface Specification for 155 Mb/s over Twisted Pair Cable", version 1.0 Ballot Draft, 1994, requires the transmitter at the ATM user device to have a free-running transmit reference clock at 155.52 Mb/s with an accuracy of +/- 100 ppm or better. In the SORD design, a 19.44 MHz oscillator is used as a reference from which the 155.52Mb/s is generated without loss of clock accuracy. Some of the vendors that provide these 19.44 MHz oscillators are listed below:

| <b>Vendor</b>                                  | <b>+/-20ppm or better</b> | <b>+/-100ppm</b> |
|------------------------------------------------|---------------------------|------------------|
| Motron Industries<br>605-665-9321              | Yes                       | Yes              |
| Connor Winfield<br>708-851-4722                | Yes                       | Yes              |
| K&L Oscillatek                                 | Yes                       | Yes              |
| Champion<br>708-451-1000                       | Yes                       | Yes              |
| Oak Frequency Control<br>Group<br>717-486-3411 | Yes                       | Yes              |
| Ecliptek<br>714-433-1200                       | No                        | Yes              |

Table 3: 19.44 MHz Oscillator Vendors

### 3. FUNCTIONAL DESCRIPTION

#### 3.1. Block Diagram



#### 3.2. S/UNI-LITE

The S/UNI-LITE is a monolithic integrated circuit that implements the SONET/SDH processing and ATM mapping functions of a 155 Mbit/s or 51 Mbits/s ATM User Network Interface. It is the heart of the SORD board; all traffic goes through the S/UNI-LITE. On the line side, the S/UNI-LITE transmits SONET frames through the line interface and receives frames from the line interface. On the drop side, the S/UNI-LITE sinks cells provided by the buffer interface and sources cells to the buffer interface. Below, the S/UNI-LITE is briefly described.

The S/UNI-LITE receives SONET/SDH frames via a bit serial interface, recovers clock and data, and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (Z2,G1) are also accumulated. The S/UNI-LITE interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

The S/UNI-LITE frames to the ATM payload using cell delineation. Header check sequence (HCS) error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an Uncorrectable HCS error. The ATM cell payloads are descrambled. Generic flow control (GFC) bits from error free cells are extracted and presented on a serial link for external processing.

Legitimate ATM cells are written to a four cell FIFO buffer. These cells are read from the FIFO using a synchronous 8-bit wide datapath interface with cell-based handshake. Counts of received ATM cell headers that are erred and uncorrectable, and also those that are erred and correctable, are accumulated independently for performance monitoring purposes.

The S/UNI-LITE transmits SONET/SDH frames via a bit serial interface, and formats section, line, and path overhead bytes appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and inserts section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (Z2, G1) are also inserted.

The S/UNI-LITE generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. The S/UNI-LITE also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

ATM cells are written to an internal programmable-length 4-cell FIFO using a synchronous 8 bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell or the XOFF input is asserted. Generic flow control (GFC) bits may be inserted downstream of the FIFO via a serial link so that all FIFO latency may be bypassed. A Transmission Off (XOFF) input is provided to allow the suspension of active ATM cell transmission independent of the FIFO fill state.

The S/UNI-LITE generates of the header check sequence and scrambles the payload of the ATM cells. Payload scrambling can be disabled.

No line rate clocks are required directly by the S/UNI-LITE as it synthesizes the transmit clock and recovers the receive clock using a 19.44 MHz reference clock.

The S/UNI-LITE is configured, controlled and monitored via the SCI-PHY interface. It is implemented in low power, +5 Volt CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and TTL compatible outputs and is packaged in a 128 pin PQFP package.

For a complete description of the S/UNI-LITE, please refer to PMC-Sierra's PM5345 datasheet.

### **3.3. Line Interface**

The receive line interface consists of receive optics connected directly to the S/UNI-LITE RXD+/- inputs. To ensure that there is a clock in the absence of incoming light, the signal detect (SD) output of the optics is connected to the ALOS- input of the S/UNI-LITE (the ALOS+ input is grounded). In normal operation (good incoming signal) the S/UNI-LITE device recovers the clock from the incoming data. In loss of signal condition, the S/UNI-LITE will squelch the data on the receive data (RXC+/-) pins and the phase locked loop will switch to the reference clock (19.44 MHz) to keep the recovered clock in range. This technique guarantees that the S/UNI-LITE will generate a LOS indication when the optics loses incoming light.

The transmit line interface consists of the S/UNI-LITE CMOS transmit outputs which AC-coupled, attenuated, terminated, level shifted and fed into to the transmit optics.

Optical transceivers having a standard 9-pin duplex SC receptacle are used.

The S/UNI-LITE is configured for non-bypass mode (TBYP & RBYP are tied low) of operation. The 155.52 MHz transmit clock source is synthesized from a 19.44 MHz oscillator and the 155.52 MHz receive clock is recovered from the incoming data.

The S/UNI-LITE can also be configured for loop time operation.

### **3.4. GFC PAL (U9)**

The Generic Flow Control (GFC) Pal extracts the GFC bits from the generic flow control (RGFC) serial output port of the S/UNI-LITE. If the GFC[0] bit is high, the PAL will assert the transmit off (XOFF) signal going to the S/UNI-LITE XOFF input. If the XOFF input on the S/UNI-LITE is asserted high, the next cell transmitted is an idle/unassigned cell regardless of the number of cells in the FIFO.

The GFC PAL also puts the S/UNI-LITE in STS-3c/STM-1 mode by asserting the RATE1 and RATE0 input pins of the S/UNI-LITE.

The receive alarm (RALM) output signal of the S/UNI-LITE goes to the input to the GFC PAL. The RALM signal is used by the PAL to turn on a red LED when the RALM signal is high and to turn on a green LED when the RALM signal is low.

#### 4. INTERFACE DESCRIPTION

The SORD SCI-PHY Edge Connector Interface includes all the signals required to connect the SORD board to a high layer protocol entity (i.e. a AAL processor). Cells can be written to the S/UNI-LITE transmit FIFO and read from the S/UNI-LITE receive FIFO using this interface. The edge connector is made up of a 100 pin dual line female connector as shown in table below. It consists of signals appropriate to read and write to the registers of the devices on the daughter board, and it provides the necessary power and ground. TTL signal levels are used on this interface.

| Signal Name                                                                          | Type                                                                 | PIN                                     | Function                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------------------------------------------------------------------------------|----------------------------------------------------------------------|-----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND                                                                                  | Power                                                                | 1                                       | Ground                                                                                                                                                                                                                                                                                                                                                                                     |
| GND                                                                                  | Power                                                                | 2                                       | Ground                                                                                                                                                                                                                                                                                                                                                                                     |
| TDAT[0]<br>TDAT[1]<br>TDAT[2]<br>TDAT[3]<br>TDAT[4]<br>TDAT[5]<br>TDAT[6]<br>TDAT[7] | INPUT<br>INPUT<br>INPUT<br>INPUT<br>INPUT<br>INPUT<br>INPUT<br>INPUT | 3<br>5<br>9<br>11<br>4<br>6<br>10<br>12 | The S/UNI-LITE is configured for the 8 bit FIFO interface, TDAT[7:0] corresponds to a cell byte.                                                                                                                                                                                                                                                                                           |
| TPRTY                                                                                | INPUT                                                                | 14                                      | The transmit parity (TPRTY) signal indicates the parity of the TDAT[7:0] bus (odd parity). Not required.                                                                                                                                                                                                                                                                                   |
| VCC                                                                                  | Power                                                                | 7                                       | +5 Volts                                                                                                                                                                                                                                                                                                                                                                                   |
| VCC                                                                                  | Power                                                                | 8                                       | +5 Volts                                                                                                                                                                                                                                                                                                                                                                                   |
| GND                                                                                  | Power                                                                | 13                                      | Ground                                                                                                                                                                                                                                                                                                                                                                                     |
| TSOC                                                                                 | INPUT                                                                | 15                                      | The transmit start of cell (TSOC) signal marks the start of cell on the TDAT[7:0] bus. When TSOC is high, the first octet of the cell is present on the TDAT[7:0] stream. It is not necessary for TSOC to be present at each cell. An interrupt may be generated on the INTB signal if TSOC is high during any byte other than the first byte. TSOC is sampled on the rising edge of TFCLK |
| GND                                                                                  | Power                                                                | 16                                      | Ground                                                                                                                                                                                                                                                                                                                                                                                     |
| GND                                                                                  | Power                                                                | 17                                      | Ground                                                                                                                                                                                                                                                                                                                                                                                     |

|       |       |    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|-------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TCA   | O     | 18 | The transmit cell available (TCA) signal indicates when a cell is available in the S/UNI-LITE transmit FIFO. When high, TCA indicates that the S/UNI-LITE transmit FIFO is not full and a complete cell may be written in. When TCA goes low, it indicates either that the S/UNI-LITE transmit FIFO is near full and can accept no more than four writes or that the transmit FIFO is full. Selection is made using a register bit in the S/UNI-LITE TACP FIFO Control register. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the S/UNI-LITE TACP FIFO Control register. If the programmed depth is less than four, additional cells may be written after TCA is asserted. TCA is updated on the rising edge of TFCLK. The active polarity of this signal is programmable in the S/UNI-LITE and defaults to active high. |
|       |       | 19 | No Connect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| GND   | Power | 20 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| GND   | Power | 21 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| TFCLK | INPUT | 22 | The transmit write clock (TFCLK) is used to write ATM cells to the SUNI-Lite four cell transmit FIFO. TFCLK cycles at a 33 MHz or lower instantaneous rate. A complete 53 octet cell must be written to the SUNI-Lite FIFO before being inserted in the synchronous payload envelope (SPE). TDAT[7:0], TXPRTY, TWRENB and TSOC are sampled on the rising edge of TFCLK. TCA is updated on the rising edge of TFCLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| TFPO  | O     | 23 | The active high framing position output (TFPO) signal is an 8 kHz timing marker for the transmitter TFPO goes high for a single TCLK period once every 2430 TCLK cycles. TFPO is updated on the rising edge of TCLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| GND   | Power | 24 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| GND   | Power | 25 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| TXXON | O     | 26 | PHY layer flow control. 1= Xon, 0= Xoff. Asserted by the PHY layer for normal transmission. Deasserted by the PHY layer when the ATM link is experiencing congestion. The response of the ATM layer to this signal is user defined.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

|                                                                                      |                                      |                                              |                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------------------------------------------------------------------|--------------------------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TWRENB                                                                               | INPUT                                | 27                                           | The active low transmit write enable Input (TWRENB) is used to initiate writes to the SUNI-Lite transmit FIFO. When sampled low using the rising edge of TFCLK, the byte on TDATA[7:0] is written into the SUNI-Lite transmit FIFO. When sampled high using the rising edge of TFCLK, no write is performed. A complete 53 octet cell must be written to the SUNI-Lite transmit FIFO before it is inserted into the SPE. |
| GND                                                                                  | Power                                | 28                                           | Ground                                                                                                                                                                                                                                                                                                                                                                                                                   |
| GND                                                                                  | Power                                | 29                                           | Ground                                                                                                                                                                                                                                                                                                                                                                                                                   |
| RDAT[0]<br>RDAT[1]<br>RDAT[2]<br>RDAT[3]<br>RDAT[4]<br>RDAT[5]<br>RDAT[6]<br>RDAT[7] | O<br>O<br>O<br>O<br>O<br>O<br>O<br>O | 31<br>33<br>37<br>39<br>30<br>32<br>38<br>40 | RXDAT[7:0] corresponds to a cell byte. Please refer to the S/UNI-LITE datasheet for the byte cell data structure.                                                                                                                                                                                                                                                                                                        |
| RXPRTY                                                                               | O                                    | 34                                           | The receive parity (RXPRTY) signal indicates the parity of the RDAT[7:0] bus. Odd or even parity selection can be made using a register in the S/UNI-LITE. RXPRTY is updated on the rising edge of RFCLK.                                                                                                                                                                                                                |
| VCC                                                                                  | Power                                | 35                                           | +5 Volts                                                                                                                                                                                                                                                                                                                                                                                                                 |
| VCC                                                                                  | Power                                | 36                                           | +5 Volts                                                                                                                                                                                                                                                                                                                                                                                                                 |
| GND                                                                                  | Power                                | 41                                           | Ground                                                                                                                                                                                                                                                                                                                                                                                                                   |
|                                                                                      |                                      | 42                                           | Not used.                                                                                                                                                                                                                                                                                                                                                                                                                |
| RSOC                                                                                 | O                                    | 43                                           | The receive start of cell (RSOC) signal marks the start of cell on the RDAT[7:0] bus. When RSOC is high, the first octet of the cell is present on the RDAT[7:0] stream. RSOC is updated on the rising edge of RFCLK.                                                                                                                                                                                                    |
| GND                                                                                  | Power                                | 44                                           | Ground                                                                                                                                                                                                                                                                                                                                                                                                                   |
| GND                                                                                  | Power                                | 45                                           | Ground                                                                                                                                                                                                                                                                                                                                                                                                                   |
| RCA                                                                                  | 0                                    | 46                                           | Active high receive cell available (RCA) signal (polarity selectable in S/UNI-LITE) indicates when a cell is available. RCA can be configured to be deasserted when either zero or four bytes remain in the S/UNI-LITE FIFO. RCA is updated on the rising edge of RFCLK.                                                                                                                                                 |

|        |       |    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------|-------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RRDENB | INPUT | 47 | <p>The active low receive read enable Input (RRDENB) is used to initiate reads from the SUNI-Lite receive FIFO. When sampled low using the rising edge of RFCLK, a byte is read from the SUNI-Lite internal synchronous FIFO and output on the RDAT[7:0] bus. When sampled high using the rising edge of RFCLK, no read is performed. RRDENB must operate in conjunction with RFCLK to access the SUNI-Lite FIFO at a high enough instantaneous rate (<math>\geq 19.44</math> MHz) as to avoid FIFO overflows. The ATM layer device may deassert RRDENB at anytime it is unable to accept another byte.</p> <p>When the RCA signal is configured to be deasserted with zero octets (as opposed to four) in the SUNI-Lite FIFO, it is not an error condition to hold the read enable (RRDENB) active. In this situation, the RCA signal identifies the valid octets.</p> |
| GND    | Power | 48 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| GND    | Power | 49 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| RFCLK  | INPUT | 50 | <p>The receive read clock (RFCLK) is used to read ATM cells from the SUNI-Lite receive FIFO. RFCLK must cycle at a 33 MHz or lower instantaneous rate, but at a high enough rate to avoid FIFO overflow (<math>\geq 19.44</math> MHz @ 155.52 MHz line rate). RRDENB is sampled using the rising edge of RFCLK. RSOC, RDAT[7:0], RXPRTY and RCA are updated on the rising edge of RFCLK</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| RFP    | O     | 51 | <p>The receive frame pulse (RFP) output is an 8 kHz signal derived from the receive line clock. RFP is pulses high for one RCLK cycle every 2430 RCLK cycles for STS-3c (STM-1). RFP is updated on the rising edge of RCLK.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| GND    | Power | 52 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| GND    | Power | 53 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|        |       | 54 | Not Used                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|        |       | 55 | Not Used                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| GND    | Power | 56 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| GND    | Power | 57 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

|          |             |    |                                                                                                                                                                                                                                                                                                                                                        |
|----------|-------------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A[0]     | INPUT       | 59 | <p>The address bus A[7:0] selects specific registers during S/UNI-LITE register accesses.</p> <p>The test register select (TRS) signal selects between S/UNI-LITE normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses. TRS has an integral pull down resistor.</p> |
| A[1]     |             | 61 |                                                                                                                                                                                                                                                                                                                                                        |
| A[2]     |             | 65 |                                                                                                                                                                                                                                                                                                                                                        |
| A[3]     |             | 67 |                                                                                                                                                                                                                                                                                                                                                        |
| A[4]     |             | 58 |                                                                                                                                                                                                                                                                                                                                                        |
| A[5]     |             | 60 |                                                                                                                                                                                                                                                                                                                                                        |
| A[6]     |             | 66 |                                                                                                                                                                                                                                                                                                                                                        |
| A[7]/TRS |             | 68 |                                                                                                                                                                                                                                                                                                                                                        |
|          |             | 62 | Not Used                                                                                                                                                                                                                                                                                                                                               |
| VCC      | Power       | 63 | +5 Volts                                                                                                                                                                                                                                                                                                                                               |
| VCC      | Power       | 64 | +5 Volts                                                                                                                                                                                                                                                                                                                                               |
| GND      | Power       | 69 | Ground                                                                                                                                                                                                                                                                                                                                                 |
| GND      | Power       | 70 | Ground                                                                                                                                                                                                                                                                                                                                                 |
| D[0]     | INPUT/<br>O | 71 | <p>The bidirectional data bus D[7:0] is used during S/UNI-LITE register read and write accesses.</p>                                                                                                                                                                                                                                                   |
| D[1]     |             | 73 |                                                                                                                                                                                                                                                                                                                                                        |
| D[2]     |             | 77 |                                                                                                                                                                                                                                                                                                                                                        |
| D[3]     |             | 79 |                                                                                                                                                                                                                                                                                                                                                        |
| D[4]     |             | 74 |                                                                                                                                                                                                                                                                                                                                                        |
| D[5]     |             | 78 |                                                                                                                                                                                                                                                                                                                                                        |
| D[6]     |             | 80 |                                                                                                                                                                                                                                                                                                                                                        |
| D[7]     |             | 84 |                                                                                                                                                                                                                                                                                                                                                        |
| A[8]     | INPUT       | 72 | Address bit 8. Not Used.                                                                                                                                                                                                                                                                                                                               |
| GND      | Power       | 75 | Ground                                                                                                                                                                                                                                                                                                                                                 |
| GND      | Power       | 76 | Ground                                                                                                                                                                                                                                                                                                                                                 |
| GND      | Power       | 81 | Ground                                                                                                                                                                                                                                                                                                                                                 |
| GND      | Power       | 82 | Ground                                                                                                                                                                                                                                                                                                                                                 |
|          |             | 83 | Not Used.                                                                                                                                                                                                                                                                                                                                              |
| VCC      | Power       | 85 | +5 Volts                                                                                                                                                                                                                                                                                                                                               |
| VCC      | Power       | 86 | +5 Volts                                                                                                                                                                                                                                                                                                                                               |
|          |             | 87 | Not Used                                                                                                                                                                                                                                                                                                                                               |

|      |                   |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|-------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INTB | Open Drain Output | 88  | The active low interrupt (INTB) signal goes low when a S/UNI-LITE interrupt source is active, and that source is unmasked. The S/UNI-LITE may be enabled to report many alarms or events via interrupts. Examples are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (RDI), loss of pointer (LOP), path AIS, path RDI and many others. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output. |
| CSB  | INPUT             | 89  | The active low chip select (CSB) signal is low during S/UNI-LITE register accesses.                                                                                                                                                                                                                                                                                                                                                                                                               |
| GND  | Power             | 90  | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| GND  | Power             | 91  | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| RSTB | INPUT             | 92  | The active low reset (RSTB) signal provides an asynchronous S/UNI-LITE reset. RSTB is a Schmitt triggered Input with an integral pull up resistor.                                                                                                                                                                                                                                                                                                                                                |
| RDB  | INPUT             | 93  | The active low read enable (RDB) signal is low during S/UNI-LITE register read accesses. The S/UNI-LITE drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.                                                                                                                                                                                                                                                                                              |
| GND  | Power             | 94  | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| GND  | Power             | 95  | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| RDY  |                   | 96  | Not Used                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| WRB  | INPUT             | 97  | The active low write strobe (WRB) signal is low during a S/UNI-LITE register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.                                                                                                                                                                                                                                                                                             |
| ALE  | INPUT             | 98  | The address latch enable (ALE) is active high and latches the address bus A[7:0] when low. When ALE is high, the internal S/UNI-LITE address latches are transparent. It allows the S/UNI-LITE to interface to a multiplexed address/data bus. The S/UNI-LITE ALE has an integral pull up resistor. Not Used.                                                                                                                                                                                     |
| GND  | Power             | 99  | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| GND  | Power             | 100 | Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

## 5. S/UNI-LITE REGISTER ADDRESS MAP

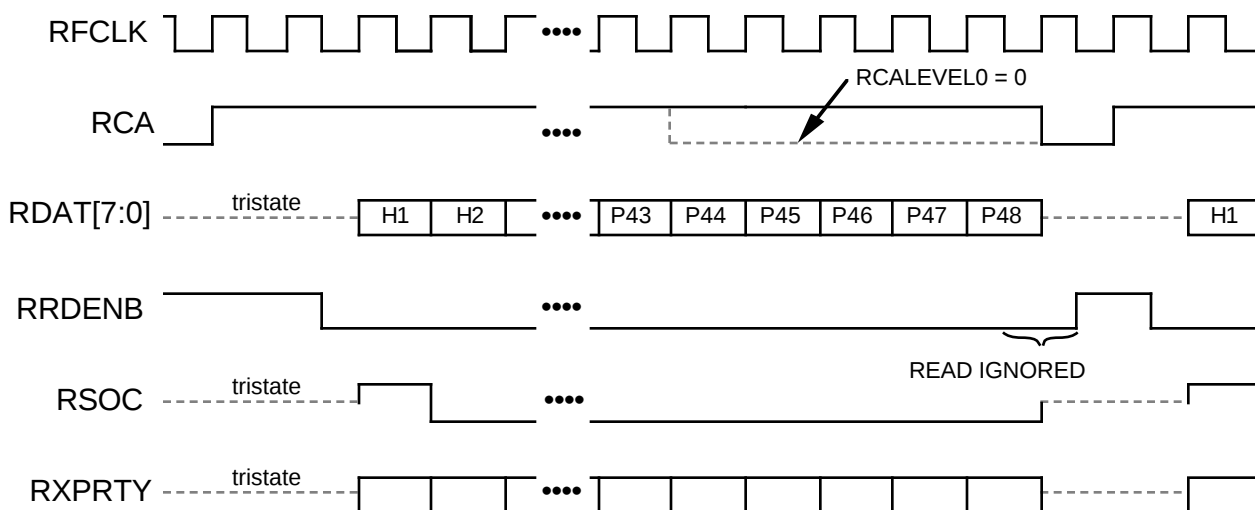
The microprocessor interface provides access to the S/UNI-LITE device registers via the 100 pin SCI-PHY connector. The S/UNI-LITE address space extends from 00H to FFH. Address bit 7 (A7 being the most significant bit and A0 being the least significant bit) is set low to access the S/UNI-LITE register space. Below is a list of the device registers. For further details, please refer to the S/UNI-LITE Datasheet.

| Address   | Register                                           |
|-----------|----------------------------------------------------|
| 0x00      | S/UNI-LITE Master Reset and Identity / Load Meters |
| 0x01      | S/UNI-LITE Master Configuration                    |
| 0x02      | S/UNI-LITE Master Interrupt Status                 |
| 0x04      | S/UNI-LITE Master Clock Monitor                    |
| 0x05      | S/UNI-LITE Master Control                          |
| 0x06      | S/UNI-LITE Clock Synthesis Control and Status      |
| 0x07      | S/UNI-LITE Clock Recovery Control and Status       |
| 0x08-0x0B | Reserved                                           |
| 0x0C-0x0F | Reserved                                           |
| 0x10      | RSOP Control/Interrupt Enable                      |
| 0x11      | RSOP Status/Interrupt Status                       |
| 0x12      | RSOP Section BIP-8 LSB                             |
| 0x13      | RSOP Section BIP-8 MSB                             |
| 0x14      | TSOP Control                                       |
| 0x15      | TSOP Diagnostic                                    |
| 0x16-0x17 | TSOP Reserved                                      |
| 0x18      | RLOP Control/Status                                |
| 0x19      | RLOP Interrupt Enable/Status                       |
| 0x1A      | RLOP Line BIP-8/24 LSB                             |
| 0x1B      | RLOP Line BIP-8/24                                 |
| 0x1C      | RLOP Line BIP-8/24 MSB                             |
| 0x1D      | RLOP Line FEBE LSB                                 |
| 0x1E      | RLOP Line FEBE                                     |
| 0x1F      | RLOP Line FEBE MSB                                 |
| 0x20      | TLOP Control                                       |
| 0x21      | TLOP Diagnostic                                    |
| 0x22-0x23 | TLOP Reserved                                      |
| 0x24-0x27 | Reserved                                           |
| 0x28-0x2B | Reserved                                           |
| 0x2C-0x2F | Reserved                                           |
| 0x30      | RPOP Status/Control                                |
| 0x31      | RPOP Interrupt Status                              |
| 0x32      | RPOP Reserved                                      |
| 0x33      | RPOP Interrupt Enable                              |
| 0x34      | RPOP Reserved                                      |
| 0x35      | RPOP Reserved                                      |

|           |                                                 |
|-----------|-------------------------------------------------|
| 0x36      | RPOP Reserved                                   |
| 0x37      | RPOP Path Signal Label                          |
| 0x38      | RPOP Path BIP-8 LSB                             |
| 0x39      | RPOP Path BIP-8 MSB                             |
| 0x3A      | RPOP Path FEBE LSB                              |
| 0x3B      | RPOP Path FEBE MSB                              |
| 0x3C      | RPOP Reserved                                   |
| 0x3D      | RPOP Path BIP-8 Configuration                   |
| 0x3E-0x3F | RPOP Reserved                                   |
| 0x40      | TPOP Control/Diagnostic                         |
| 0x41      | TPOP Pointer Control                            |
| 0x42      | TPOP Reserved                                   |
| 0x43      | TPOP Reserved                                   |
| 0x44      | TPOP Reserved                                   |
| 0x45      | TPOP Arbitrary Pointer LSB                      |
| 0x46      | TPOP Arbitrary Pointer MSB                      |
| 0x47      | TPOP Reserved                                   |
| 0x48      | TPOP Path Signal Label                          |
| 0x49      | TPOP Path Status                                |
| 0x4A      | TPOP Reserved                                   |
| 0x4B-0x4F | TPOP Reserved                                   |
| 0x50      | RACP Control/Status                             |
| 0x51      | RACP Interrupt Enable/Status                    |
| 0x52      | RACP Match Header Pattern                       |
| 0x53      | RACP Match Header Mask                          |
| 0x54      | RACP Correctable HCS Error Count                |
| 0x55      | RACP Uncorrectable HCS Error Count              |
| 0x56      | RACP Receive Cell Counter (LSB)                 |
| 0x57      | RACP Receive Cell Counter                       |
| 0x58      | RACP Receive Cell Counter (MSB)                 |
| 0x59      | RACP Configuration                              |
| 0x5A-0x5F | RACP Reserved                                   |
| 0x60      | TACP Control/Status                             |
| 0x61      | TACP Idle/Unassigned Cell Header Pattern        |
| 0x62      | TACP Idle/Unassigned Cell Payload Octet Pattern |
| 0x63      | TACP FIFO Configuration                         |
| 0x64      | TACP Transmit Cell Counter (MSB)                |
| 0x65      | TACP Transmit Cell Counter (MSB)                |
| 0x66      | TACP Transmit Cell Counter (MSB)                |
| 0x67      | TACP Configuration                              |
| 0x68-0x7F | Reserved                                        |
| 0x80      | S/UNI-LITE Master Test                          |
| 0x81-0xFF | Reserved for Test                               |

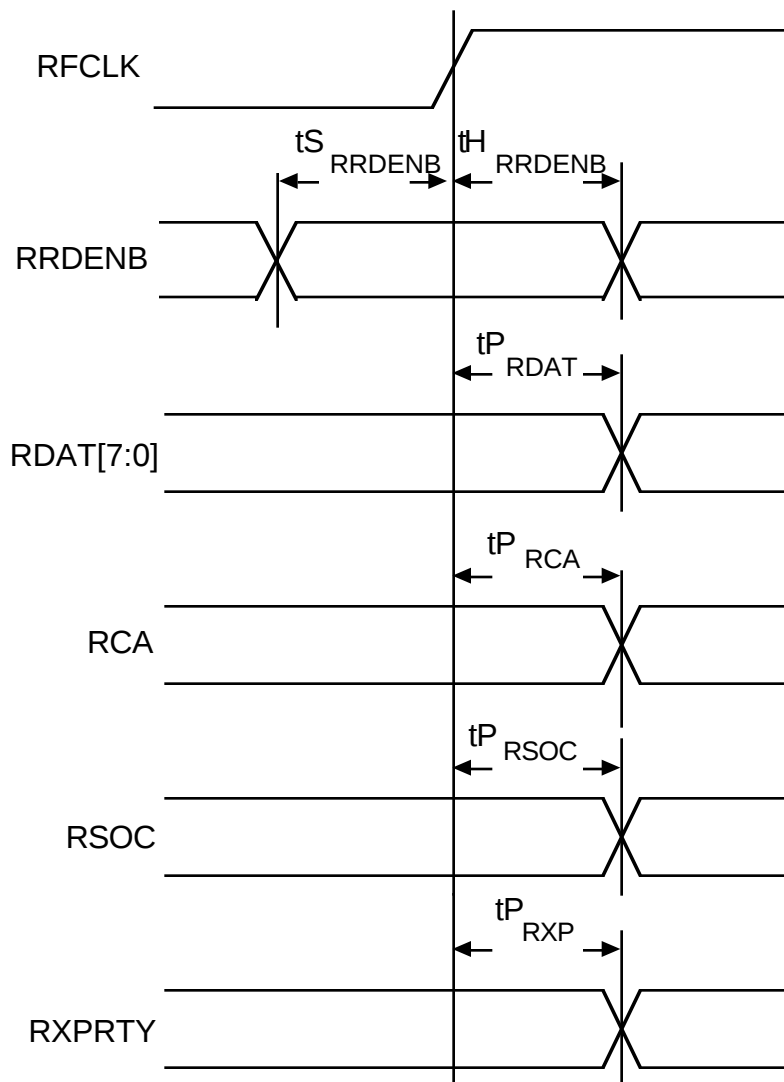
## 6. RECEIVE DROP SIDE TIMING

### 6.1. Receive Functional Timing



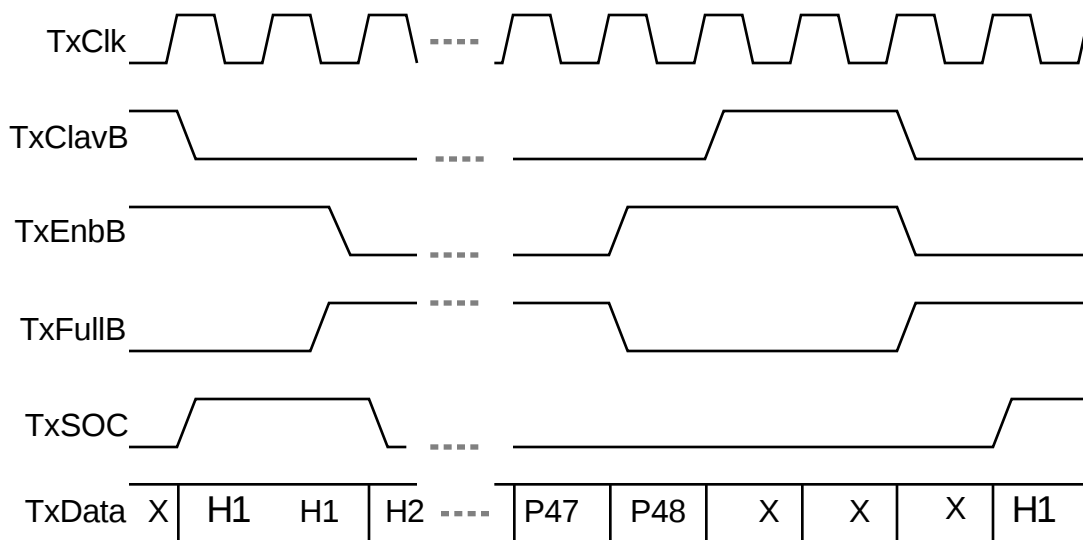
### 6.2. Receive Interface Timing

| Symbol        | Description                   | Min | Max | Units |
|---------------|-------------------------------|-----|-----|-------|
|               | RFCLK Frequency               |     | 33  | MHz   |
|               | RFCLK Duty Cycle              | 40  | 60  | %     |
| $t_{SRRDENB}$ | RRDENB to RFCLK High Setup    | 10  |     | ns    |
| $t_{HRRDENB}$ | RFCLK High to RRDENB Hold     | 1   |     | ns    |
| $t_{PRDAT}$   | RFCLK High to RDAT[7:0] Valid | 2   | 20  | ns    |
| $t_{PRXP}$    | RFCLK High to RXPRTY Valid    | 2   | 20  | ns    |
| $t_{PRCA}$    | RFCLK High to RCA Valid       | 2   | 20  | ns    |
| $t_{PRSOC}$   | RFCLK High to RSOC Valid      | 2   | 20  | ns    |



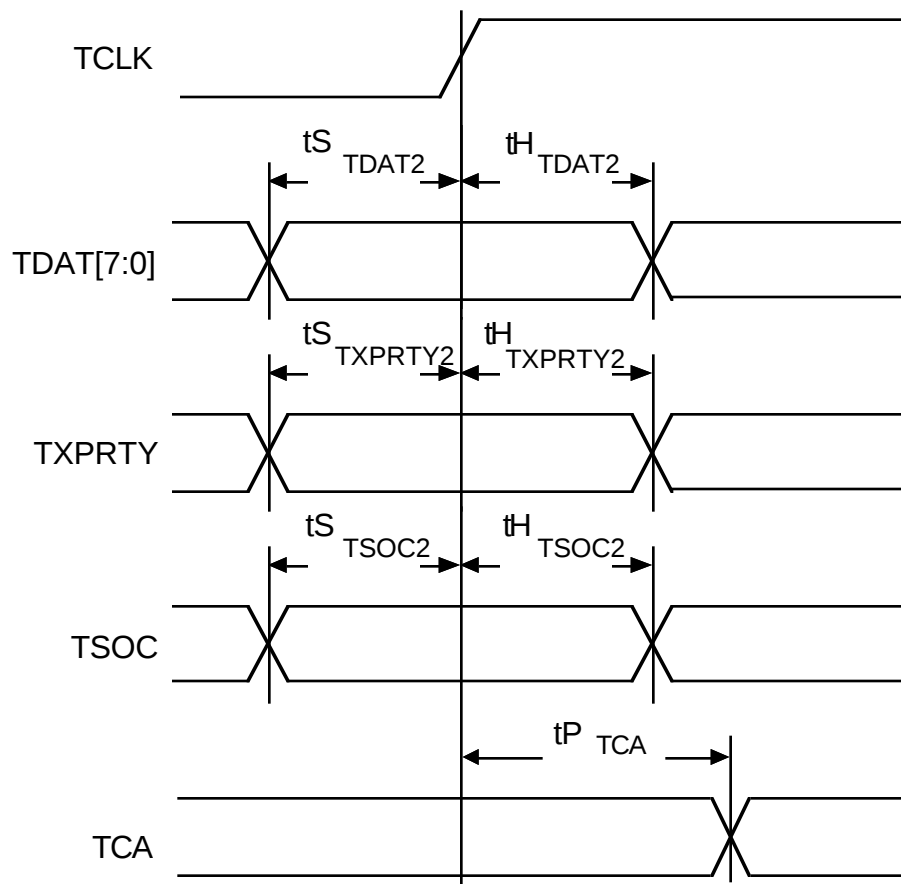
## 7. TRANSMIT DROP SIDE TIMING

### 7.1. Transmit Functional Timing



### 7.2. Transmit Interface Timing

| Symbol               | Description                    | Min | Max | Units |
|----------------------|--------------------------------|-----|-----|-------|
|                      | TFCLK Frequency                |     | 33  | MHz   |
|                      | TFCLK Duty Cycle               | 40  | 60  | %     |
| t <sub>STWRENB</sub> | TWRENB Set-up time to TFCLK    | 10  |     | ns    |
| t <sub>HTWRENB</sub> | TWRENB Hold time to TFCLK      | 1   |     | ns    |
| t <sub>STDAT</sub>   | TDAT[7:0] Set-up time to TFCLK | 10  |     | ns    |
| t <sub>HTDAT</sub>   | TDAT[7:0] Hold time to TFCLK   | 1   |     | ns    |
| t <sub>STXP</sub>    | TXPRTY Set-up time to TFCLK    | 10  |     | ns    |
| t <sub>HTXP</sub>    | TXPRTY Hold time to TFCLK      | 1   |     | ns    |
| t <sub>STSOC</sub>   | TSOC Set-up time to TFCLK      | 10  |     | ns    |
| t <sub>HTSOC</sub>   | TSOC Hold time to TFCLK        | 1   |     | ns    |
| t <sub>PTCA</sub>    | TFCLK to TCA Valid             | 2   | 20  | ns    |



## 8. DC CHARACTERISTICS

| Symbol           | Parameter                   | Min  | Max  | Units | Test Conditions                   |
|------------------|-----------------------------|------|------|-------|-----------------------------------|
| V <sub>5DC</sub> | +5V DC Power Supply Voltage | 4.75 | 5.25 | V     |                                   |
| I <sub>5DC</sub> | +5V DC Power Supply Current |      | 1.50 | A     | V <sub>5DC</sub> = 5.0 V $\pm$ 5% |
| T <sub>A</sub>   | Ambient Temperature         | 0    | 70   | °C    | V <sub>DC</sub> = 5.0 V $\pm$ 5%  |

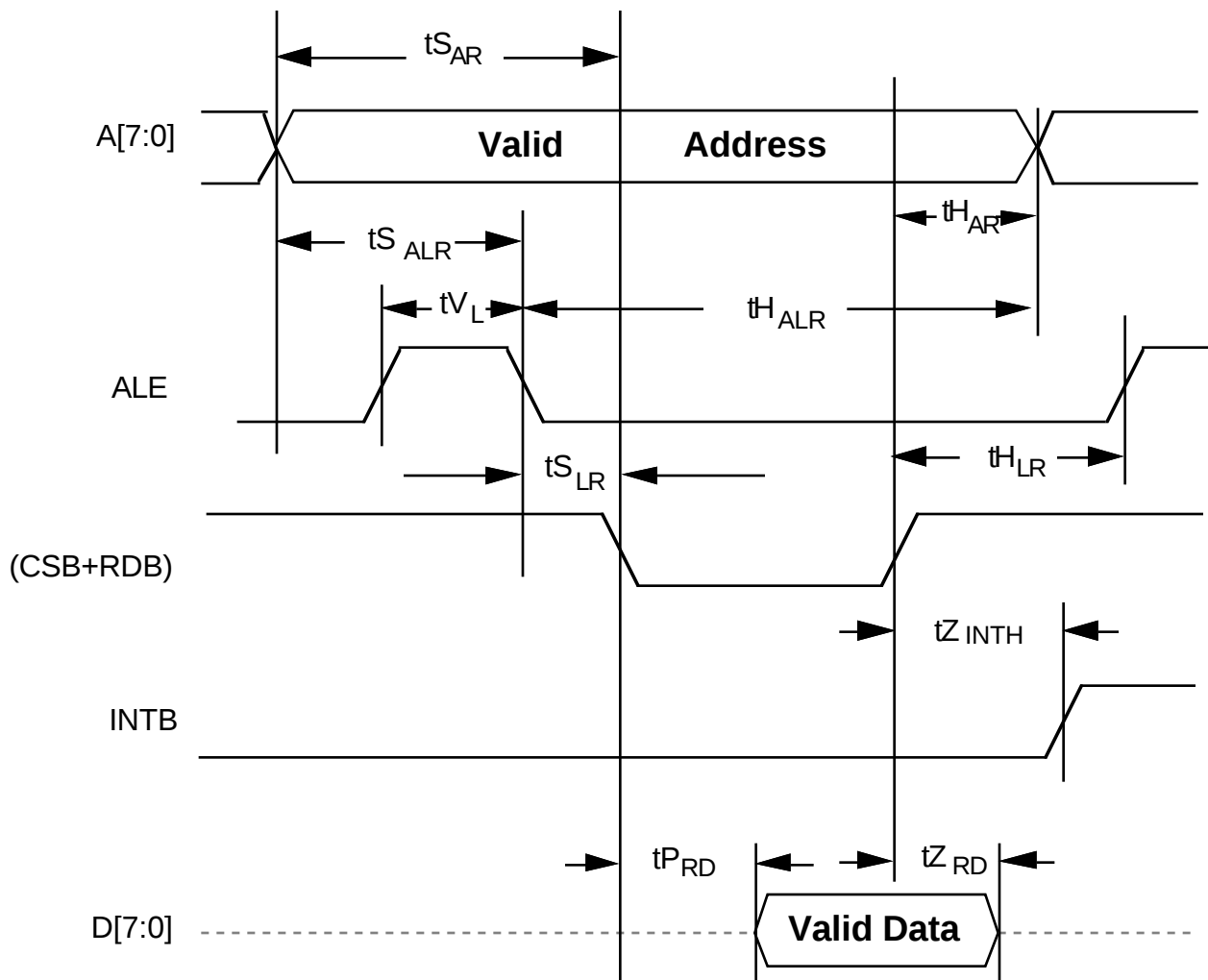
## 9. MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T<sub>A</sub> = 0°C to +70°C, V<sub>DD</sub> = 5 V  $\pm$ 10%)

### 9.1. Microprocessor Interface Read Access

| Symbol             | Parameter                                  | Min | Max | Units |
|--------------------|--------------------------------------------|-----|-----|-------|
| t <sub>SAR</sub>   | Address to Valid Read Set-up Time          | 25  |     | ns    |
| t <sub>HAR</sub>   | Address to Valid Read Hold Time            | 5   |     | ns    |
| t <sub>SALR</sub>  | Address to Latch Set-up Time               | 20  |     | ns    |
| t <sub>HALR</sub>  | Address to Latch Hold Time                 | 10  |     | ns    |
| t <sub>VL</sub>    | Valid Latch Pulse Width                    | 20  |     | ns    |
| t <sub>SLR</sub>   | Latch to Read Set-up                       | 0   |     | ns    |
| t <sub>HLR</sub>   | Latch to Read Hold                         | 5   |     | ns    |
| t <sub>PRD</sub>   | Valid Read to Valid Data Propagation Delay |     | 80  | ns    |
| t <sub>ZRD</sub>   | Valid Read Negated to Output Tri-state     |     | 20  | ns    |
| t <sub>ZINTH</sub> | Valid Read Negated to Output Tri-state     |     | 50  | ns    |

## 9.2. Microprocessor Interface Read Timing



## 9.3. Notes on Microprocessor Interface Read Timing:

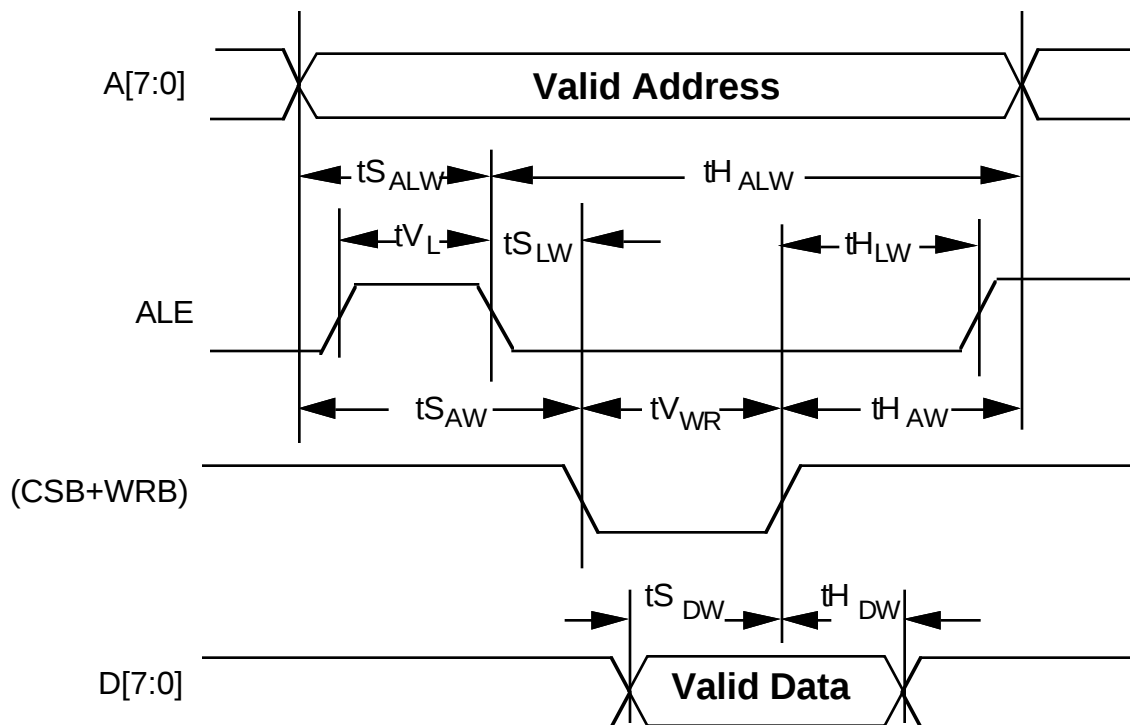
1. Output propagation delay time is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
3. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

4. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

#### 9.4. Microprocessor Interface Write Access

| Symbol            | Parameter                          | Min | Max | Units |
|-------------------|------------------------------------|-----|-----|-------|
| t <sub>SAW</sub>  | Address to Valid Write Set-up Time | 25  |     | ns    |
| t <sub>SDW</sub>  | Data to Valid Write Set-up Time    | 20  |     | ns    |
| t <sub>SALW</sub> | Address to Latch Set-up Time       | 20  |     | ns    |
| t <sub>HALW</sub> | Address to Latch Hold Time         | 10  |     | ns    |
| t <sub>VL</sub>   | Valid Latch Pulse Width            | 20  |     | ns    |
| t <sub>SLW</sub>  | Latch to Write Set-up              | 0   |     | ns    |
| t <sub>HLW</sub>  | Latch to Write Hold                | 5   |     | ns    |
| t <sub>HDW</sub>  | Data to Valid Write Hold Time      | 5   |     | ns    |
| t <sub>HAW</sub>  | Address to Valid Write Hold Time   | 5   |     | ns    |
| t <sub>WR</sub>   | Valid Write Pulse Width            | 40  |     | ns    |

### 9.5. Microprocessor Interface Write Timing



### 9.6. Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor Interface timing applies to normal mode register accesses only.
3. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
4. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

**APPENDIX A: PAL EQUATIONS**

```
-- Generic Flow Control and Alarms PAL U9
-- Used to generate
--   RALM alarm
--   Generic Flow Control Signals
--   Select Line Rate Mode Pins
```

```
USE work.bv_math.all;      -- necessary for inc_bv();
USE work.rtlpkg.all;
USE work.cypress.all;
```

```
ENTITY gfc_pal IS
    PORT (rclk, rcp,rgfc,ralm,rstb : IN BIT;
          xoff,txxon,rate1,rate0,red_ralm,green_ralm: OUT BIT);

    ATTRIBUTE order_code of gfc_pal:ENTITY IS "PAL22V10D-10JC";
    ATTRIBUTE part_name of gfc_pal:ENTITY IS "C22V10";
```

```
ATTRIBUTE pin_numbers of
    gfc_pal:ENTITY IS "rclk:2  " &
    "rcp:5      " &
    "rgfc:6      " &
    "ralm:13     " &
    "rstb:16     " &
    "red_ralm:18 " &
    "green_ralm:17 " &
    "rate0:24    " &
    "rate1:25    " &
    "txxon:26    " &
    "xoff:27";
```

```
END gfc_pal;
```

```
ARCHITECTURE behavior OF gfc_pal IS
    SIGNAL count:bit_vector(1 downto 0);
    SIGNAL sample_rgfc: BIT;
    SIGNAL high :BIT := '1';
    BEGIN
        rate0 <= '1';
        rate1 <= '1';
```

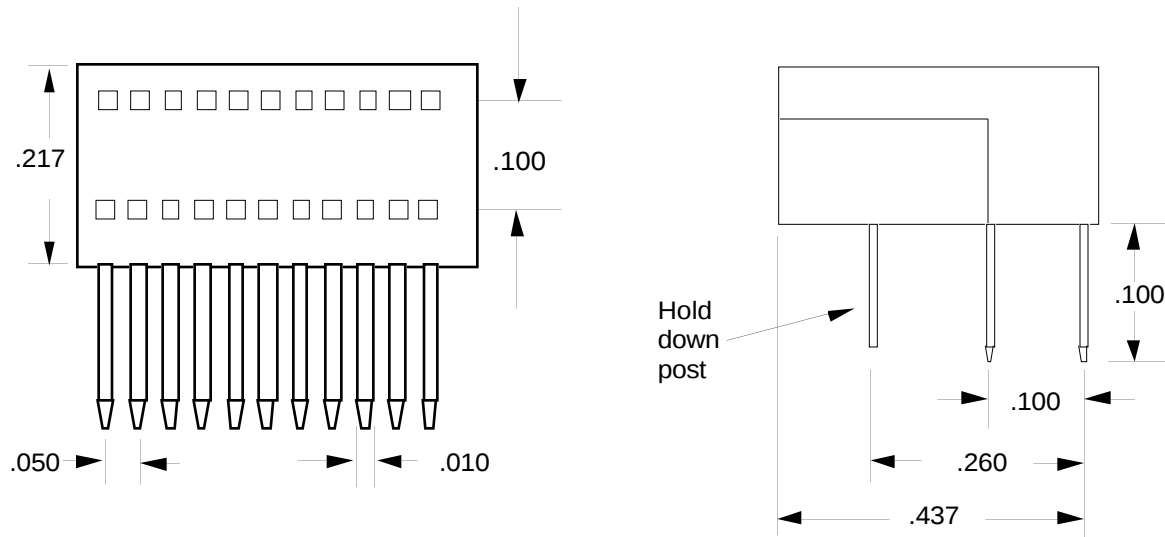
```
-- Generic Flow Control
proc1: PROCESS
```

---

```
BEGIN
  WAIT UNTIL (rclk = '1');
-- Sample RGFC & RCP
  IF (rstb = '0') THEN
    count <= "11";
    xoff <= '0';
    txxon <= '1';
  END IF;
  IF ( rcp = '1' ) THEN
    count <= "00";
  END IF;
  IF ( rgfc = '1' AND count = "10" ) THEN
    xoff <= '1';
    txxon <= '0';
  END IF;
  IF ( rgfc = '0' AND count = "10" ) THEN
    xoff <= '0';
    txxon <= '1';
  END IF;
  IF ( count /= "11" ) THEN
    Count <= inc_bv(Count); -- increment bit vector
  END IF;
END process;

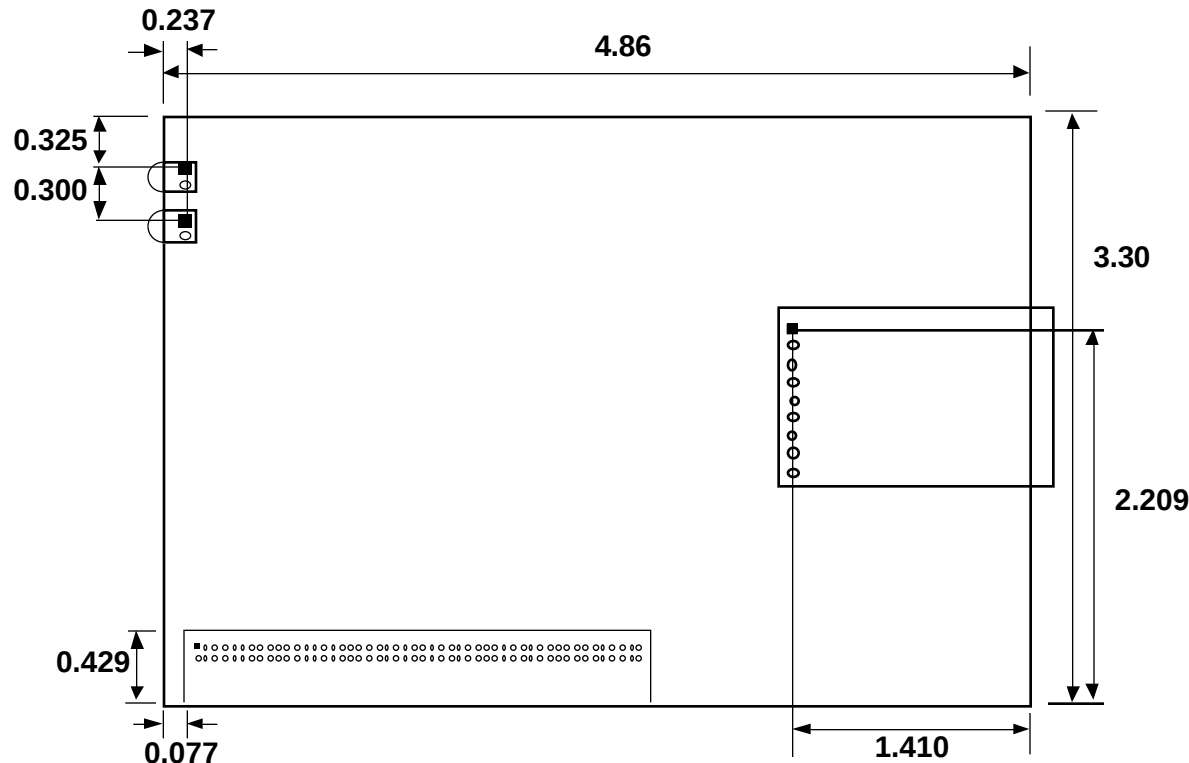
-- Set the Red RALM alarm if the RALM input is high
-- Set the Green RALM alarm if the RALM input is low
proc2: PROCESS
  BEGIN
    IF (rstb = '0' ) THEN
      green_ralm <= '1';
      red_ralm <= '0';
    ELSIF ( ralm = '0' ) THEN
      green_ralm <= '1';
      red_ralm <= '0';
    ELSE
      green_ralm <= '0';
      red_ralm <= '1';
    END IF;
  END process;
END behavior;
```

**APPENDIX B: MECHANICAL DRAWINGS**



**AMP 101911-8 Edge Connector**

Note: 100 pin, 100 position



**PCB Board Dimensions**

**APPENDIX C: MATERIAL LIST**

| Item | Refdes                                                           | Total | Description                                                                                                     |
|------|------------------------------------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------|
| 1    | C1<br>C6<br>C33                                                  | 3     | Capacitor, 100uF, electrolytic, Radial leads, 0.196" spacing                                                    |
| 2    | P1                                                               | 1     | 100 pin DIP connector, 0.050" pitch, AMP 103911-8                                                               |
| 3    | Y1                                                               | 1     | 19.44 MHz, 20 ppm, DIP Osc, 0.26" case, 14 pins DIP, TTL levels, Connor Winfield, S54R8-19.44MHz, or equivalent |
| 4    | L1<br>L2<br>L3<br>L4<br>L5<br>L6<br>L7<br>L8<br>L9<br>L10<br>L11 | 11    | Ferrite Beads, surface mount, 0.2", Fair_rite #2743019446                                                       |
| 5    | U10                                                              | 1     | Fiber Optics transceiver, 9 Pins, HP HFBR5205                                                                   |
| 6    | U5                                                               | 1     | LED, green, 0.1" spacing, Right angle                                                                           |
| 7    | U7                                                               | 1     | LED, red, 0.1" spacing, Right angle                                                                             |
| 8    | U9                                                               | 1     | CMOS PAL, 10 ns prop, 28 pins PLCC, Cypress, PAL22V10D-10JC                                                     |
| 9    | U2                                                               | 1     | Saturn User Network Interface, 128 pins PQFP, 0.50 mm pitch, PMC-Sierra PM5346                                  |
| 10   | C24<br>C38<br>C47<br>C49<br>C54<br>C57<br>C60<br>C62             | 8     | Capacitors, 0.1 uF MultiLayer Ceramic chip capacitor, 50V, Size 1206, Surface mount                             |

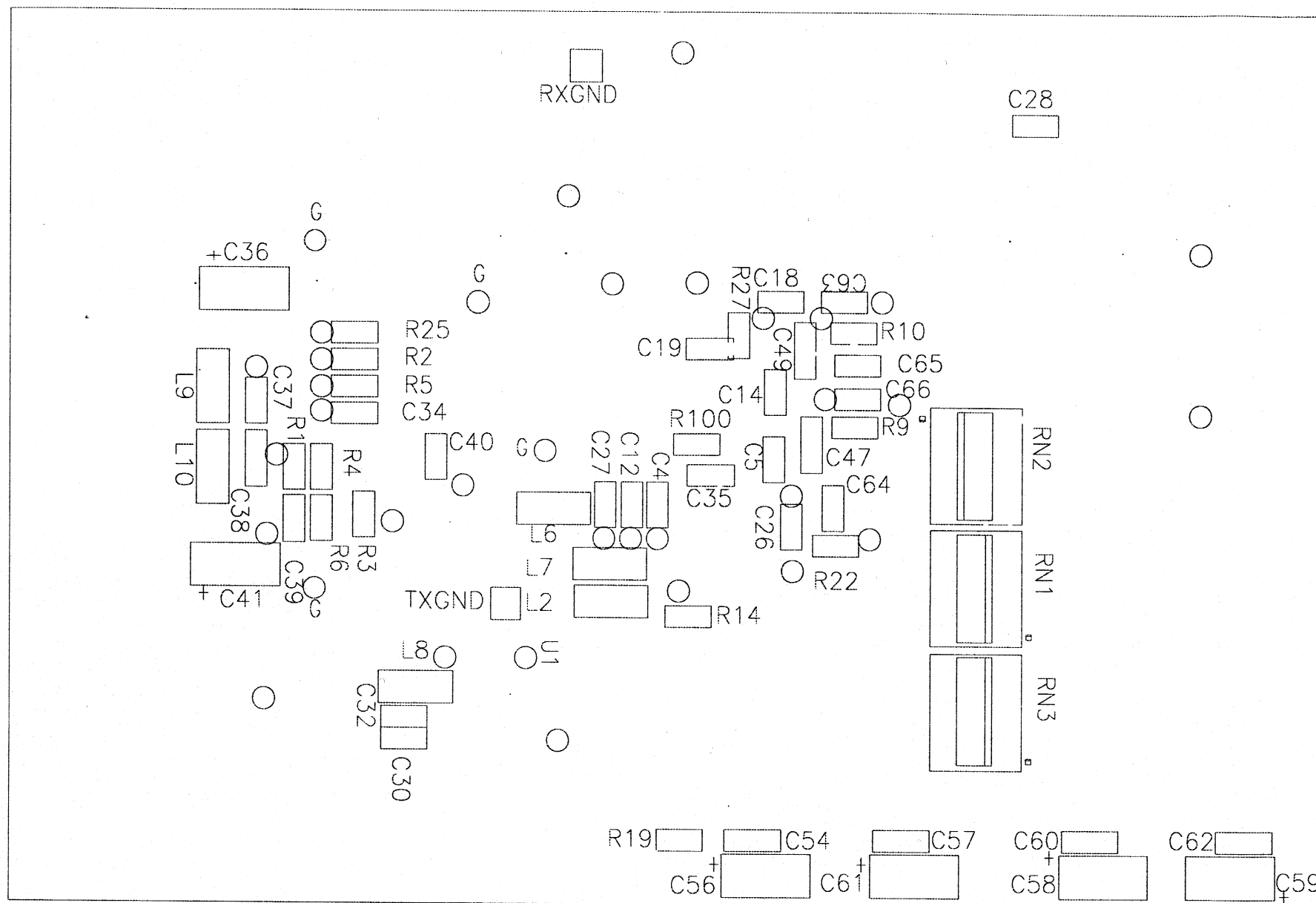
|    |                                                                                                                                                                                       |    |                                                                                      |
|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|--------------------------------------------------------------------------------------|
| 11 | C2<br>C3<br>C5<br>C9<br>C10<br>C11<br>C13<br>C14<br>C15<br>C18<br>C19<br>C22<br>C25<br>C26<br>C27<br>C28<br>C32<br>C35<br>C37<br>C39<br>C40<br>C42<br>C43<br>C63<br>C64<br>C65<br>C66 | 27 | Capacitors, 0.01 uF MultiLayer Ceramic chip capacitor, 50V, Size 805, Surface mount  |
| 12 | C17<br>C46                                                                                                                                                                            | 2  | Capacitors, 47 pF MultiLayer Ceramic chip capacitor, 50V, Size 805, Surface mount    |
| 13 | C4<br>C7<br>C8<br>C12<br>C30<br>C34<br>C45<br>C48                                                                                                                                     | 8  | Capacitors, 0.001 uF MultiLayer Ceramic chip capacitor, 50V, Size 805, Surface mount |
| 14 | R12<br>R14<br>R26                                                                                                                                                                     | 3  | Resistors, 100 ohm 1/10 watt MF 1%, Size 805, Surface mount                          |
| 15 | R22                                                                                                                                                                                   | 1  | Resistors, 10K ohm 1/10 watt MF 5%, Size 805, Surface mount                          |
| 16 | R11                                                                                                                                                                                   | 1  | Resistor, 68 ohm 1/10 watt MF 1%, Size 805, Surface mount                            |

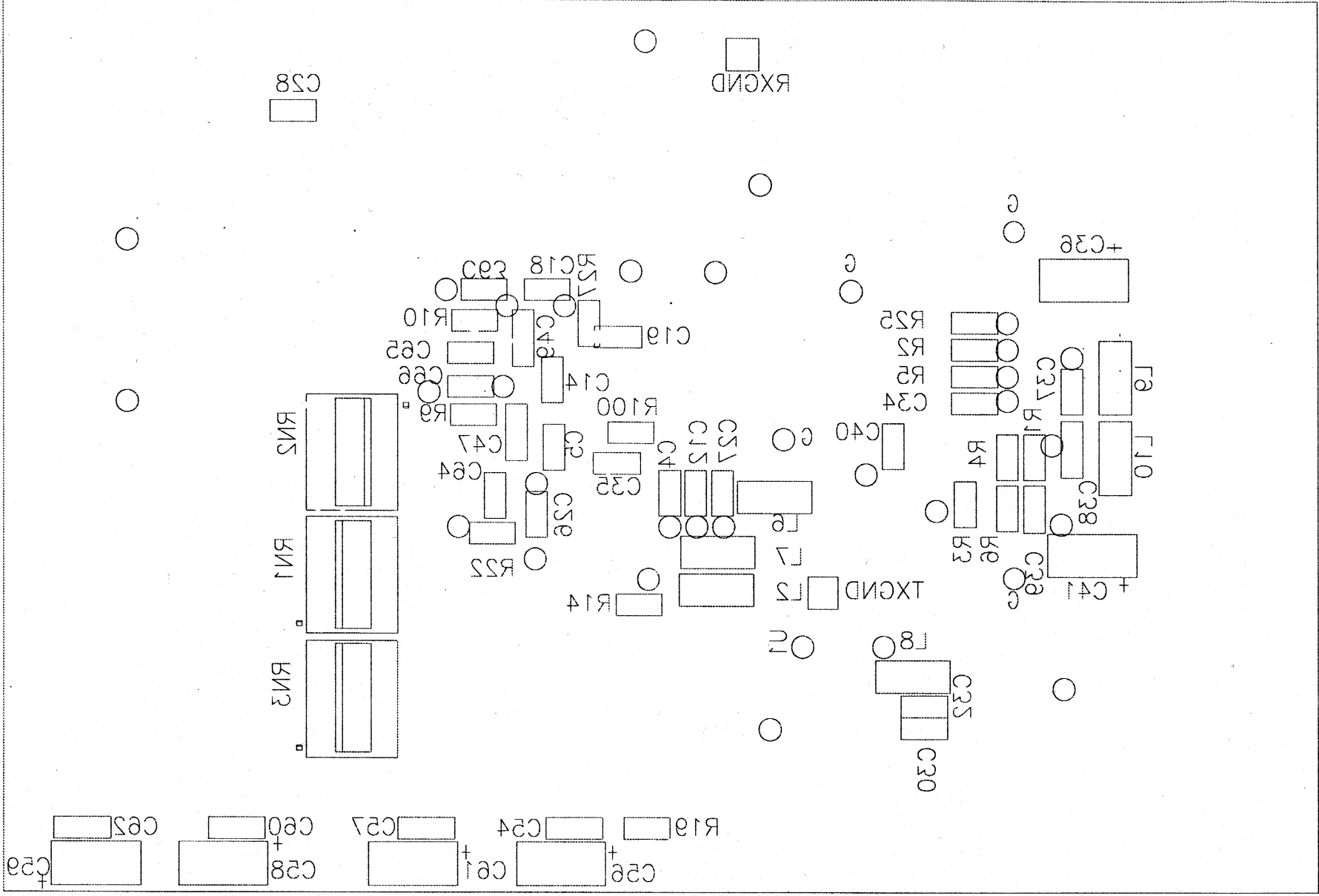
|    |                                        |   |                                                                                                                         |
|----|----------------------------------------|---|-------------------------------------------------------------------------------------------------------------------------|
| 17 | R6<br>R7<br>R8                         | 3 | Resistors, 237 ohm 1/10 watt MF 1%, Size 805, Surface mount                                                             |
| 18 | R18<br>R23                             | 2 | Resistors, 270 ohm 1/10 watt MF 5%, Size 805, Surface mount                                                             |
| 19 | R2<br>R5<br>R25                        | 3 | Resistors, 330 ohm 1/10 watt MF 1%, Size 805, Surface mount                                                             |
| 20 | R19                                    | 1 | Resistor, 4.7K ohm 1/10 watt MF 5%, Size 805, Surface mount                                                             |
| 21 | R13                                    | 1 | Resistor, 90.9 ohm 1/10 watt MF 1%, Size 805, Surface mount                                                             |
| 22 | R3<br>R4<br>R27<br>R37<br>R100         | 5 | Resistors, 49.9 ohm 1/10 watt MF 1%, Size 805, Surface mount                                                            |
| 23 | R1                                     | 1 | Resistor, 680 ohm 1/10 watt MF 1%, Size 805, Surface mount                                                              |
| 24 | R9<br>R10                              | 2 | Resistors, 75 ohm 1/10 watt MF 1%, Size 805, Surface mount                                                              |
| 25 | C36<br>C41<br>C56<br>C58<br>C59<br>C61 | 6 | Capacitors Pol. 10 uF, Panasonic TEH series, Resin molded chips tantalum electrolytic capacitor, Size C, Surface mount  |
| 26 | C16<br>C20                             | 2 | Capacitors Pol. 6.8 uF, Panasonic TEH series, Resin molded chips tantalum electrolytic capacitor, Size C, Surface mount |
| 27 | RN1<br>RN2<br>RN3                      | 3 | Chip-resistor array, 8K ohm x 8, SOIC package                                                                           |
| 28 | U1                                     | 1 | non-inverting 8-bit buffers/line drivers, Cypress, CY74FCT541, 20 pin SOIC                                              |
| 29 | Q1                                     | 1 | Discrete Transistor, 2N3904, SOT23 package                                                                              |

|    |                                                                                      |    |                                                        |
|----|--------------------------------------------------------------------------------------|----|--------------------------------------------------------|
| 30 | TP1<br>TP2<br>TP3<br>TP4<br>TP5<br>TP6<br>TP8<br>TP9<br>TP10<br>TP11<br>TP17<br>TP18 | 12 | Headers, 0.025" square pins, 0.1" spacing, 10 position |
|----|--------------------------------------------------------------------------------------|----|--------------------------------------------------------|

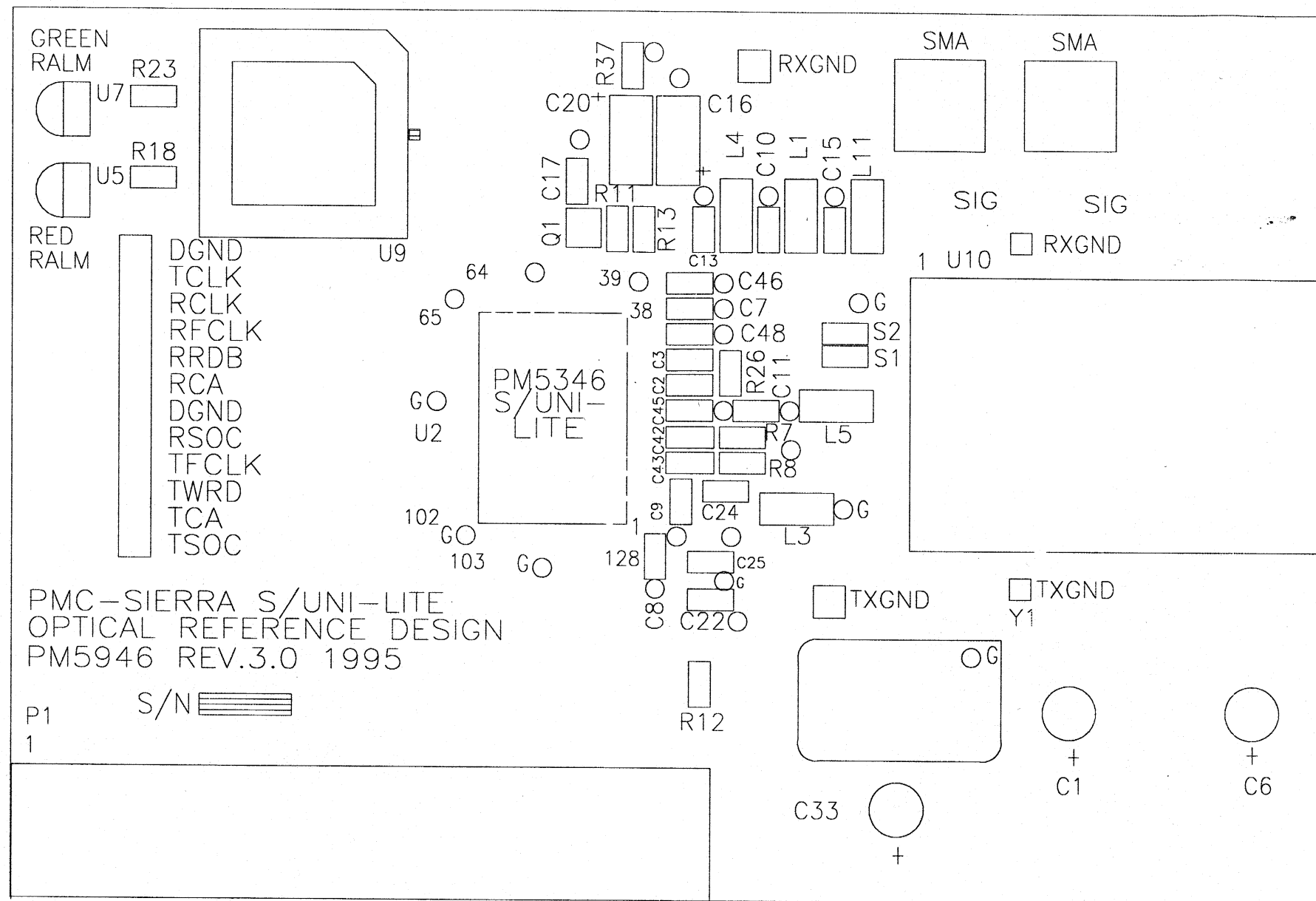
**APPENDIX D: COMPONENT PLACEMENT**

SILK\_SCREEN BOTTOM

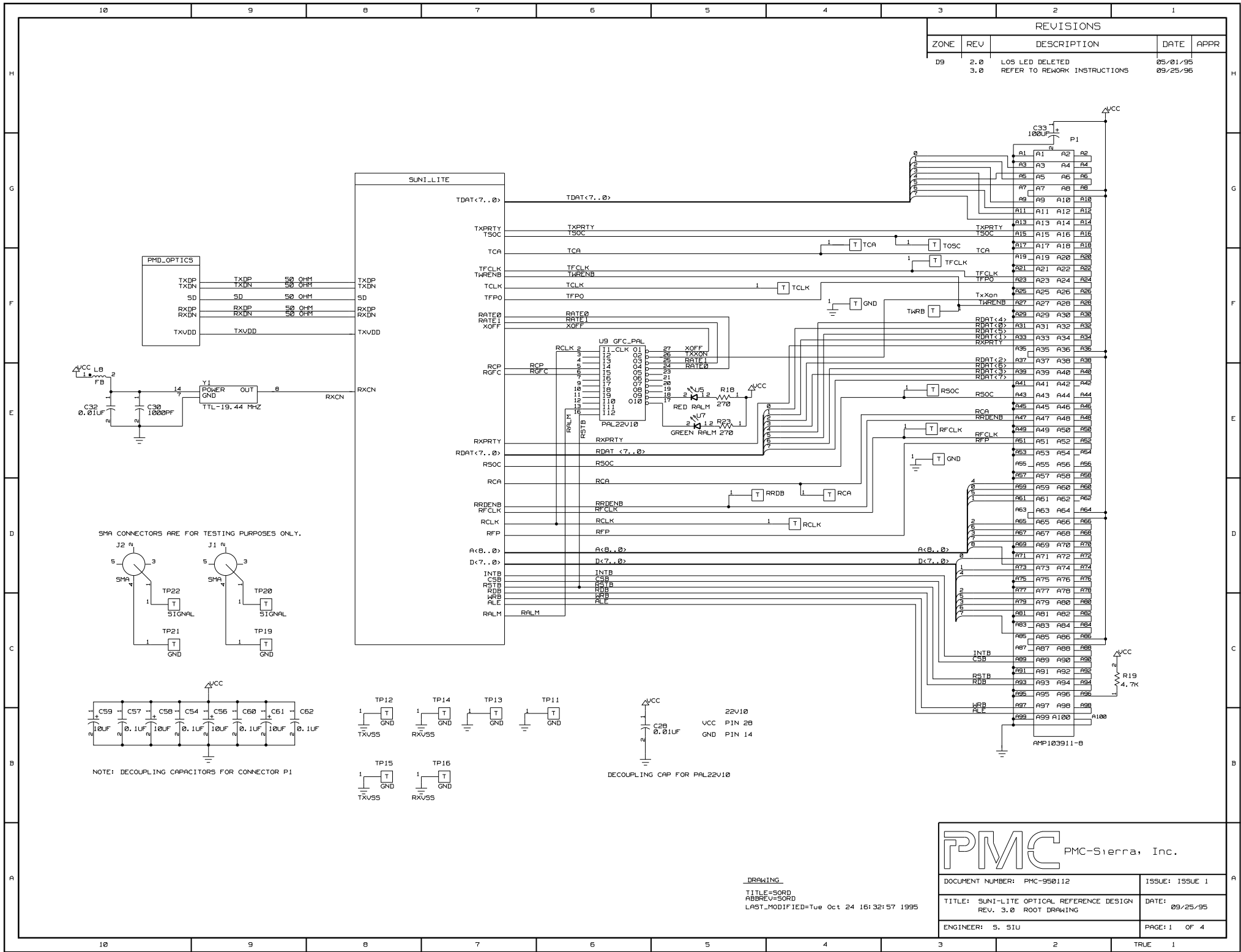




# SILK\_SCREEN TOP



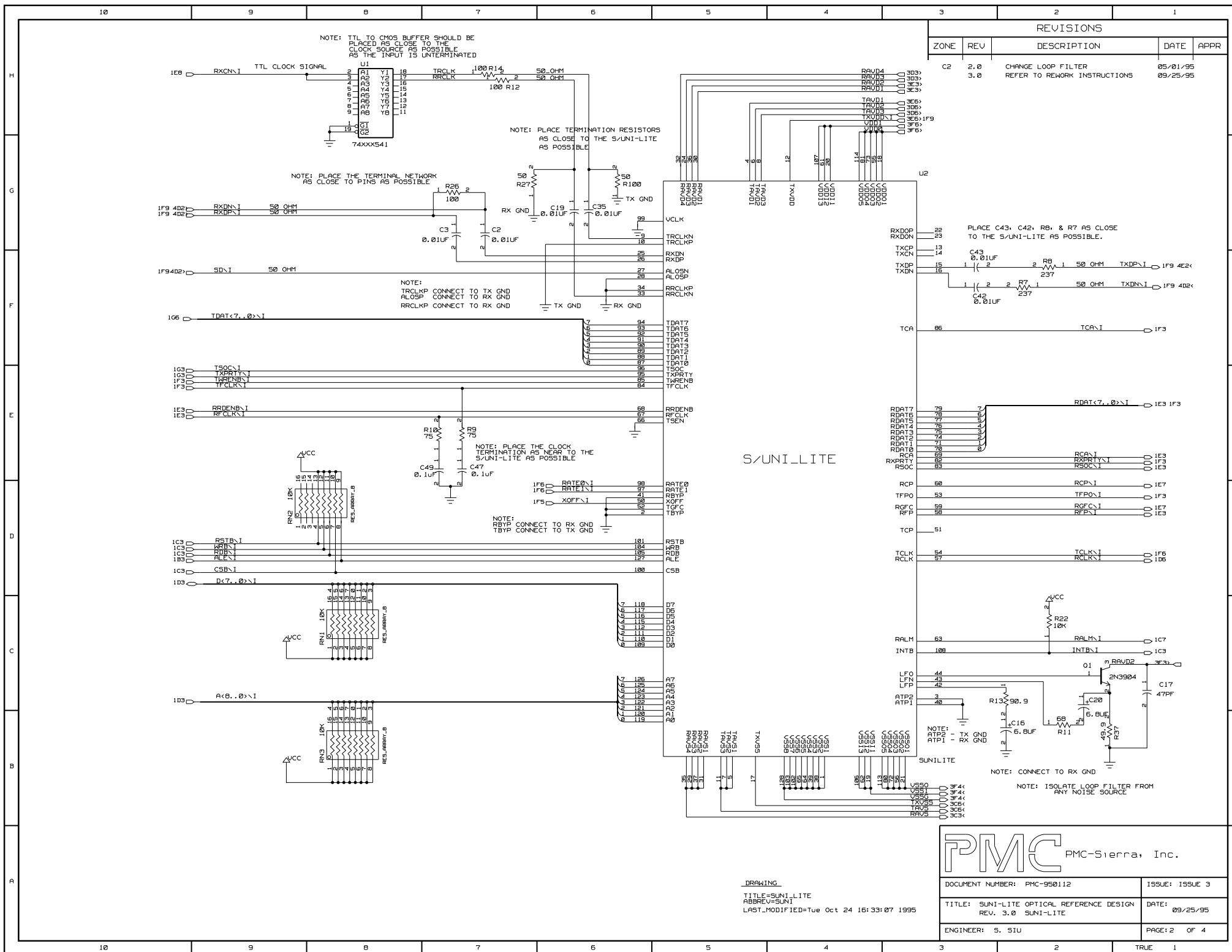
**APPENDIX E: SCHEMATICS**

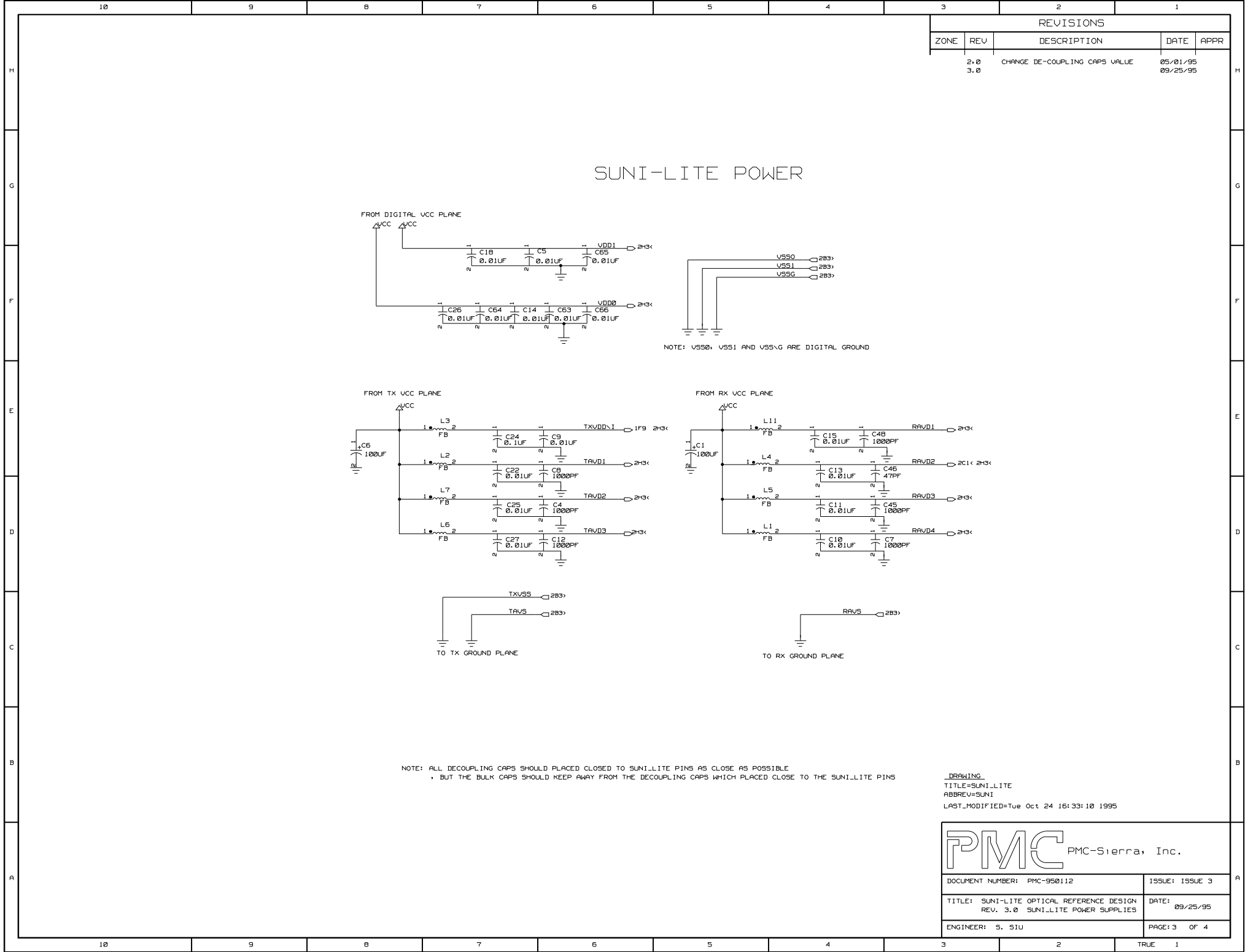


| REVISIONS |     |                              |          |      |
|-----------|-----|------------------------------|----------|------|
| ZONE      | REV | DESCRIPTION                  | DATE     | APPR |
| D9        | 2.0 | LOS LED DELETED              | 05/01/95 |      |
|           | 3.0 | REFER TO REWORK INSTRUCTIONS | 09/25/96 |      |

|                                                                    |                |
|--------------------------------------------------------------------|----------------|
| <b>PMc</b> PMc-Sierra, Inc.                                        |                |
| DOCUMENT NUMBER: PMC-950112                                        | ISSUE: ISSUE 1 |
| TITLE: SUNI-LITE OPTICAL REFERENCE DESIGN<br>REV. 3.0 ROOT DRAWING | DATE: 09/25/95 |
| ENGINEER: S. SIU                                                   | PAGE: 1 OF 4   |

DRAWING  
TITLE=950RD  
ABBREV=950RD  
LAST\_MODIFIED=Tue Oct 24 16:32:57 1995







## APPENDIX F: LAYOUT NOTES

### F.1. Background

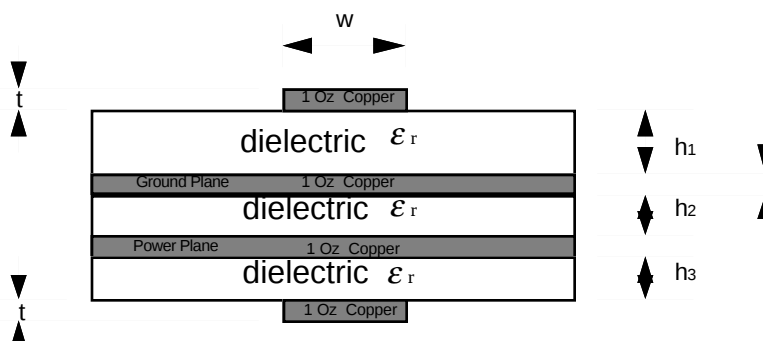
The SORD board is a 4-layer board that has both throughhole and surface mount components. Layer 1 and 4 are signal layers. Layer 2 and 3 are ground and power respectively.

### F.2. Trace Impedance Control

To reduce signal degradation due to reflection and radiation, the impedance of the traces that carry high speed signals such as transmitted and received data should be treated as microstrip transmission lines and terminated with matching impedance. The trace width is calculated using the formula

$$Z_o = \frac{87}{\sqrt{\epsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

based on the following layer setup:



where

$\epsilon_r$  = relative dielectric constant, nominally 5.0 for G - 10 fibre - glass epoxy

$t$  = thickness of the copper, fixed according to the weight of copper selected.

For 1 oz copper, the thickness is 1.4 mil. This thickness can be ignored if  $w$  is great enough.

$h_1, h_2, h_3$  = thickness of dielectric.

$w$  = width of copper

The parameters  $h_1$ ,  $h_2$ , and  $h_3$  can be specified. For example, if a 20 mil (including the copper thickness on both sides of the board) two layer core is selected, dielectric material that has the same relative dielectric constant can be added to both sides of the core to construct a 4 layer board.

Since all the controlled impedance traces are on the component side, only h1 is relevant in calculating the trace width. The calculation for the reference design is shown in the tables below:

| Parameters                              | Nominal                         |
|-----------------------------------------|---------------------------------|
| Board Thickness (mil)                   | 62 (including copper thickness) |
| Separation between layers 1 and 2 (mil) | 10                              |
| Separation between layers 2 and 3 (mil) | 30.5                            |
| Separation between layers 3 and 4 (mil) | 10                              |
| Relative dielectric constant            | 4.2                             |

| Parameter            | Data |
|----------------------|------|
| $\epsilon_r$         | 4.2  |
| h (mil)              | 10   |
| t (mil)              | 2.88 |
| Z <sub>0</sub> (Ohm) | 50   |
| W (mil)              | 17   |

Since h1 is proportional to the width of the traces, a small h1 will result in the traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication.

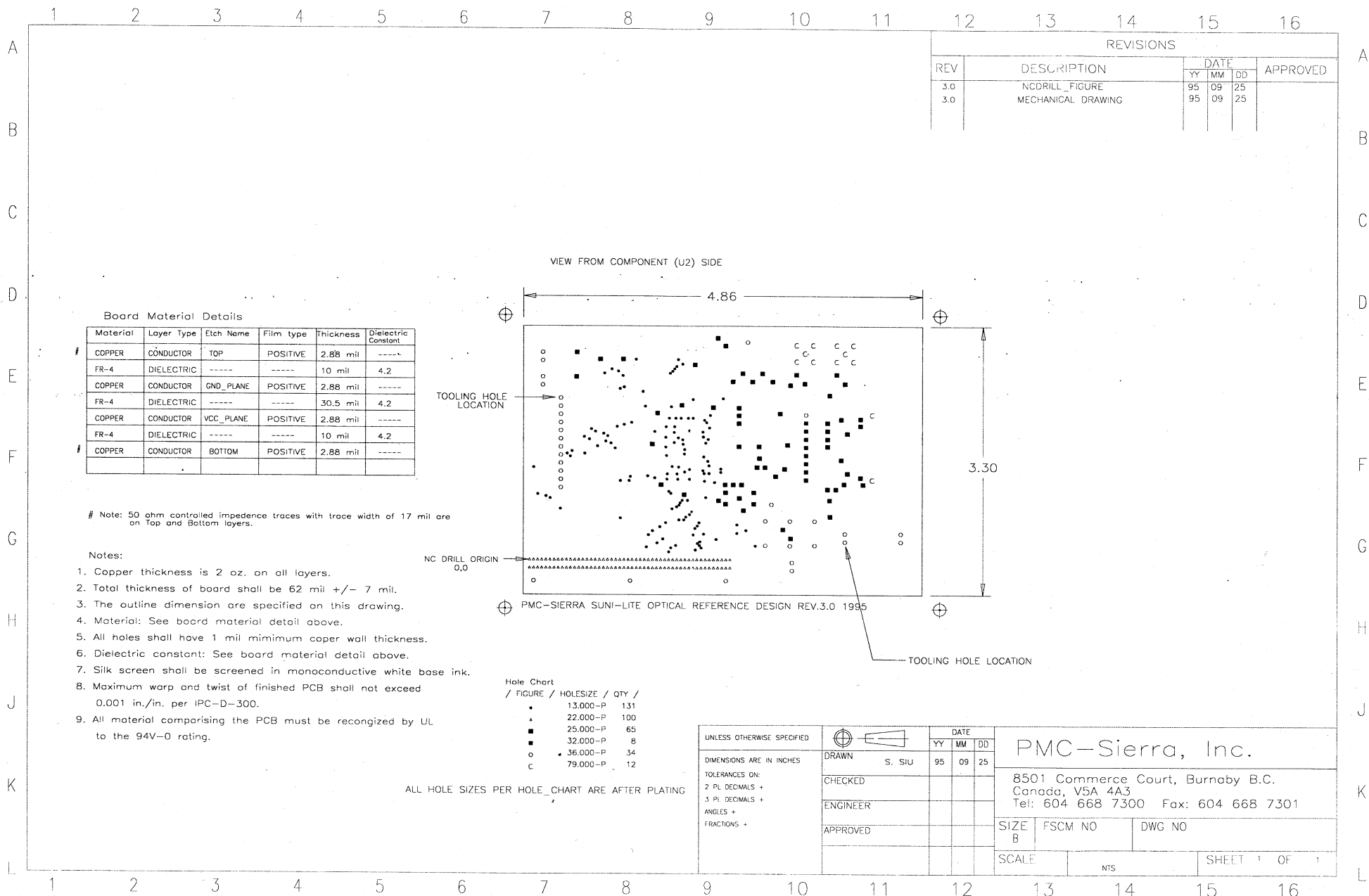
The low speed signals use 8 to 10 mil traces. Power and ground traces should be made as wide as possible to reduce the line inductance. All 50 Ohm traces are 17 mils wide.

**F.3. Routing**

Routing is based on the design considerations as well as manufacturability. Several suggestions are listed below:

- Turns and corners should be rounded to curves to avoid discontinuity in the signal path.
- Allow at least 10 mil clearance among vias, traces, and pads to prevent short and reduce crosstalk. If possible, allow 20 mil or more clearance around vias as manufacturers may have minimum clearance requirements. For the traces that run between pads of the 100 pin edge connector, clearance of 6 mil and trace width of 8 mil can be used. However, the number and lengths such traces should be kept to a minimum.
- The differential signal pairs should be of equal length so that both signals arrive at the inputs at the same time. They should also run parallel and close to one another for as long as possible so that noise will couple onto both lines and become common mode noise which is ignored by the differential inputs. Even though single ended inputs should not run parallel to one another in close proximity, all of the single ended signals that run parallel to one another on the dropside interface are low speed signals and are sampled after they have all settled down; therefore, they should not cause any concern.
- All power and ground traces should be made as wide as possible to provide low impedance paths for the supply current as well as to allow quick noise dissipation.
- The oscillator used is a 14 pin DIP package. The connections to the oscillator is setup so that an oscillator with a smaller footprint (8 pin) can also be plugged in.

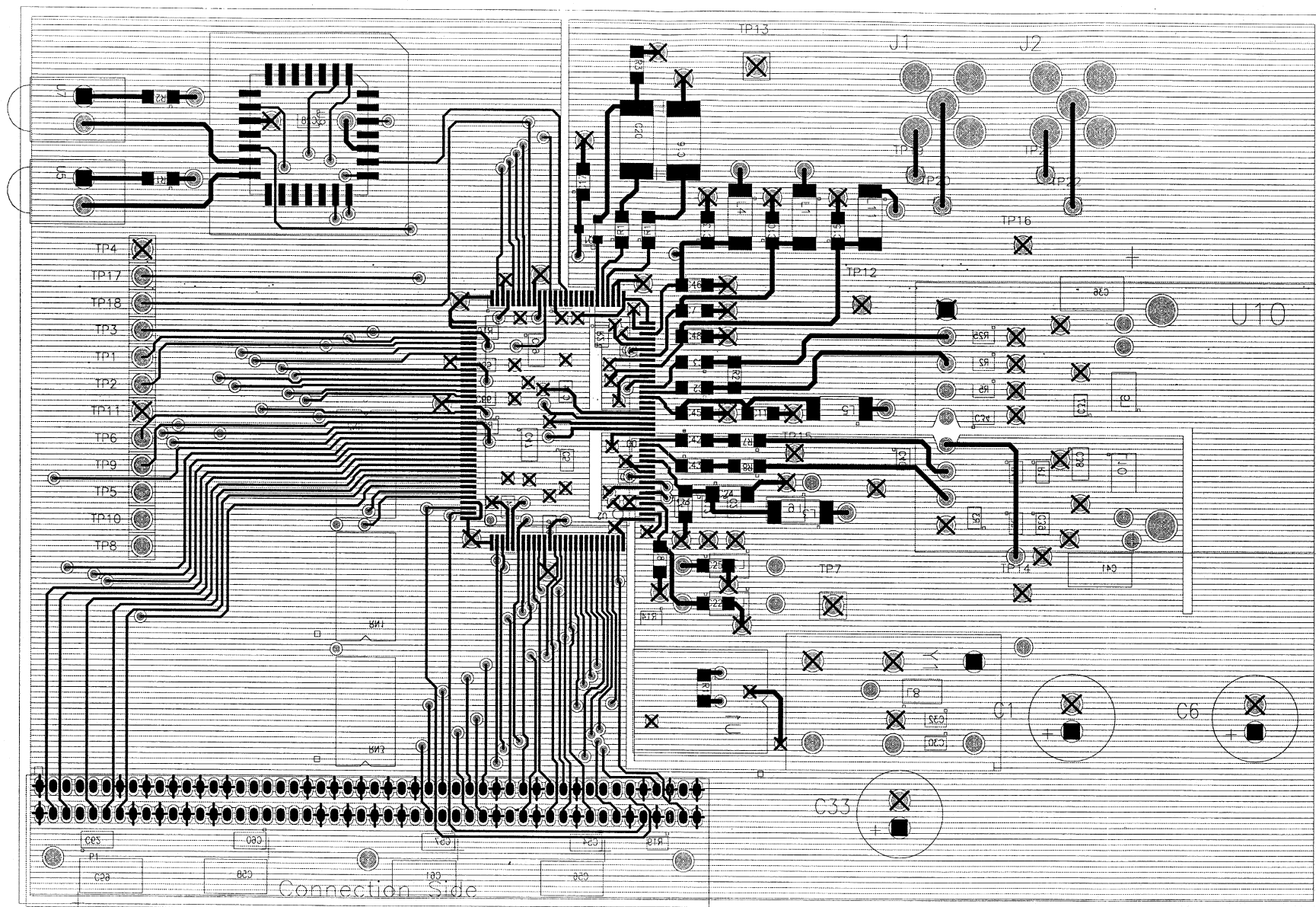
**APPENDIX G: LAYOUT**







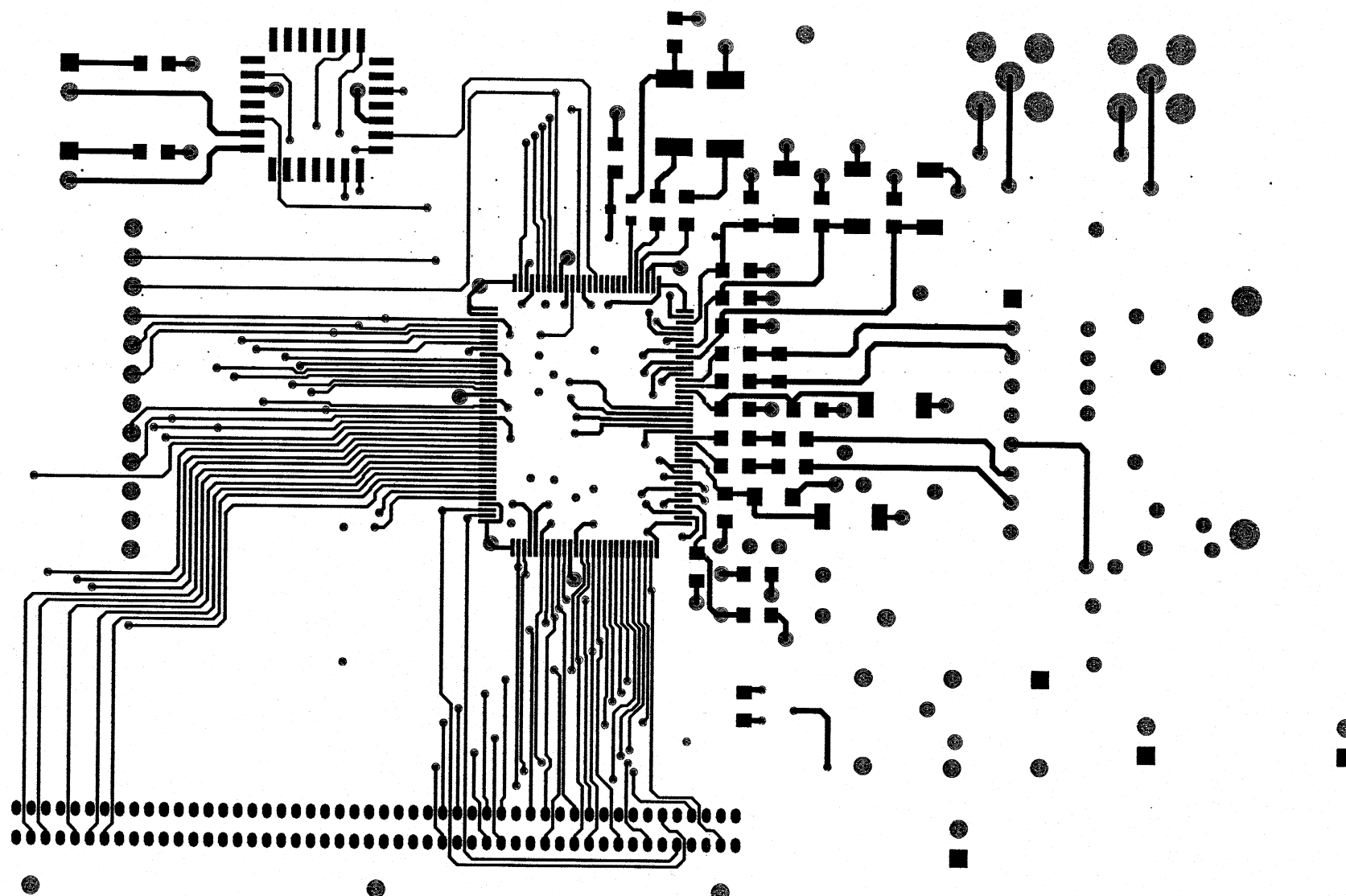
RESTORE3TOP3R TOP LAYER GND\_PLANE

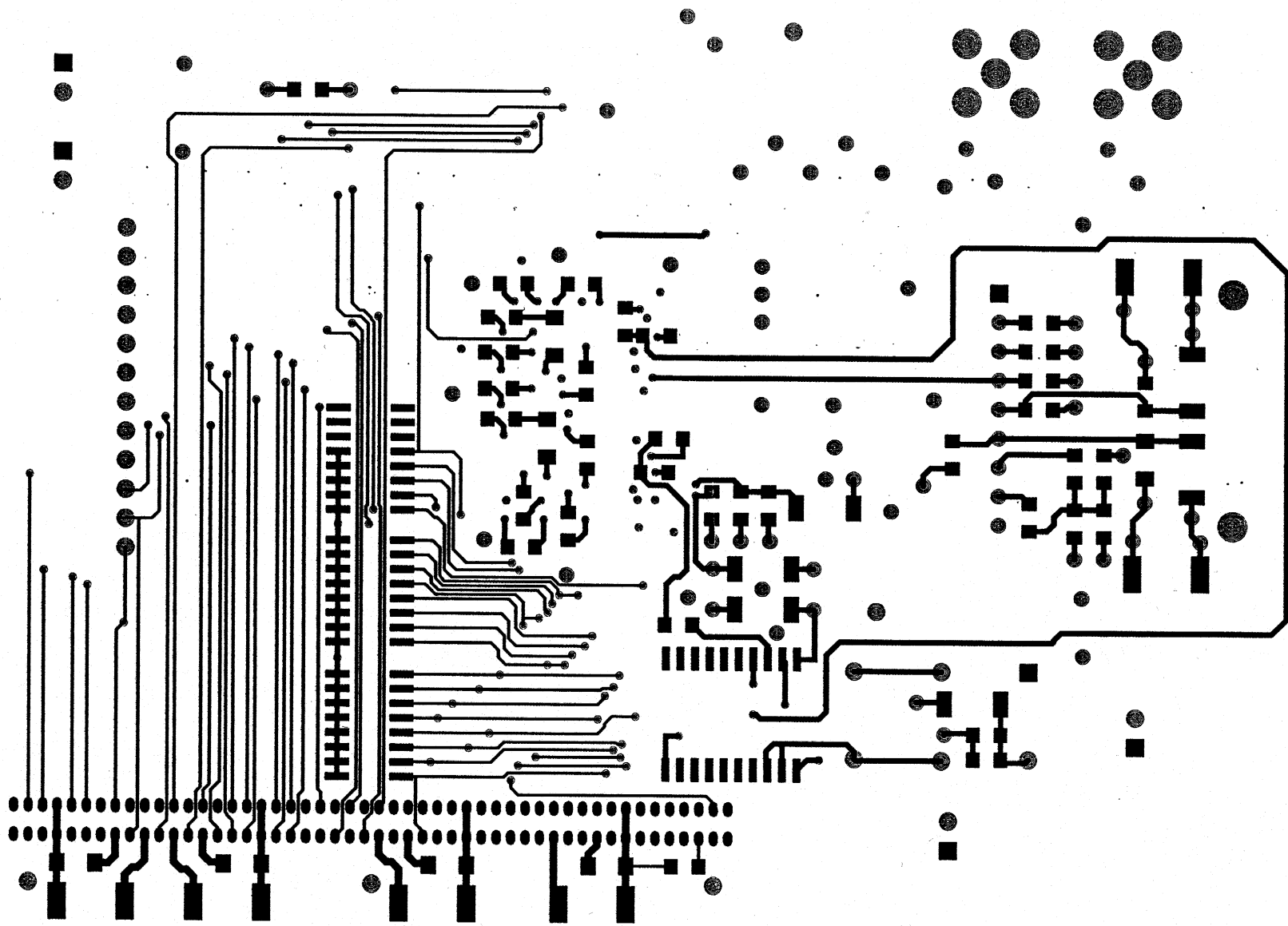


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TOP LAYER

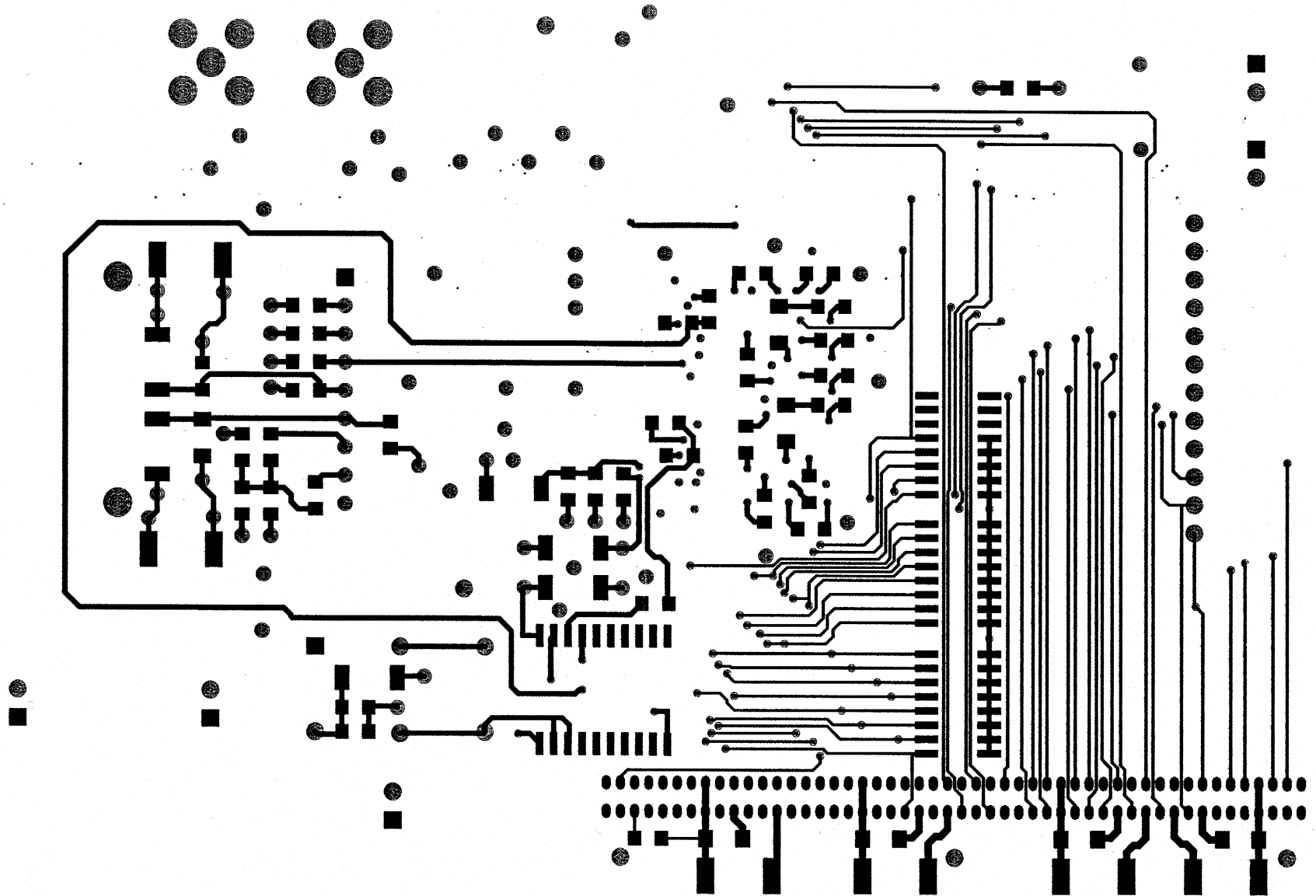




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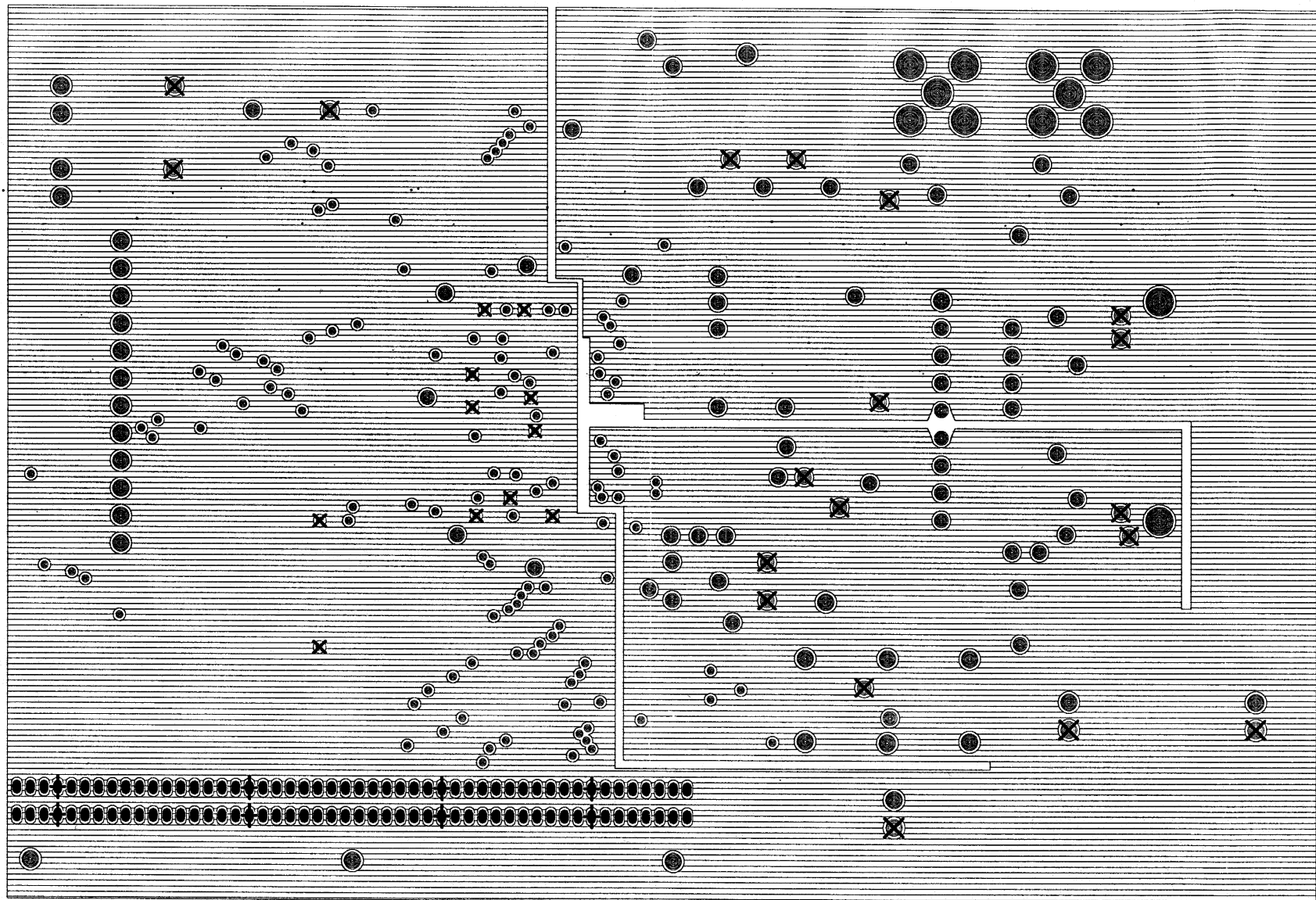
BOTTOM\_LAYER

BOTTOM\_LAYER



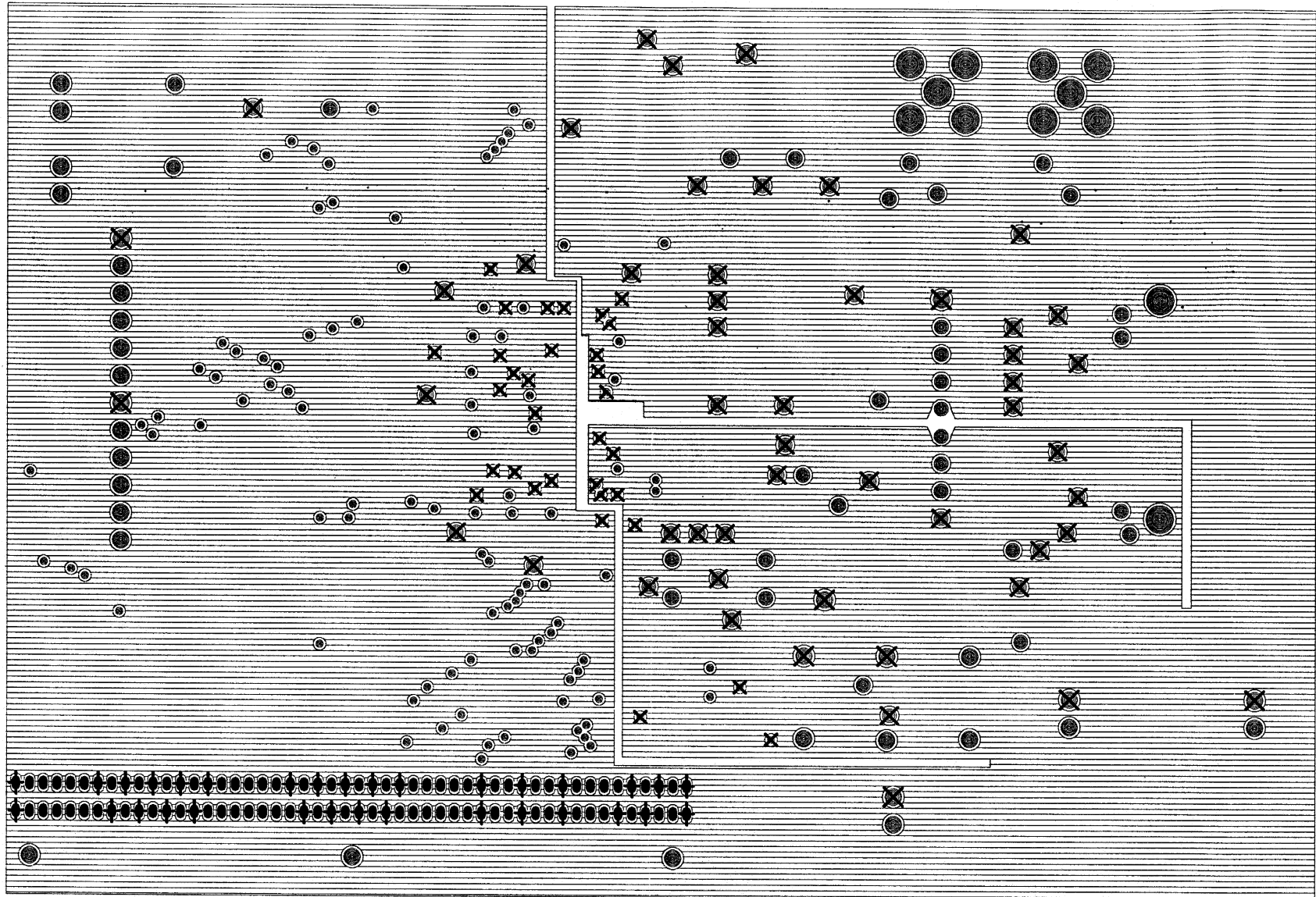
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VCC\_PLANE



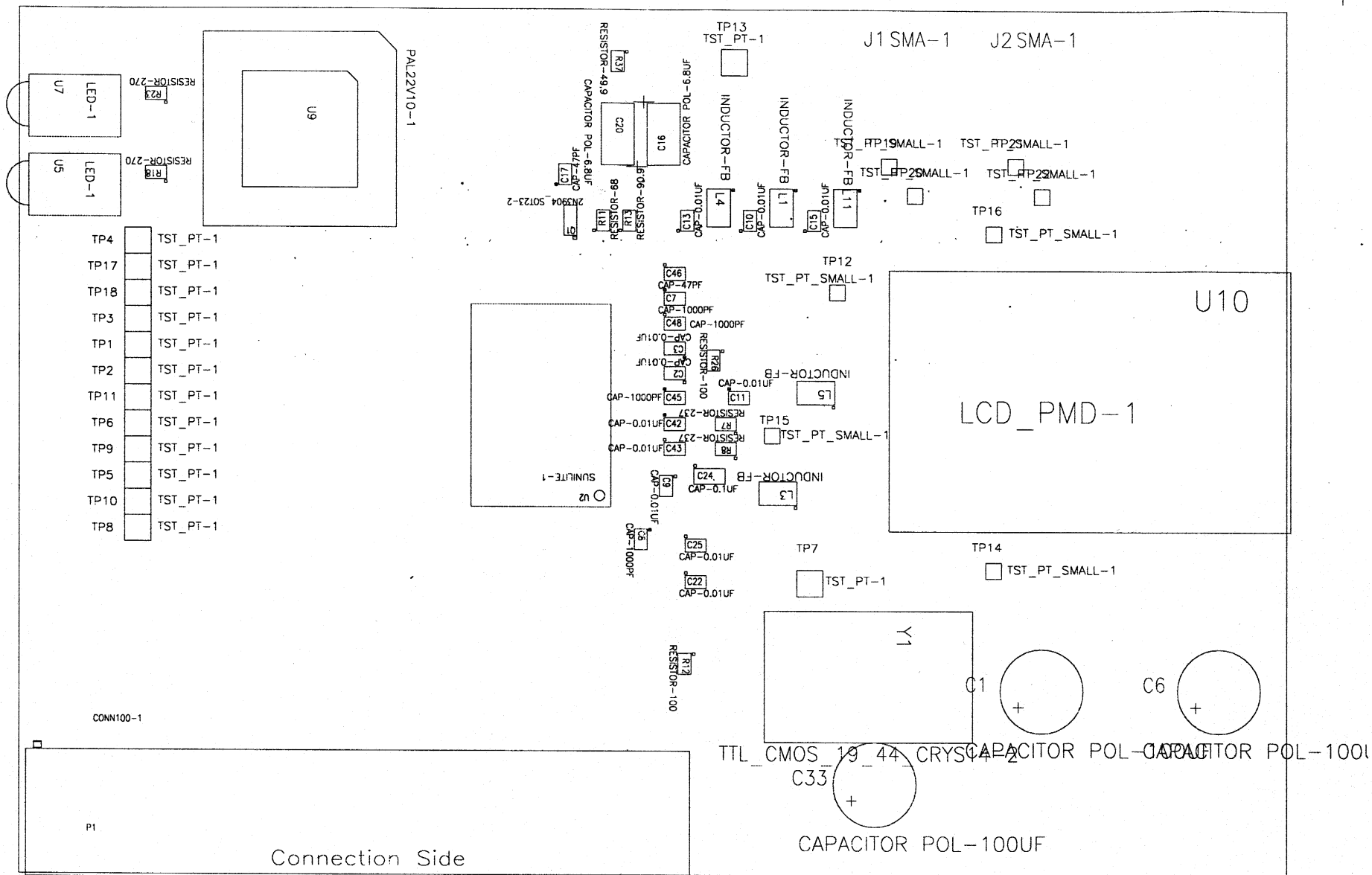
PMC-SIERRA SUNI-LITE OPTICAL REFERENCE DESIGN REV.3.0 1995

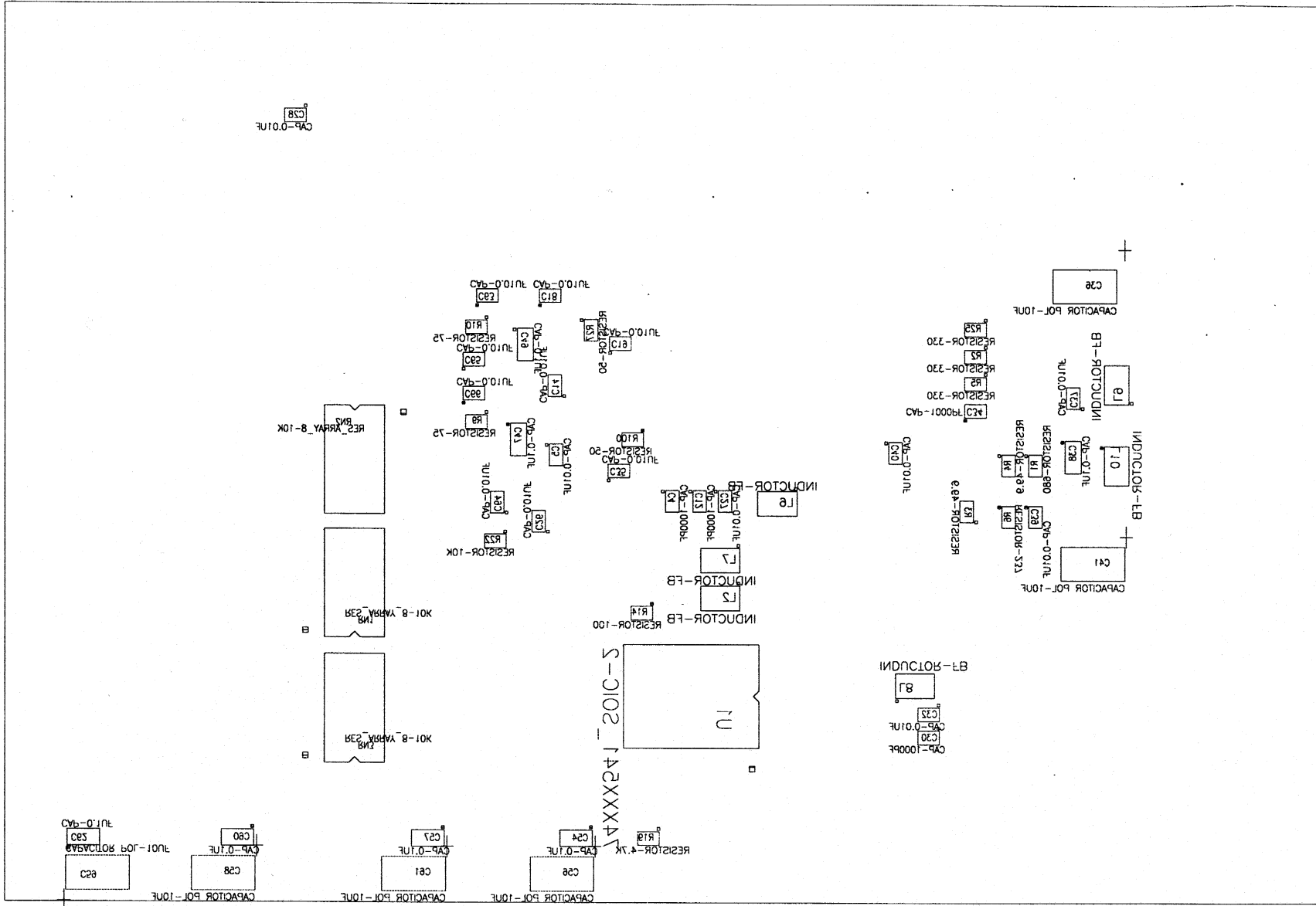
GND\_PLANE



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RES\_DES TOP



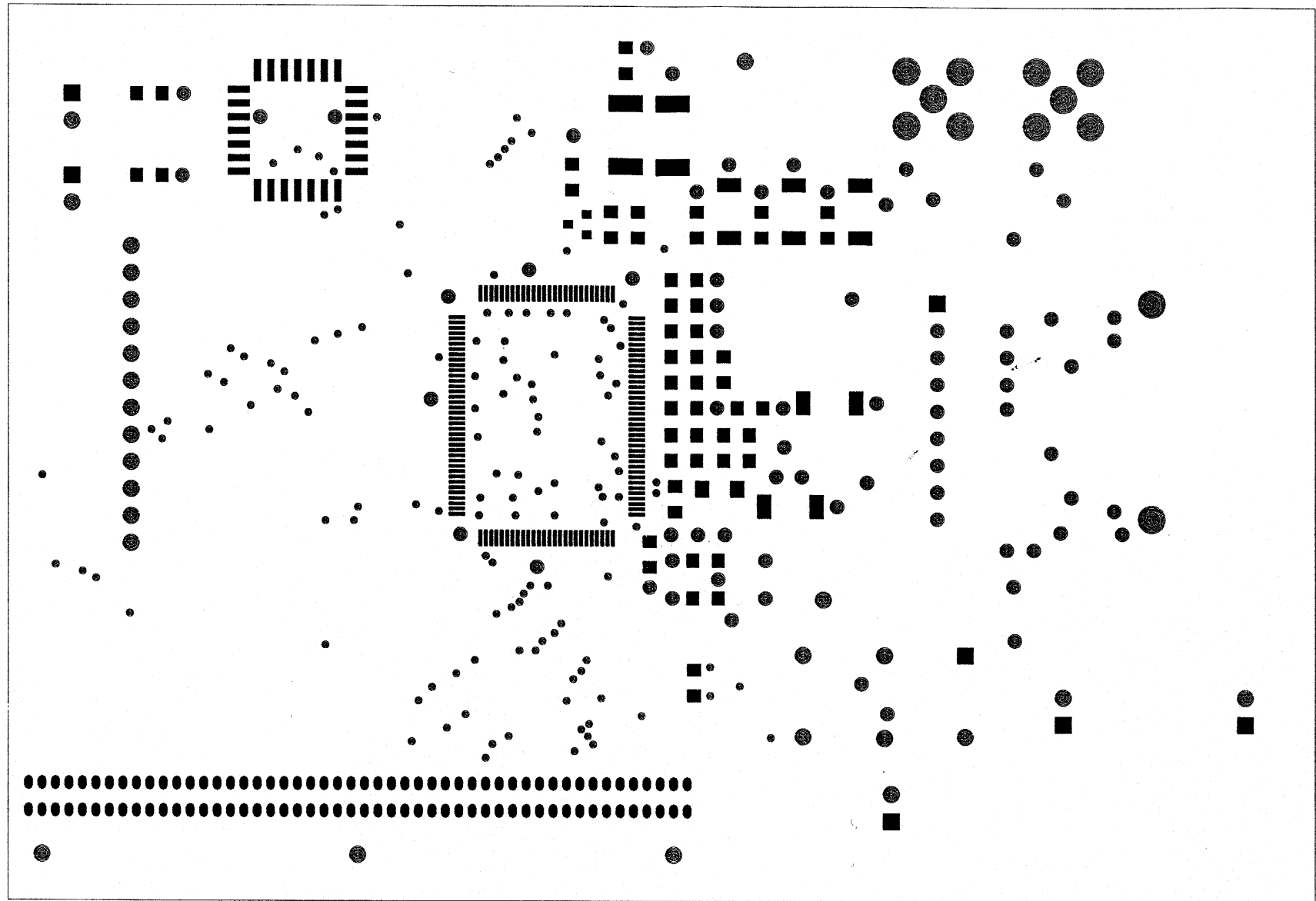




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SOLDER\_MASK TOP

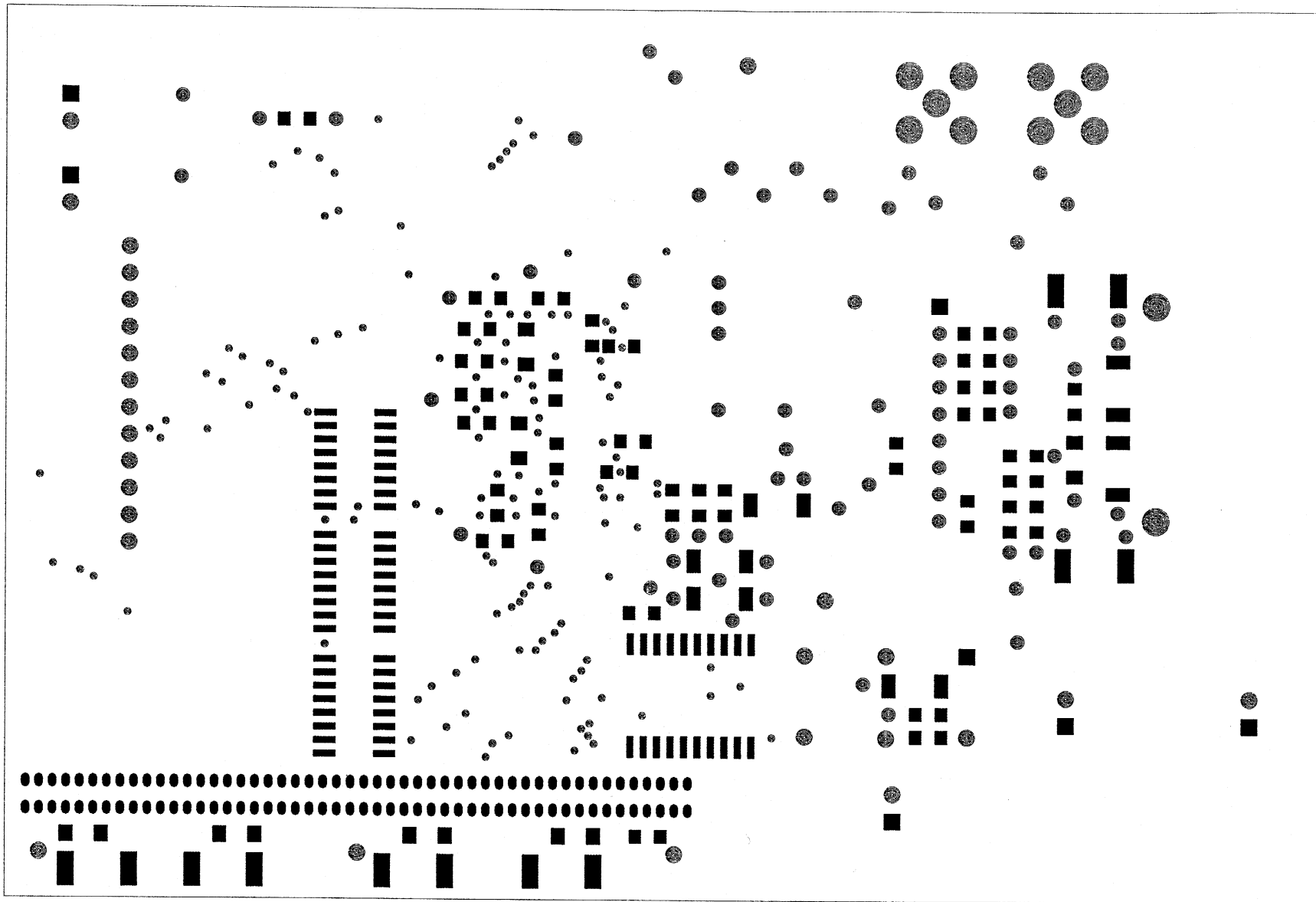


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SOLDER\_MASK BOTTOM



**APPENDIX H: REFERENCES**

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- Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", Second Edition, John Wiley & Sons.
- Montrose, Mark I., "Printed Circuit Board Design Techniques for EMC Compliance", IEEE Press, 1995.
- Graham, Martin and Johnson, Howard W., "High-Speed Digital Design: A Handbook of Black Magic", PRT Prentice-Hall Inc, 1993.

**NOTES**

Contact us for ATM support.

**Fax** (604)668-7301

**Phone** (604)668-7300

**Internet** apps@pmc-sierra.bc.ca

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