74LVC3G17

Triple non-inverting Schmitt trigger with 5 V tolerant input

Rev. 01 — 24 June 2004 Product data sheet

1. General description

The 74LVC3G17 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC3G17 provides three non-inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- SOT505 and SOT765 package
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

3. Applications

- Wave and pulse shapers for highly noisy environments.

PHILIPS

4. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay inputs nA to output nY	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ		-	5.6	-	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω		-	3.7	-	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω		-	3.8	-	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω		-	3.6	-	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω		-	2.7	-	ns
C_I	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V	[1] [2]	-	16.3	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[2] The condition is V_I = GND to V_{CC}.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC3G17DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3G17DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

6. Functional diagram

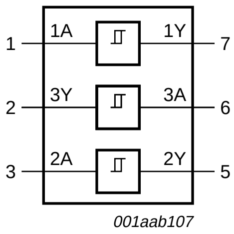


Fig 1. Logic symbol.

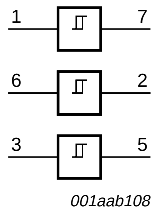


Fig 2. IEC logic symbol.

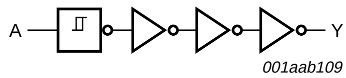


Fig 3. Logic diagram.

7. Pinning information

7.1 Pinning

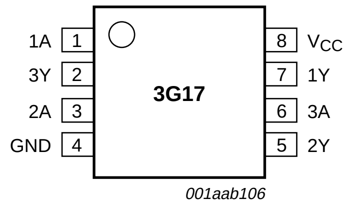


Fig 4. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1A	1	data input
3Y	2	data output
2A	3	data input
GND	4	ground (0 V)
2Y	5	data output
3A	6	data input
1Y	7	data output
V_{CC}	8	supply voltage

8. Functional description

8.1 Function table

Table 4: Function table [1]

Input	Output
nA	nY
L	L
H	H

[1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 5: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
V_O	output voltage	active mode	[1]	–0.5	V_{CC} + 0.5	V
		Power-down mode	[1] [2]	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C		-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	operating ambient temperature		–40	-	+125	°C

11. Static characteristics

Table 7: Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −100 μA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.3	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.8	-	-	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	±0.1	±5	μA
I_{off}	power off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +125 °C						
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V

Table 7: Static characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\ \mu A$; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	0.95	-	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.7	-	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	1.9	-	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.0	-	-	V
		$I_O = -32$ mA; $V_{CC} = 4.5$ V	3.4	-	-	V
I_{LI}	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 5.5$ V	-	-	±20	μA
I_{off}	power off leakage current	V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	-	±20	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	40	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V	-	-	5000	μA

[1] All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

12. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to +85 °C [1]						
t_{PHL}, t_{PLH}	propagation delay nA to nY	see Figure 5 and 6				
		$V_{CC} = 1.65$ V to 1.95 V	1.5	5.6	10.5	ns
		$V_{CC} = 2.3$ V to 2.7 V	1.0	3.7	6.5	ns
		$V_{CC} = 2.7$ V	1.0	3.8	6.5	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.0	3.6	5.7	ns
		$V_{CC} = 4.5$ V to 5.5 V	1.0	2.7	4.3	ns
C_{PD}	power dissipation capacitance per buffer	$V_{CC} = 3.3$ V [2] [3]	-	16.3	-	pF

Table 8: Dynamic characteristics *...continued*

GND = 0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay nA to nY	see Figure 5 and 6				
		V_{CC} = 1.65 V to 1.95 V	1.5	-	13.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	-	8.5	ns
		V_{CC} = 2.7 V	1.0	-	8.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	7.1	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	5.4	ns

[1] All typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

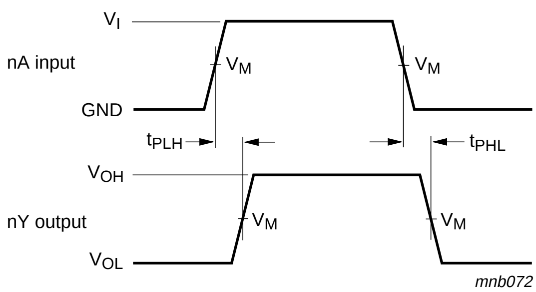
V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[3] The condition is V_I = GND to V_{CC}.

13. Waveforms



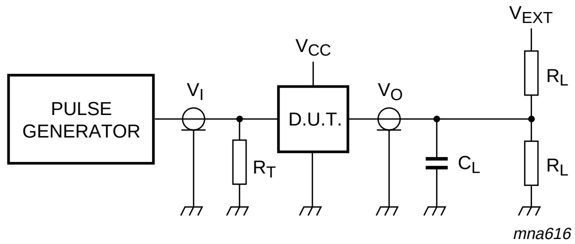
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 5. The input (nA) to output (nY) propagation delays.

Table 9: Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_M
1.65 V to 1.95 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	2.7 V	1.5 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V
4.5 V to 5.5 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}



Test data is given in Table 10.

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 6. Load circuitry for switching times.

Table 10: Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2 × V_{CC}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2 × V_{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}

14. Transfer characteristics

Table 11: Transfer characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
V_{T+}	positive-going threshold	see Figure 7 and 8				
		V_{CC} = 1.8 V	0.70	1.10	1.50	V
		V_{CC} = 2.3 V	1.00	1.40	1.80	V
		V_{CC} = 3.0 V	1.30	1.76	2.20	V
		V_{CC} = 4.5 V	1.90	2.47	3.10	V
		V_{CC} = 5.5 V	2.20	2.91	3.60	V
V_{T-}	negative-going threshold	see Figure 7 and 8				
		V_{CC} = 1.8 V	0.25	0.61	0.90	V
		V_{CC} = 2.3 V	0.40	0.80	1.15	V
		V_{CC} = 3.0 V	0.60	1.04	1.50	V
		V_{CC} = 4.5 V	1.00	1.55	2.00	V
		V_{CC} = 5.5 V	1.20	1.86	2.30	V

Table 11: Transfer characteristics *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_H	hysteresis ($V_{T+} - V_{T-}$)	see Figure 7, 8 and 9				
		V_{CC} = 1.8 V	0.15	0.49	1.00	V
		V_{CC} = 2.3 V	0.25	0.60	1.10	V
		V_{CC} = 3.0 V	0.40	0.73	1.20	V
		V_{CC} = 4.5 V	0.60	0.92	1.50	V
		V_{CC} = 5.5 V	0.70	1.02	1.70	V
T_{amb} = −40 °C to +125 °C						
V_{T+}	positive-going threshold	see Figure 7 and 8				
		V_{CC} = 1.8 V	0.70	-	1.70	V
		V_{CC} = 2.3 V	1.00	-	2.00	V
		V_{CC} = 3.0 V	1.30	-	2.40	V
		V_{CC} = 4.5 V	1.90	-	3.30	V
		V_{CC} = 5.5 V	2.20	-	3.80	V
V_{T-}	negative-going threshold	see Figure 7 and 8				
		V_{CC} = 1.8 V	0.25	-	1.10	V
		V_{CC} = 2.3 V	0.40	-	1.35	V
		V_{CC} = 3.0 V	0.60	-	1.70	V
		V_{CC} = 4.5 V	1.00	-	2.20	V
		V_{CC} = 5.5 V	1.20	-	2.50	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	see Figure 7, 8 and 9				
		V_{CC} = 1.8 V	0.15	-	1.20	V
		V_{CC} = 2.3 V	0.25	-	1.30	V
		V_{CC} = 3.0 V	0.40	-	1.40	V
		V_{CC} = 4.5 V	0.60	-	1.70	V
		V_{CC} = 5.5 V	0.70	-	1.90	V

[1] All typical values are measured at T_{amb} = 25 °C.

15. Waveforms transfer characteristics

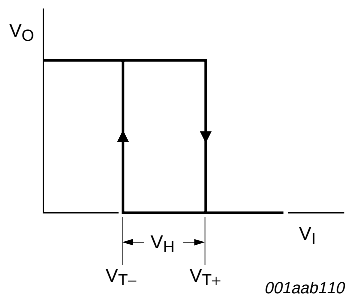


Fig 7. Transfer characteristic.

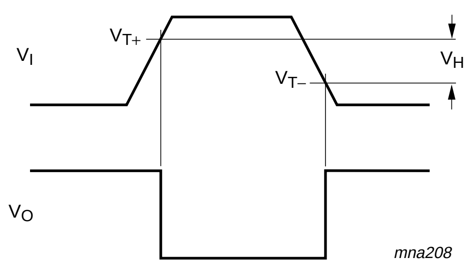
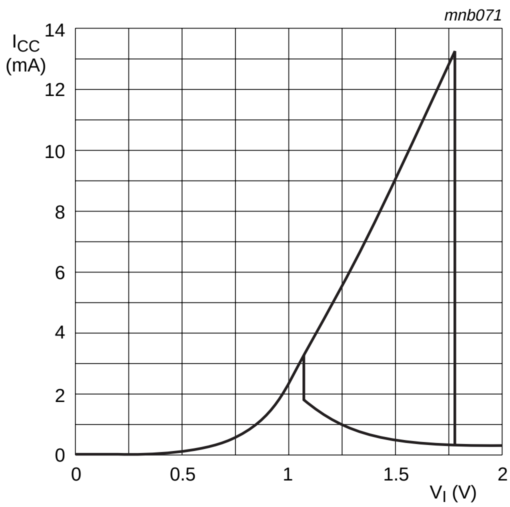


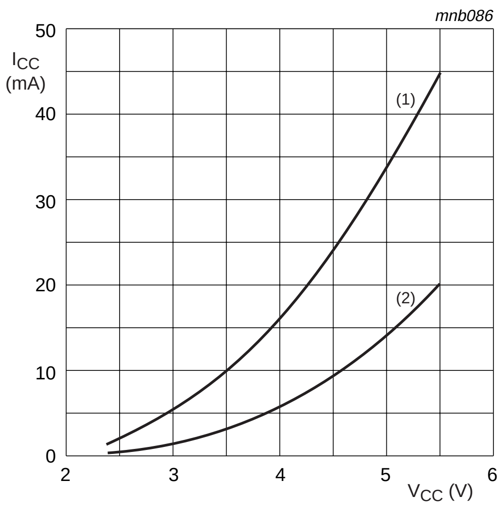
Fig 8. Definition of V_{T+}, V_{T-} and V_H.



V_{CC} = 3.0 V.

Fig 9. Typical 74LVC3G17 transfer characteristic.

16. Application information



Linear change of V_I between 0.8 V to 2.0 V.

(1) Positive-going edge.

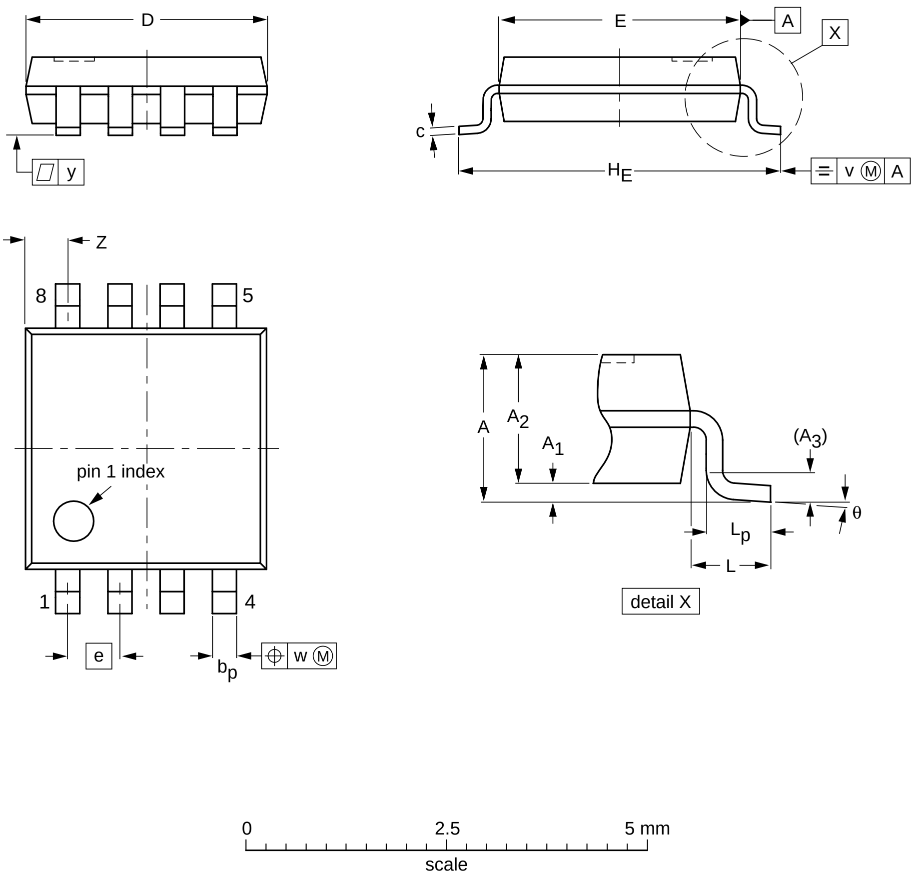
(2) Negative-going edge.

All values given are typical unless otherwise specified.

Fig 10. Average I_{CC} for 74LVC3G17 Schmitt trigger.

17. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

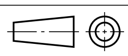
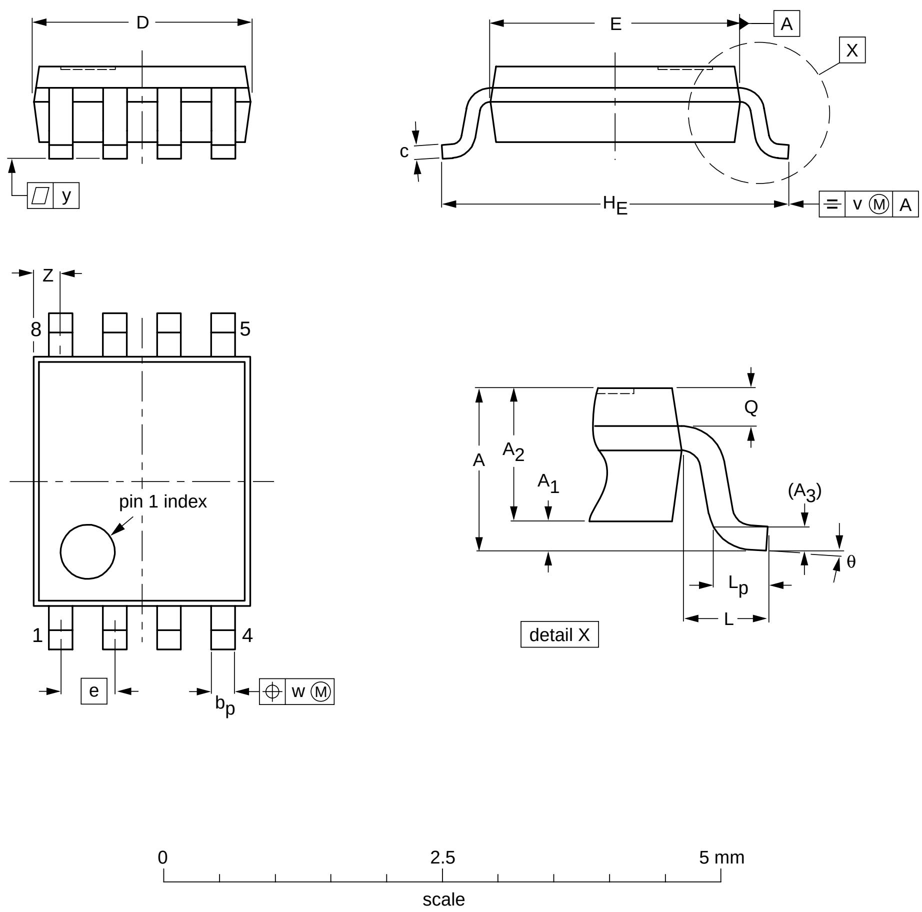
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 11. Package outline TSSOP8.

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 12. Package outline VSSOP8.

18. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LVC3G17_1	20040624	Product data	-	9397 750 13332	-

19. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

20. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For additional information, please visit: **http://www.semiconductors.philips.com**

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23. Contents

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