TDK SEMICONDUCTOR CORP.

73S1121F
EMV Smart-Card Terminal Controller
With Built-in Dual ISO-7816 Interface and USB

DATA-SHEET

April 2004

DESCRIPTION

The TDK Semiconductor Corporation 73S1121F is a CMOS single chip dual ISO-7816 smart-card terminal micro-controller that implements all the functions required to build a low-cost dual smart-card terminal with a USB interface, suitable for various applications including EMVco compliant payment terminals. Its enhanced set of features supports several configurations allowing low component count and a fast design cycle. Based on an 80C52 core, it incorporates communication and man-machine interfaces. The TDK 73S1121F device is applicable to either portable or host-connected applications. Embedded Flash memory makes the TDK 73S1121F a complete system-on-chip suitable for both development and production phases.

This data-sheet presents the package and pin description, as well as the electrical features that are unique to the TDK 73S1121F. It also presents a brief description of the architecture and of its embedded functions.
Refer to the 73S11xxF Hardware User's Guide for more detailed information about the microcontroller architecture, description of the registers, description of the different blocks that are common to the TDK 73S11xxF smart card terminal controller family.

Also refer to the TDK 73S11xxF Software User's Guide for a complete description of the Application Programming Interface (API).

APPLICATIONS

- **PIN-pads Smart Card Readers**
- **Computer-connected Terminal for:**
  - → **PATM**
  - → **E-commerce**
  - → **Home-Banking**
  - → **E-purse**
  - → **Logical Access**
- **Point of Sales & Transaction Terminals**
- **Standalone or connected Applications**
- **General Purpose Smart Card readers**

ADVANTAGES

- **True System-on-Chip solution, with built-in communication interfaces and peripherals**
- **Compact solution, that requires only a few external components**
- **Embedded 64kB Flash and 5kB RAM are the largest memory size among 8-bit smart card reader controllers in the industry**
- **Low-cost solution for portable and host-connected terminals**
- **Software API (Application Programming Interface) includes the ready-to-use protocol layers for asynchronous cards and USB**
  - → **Faster development time**
  - → **Time-to-Market**

FEATURES

80C52 core:

- 12 clock-cycle / instruction
- CPU clocked up to 24MHz (with a 12MHz crystal)
- 16-bit PC (64kB program linear memory address space)

Memory:

- 64kB internal Flash (Program Memory)
- 128 Bytes Flash Info Memory Block
- Flash memory guaranteed for 10,000 erase-write cycles
- 1kB IRAM (internal RAM for registers) + 4kB internal XRAM (User Data Memory)
- Interface for external program / data memory
- Boot-ROM loader program allows both In-System-Programming and In-Application-Programming of the embedded flash (ISP and IAP modes)
- Flash PROM-programming mode
- ISP, PROM programming modes and external memory interface can be permanently disabled by protection fuses

Oscillators:

- Single low-cost 12MHz crystal
- Optional low-cost 32kHz crystal (with internal counter for RTC support)
- An Internal PLL provides all the necessary clocks to each block of the system

Interrupts:

- Standard 80C52 2-priority level structure
- 8 different sources of interrupt

Power Down Modes:

- 2 standard 80C52 Power Down and IDLE modes
- 1 low-speed mode (CPU run at 32kHz)

Timers:

- (3) Standard 80C52 timers T0, T1 and T2
- (1) 16-bit timer that can generate RTC interrupts from the 32KHz oscillator

(2) Built-in ISO-7816 card interfaces:

- (2) Independent step-up converters generate VCC for the card (3V or 5V)
- Compliant with EMV 4.0 (EMV2000)
- Activation/Deactivation sequencers
- Auxiliary I/O lines (C4-C8 signals)
- 6kV ESD protection on all interface pins

Communication with smart cards:

- ISO-7816 UART 9600 to 115kbps (with 12MHz crystal) for protocols T=0, T=1
- 2-Byte FIFO for transmit and receive
- Hardware support to manage additional external card interfaces

Communication interfaces:

- Full-duplex serial interface (1200 to 115kbps UART)
- USB 1.1 Full Speed 12Mbps Interface (backward compatible with USB 2.0), PC/SC compliant with 4 Endpoints:
  - Control (16B FIFO)
  - Interrupt IN (32B FIFO)
  - Bulk IN (128B FIFO)
  - Bulk OUT (128B FIFO)

Man-Machine Interface and I/Os:

- 5x6 Keyboard (hardware scanning, debouching and scrambling)
- (7) Dedicated LCD I/Os (Control of any external HD44780 standard LCD driver) – Can be also used as standard I/Os
- (8) User I/Os
- (4) GPIOs (with separate voltage reference input)

Voltage Detection:

- (3) Analog Inputs (Voltage detection range: 0.2V to 2.5V)
- (1) 2.5V Voltage reference available on an output pin.

Operating Voltage:

- 2.7V to 3.6V (3V to 3.6V when USB is in use)

Operating Temperature:

- 0°C to 85°C

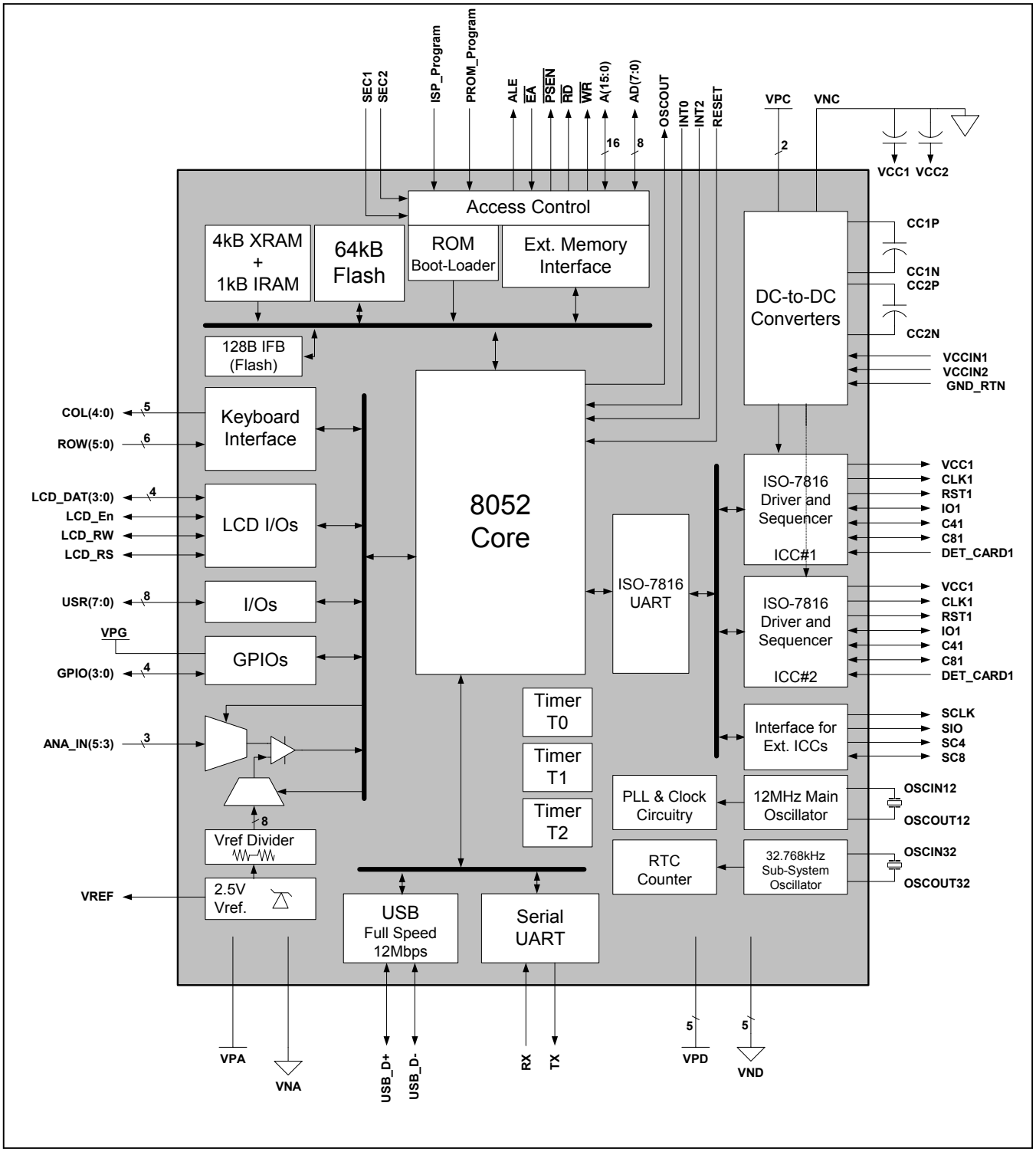
Package:

- 128 pin TQFP
- Bare Die

Software:

- Two-level Application Programming Interface (ANSI C-language libraries)
- USB and T=0 T=1 smart card protocol layers
- PIN Management functions compatible with CCID requirements

FUNCTIONAL DIAGRAM



Microcontroller

The 73S1121F core is an 8-bit 80C52 micro-controller, with embedded 5kB of RAM (data memory) and 64kB of flash (program memory). An additional Information Block Flash cell (128B IFB) is available for storage of device ID, serial number, firmware version etc

An embedded ROM boot-loader allows downloading of the flash memory (either program or IFB) through the serial port. This programming mode can be forced externally (In-System-Programming = ISP mode) or also can be called by the application (In-Application-Programming = IAP mode) through the Application Programming Interface. The 73S1121F flash memory can also be programmed with a parallel PROM programmer. An interface for external memory is provided to allow extension of the RAM up to 64kB total (addition of 59kB external). Extension of the total program memory above the 64kB can be implemented by adding bank-switched external memory pages, the firmware being responsible for management of the banks. Security fuses allows the user to permanently disable, either the ISP mode, the PROM programming mode, the interface for external memory, or any combination of the 3. It allows the 73S1121F, once programmed with an application, to run independently without possibility from the external world to access the internal memory, or to re-download a non-authorized application, or to run an external program.

The 73S1121F has a main oscillator that requires a 12MHz crystal. Internal clock circuitry generates clock signals to the different blocks and to the CPU (that can be clocked at 6, 12 or 24MHz). An optional 2nd crystal (32,768Hz) can be connected to a sub-system oscillator. It is associated with a 16-bit counter that can generate real-time interrupts to the core, every 0.5s, 1s or 2s. The firmware application is then responsible to service this interrupt and to update a real time/date counter for applications that require it. This sub-system clock can also be used as a CPU clock for low-speed operation as an additional power saving mode. Keypad scanning can also operate from a 1kHz clock generated from the sub-system clock.

The 73S1121F has the standard 8052 2-priority level interrupt structure, with 8 different interrupt sources: 2 external interrupts (pins INT2 and INT0), 3 timer interrupts, 1 serial/USB interrupt, 1 smart-card interrupt and a shared interrupt (keypad, GPIO, RTC counter and analog comparator inputs).

The 73S1121F incorporates 3 timers, T0, T1 and T2 that can be clocked internally or externally by the respective input signals on the pins USR0, USR1 and USR2.

Standard 8052 Power Down mode and IDLE mode are supported for power saving modes. The clock for each block, as well as the analog circuitry (analog input, voltage reference and USB transceiver) and the DC-to-DC converters (VCC generators for the card) can be independently enabled or disabled by firmware to optimize power consumption.

Management of the embedded card interfaces, peripherals and communication capabilities are controlled by means of dedicated registers in RAM. Management of the interrupts, of the power saving modes and of the clock circuitry is also controlled through registers.

ISO-7816 Interfaces and UART

The feature set of the TDK 73S1121F includes two built-in smart-card interfaces, controlled by an ISO-7816 compliant sequencer. Each built-in smart card interface has its own DC-DC converter, able to generate the card power supply, VCC=3V or 5V. The sequencer handles the activation / deactivation of the card signals. Each card interface includes an input for the card presence switch (programmable polarity) and auxiliary I/O lines for C4 / C8 signals. A hardware ISO-7816 UART with a dedicated FIFO allows easy implementation of asynchronous card protocols T=0 and T=1. This UART can be bypassed to allow a firmware UART to handle other protocols such as synchronous card protocols. Control and use of the ISO-7816 UART is widely and easily configurable with dedicated registers located in XRAM. A 4-line interface enables the 73S1121F to control additional external smart card (ICC) interfaces, typically for multiple-SAM configurations. The ISO-7816 UART can be shared between all the smart card interfaces (internal and external).

Communication, Man-Machine Interface and I/Os

The 73S1121F has a full-speed (12Mbps) USB slave interface with 4 endpoints for implementation of computer-connected terminals. A standard 8052 serial UART allows the 73S1121F to communicate with any host or peripheral on a serial link, at a data transmission rate from 1200 to 115kbps. Communication with a computer through RS232 can be easily implemented only using an external level shifter.
Keyboard implementation is supported with a built-in 5x6 keyboard interface with hardware scanning and debouching. It also features a scrambling capability (change of the scanning order).
7 I/O lines are dedicated to control an external standard LCD driver, allowing a wide choice of LCDs to be controlled by the 73S1121F, such as 7-wire, Hitachi-type HD44780.
Additional input/outputs feature 8 user I/Os, 4 general purpose I/Os (GPIOs, that are compatible with any interfacing voltage up to 5.5V), and 3 analog inputs for voltage detection (for battery monitoring or any DC voltage comparison). Each of the analog inputs can be multiplexed to a comparator pre-set to a threshold voltage adjustable between 0.2V to 2.5V (8 possible levels).

PIN DESCRIPTION

Pin Name	Pin Number 128 TQFP	Total Pins	Type	Description
CC1P	111	1	I/O	Card interface 1 - Charge-pump capacitor positive node (0.68μF Low ESR <100mΩ)
CC1N	109	1	I/O	Charge-pump capacitor 1 Negative Node
CC2P	103	1	I/O	Card interface 2 - Charge-pump capacitor positive node (0.68μF Low ESR <100mΩ)
CC2N	105	1	I/O	Charge-pump capacitor 2 Negative Node
COL (4)	32	5	O	Keypad column drive lines
COL (3)	33			
COL (2)	35			
COL (1)	36			
COL (0)	39			
ROW (5)	24	6	I	Keypad row sense lines
ROW (4)	25			
ROW (3)	27			
ROW (2)	28			
ROW (1)	29			
ROW (0)	30			
TXD	26	1	O	Transmit data - Serial output port from the 73S1121F serial UART
RXD	31	1	I	Receive data - Serial input port to the 73S1121F serial UART
USR (7)	50	8	I/O	User programmable I/O port.
USR (6)	53			
USR (5)	56			
USR (4)	59			
USR (3)	63			
USR (2)	68			
USR (1)	72			
USR (0)	77			
INT2	34	1	I	External interrupt input pin
INT0	118	1	I	External interrupt input pin
USB_D-	124	1	I/O	USB D-
USB_D+	125	1	I/O	USB D+
GPIO (3)	94	4	I/O	General purpose I/O with separate power supply
GPIO (2)	93			
GPIO (1)	92			
GPIO (0)	91			

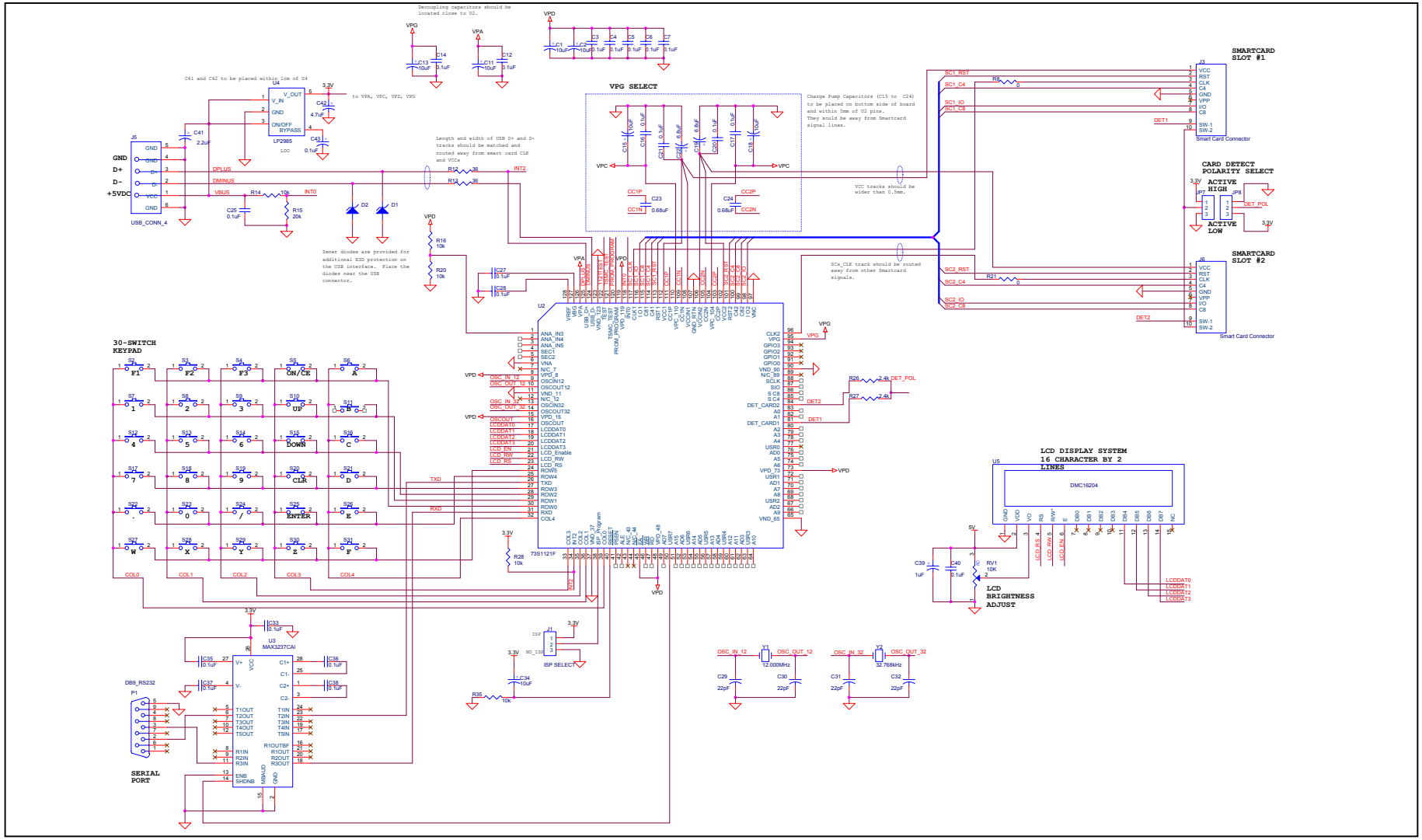
Pin Name	Pin Number 128 TQFP	Total Pins	Type	Description
LCDDAT (3)	20	4	I/O	LCD driver dedicated I/O lines - Data pins. Can be used as standard I/Os
LCDDAT (2)	19			
LCDDAT (1)	18			
LCDDAT (0)	17			
LCD_Enable (LCDDAT (4))	21	1	I/O	LCD driver dedicated I/O line: LCD Enable. Can be used as standard I/O
LCD_RW (LCDDAT (5))	22	1	I/O	LCD driver dedicated I/O line: LCD Read/Write. Can be used as standard I/O
LCD_RS (LCDDAT (6))	23	1	I/O	LCD driver dedicated I/O line: LCD Register Select. Can be used as standard I/O
ANA_IN (5)	3	3	I	Analog Inputs - (Voltage detection inputs 0.2V to 2.5V ±3%)
ANA_IN (4)	2			
ANA_IN (3)	1			
VREF	128	1	O	Voltage reference. 2.5V ± 7%. Decouple with 0.1μF capacitor to VNA.
VBG	127	1	O	Bandgap output - internal use. To be decoupled with 0.1μF capacitor to VNA. Nothing else should be connected to VBG
RESET	40	1	I	73S1121F Reset. Active high
ISP_Program	38	1	I	Forces internal Flash programming in ISP mode at reset. Active High. Inactive Low, suitable for normal operation. Internal pull-down allows NC for normal operation
N/C	7; 12; 43; 44; 89;	5	-	Not Connected
Reserved	121; 122	2	-	To be connected to VND
PROM_Program	120	1	I	Forces internal Flash programming in PROM parallel mode at reset. Active High. Internal pull-down allows NC for normal operation
SEC1	4	2	I	Digital security inputs that control the internal protection fuses. Active High. Internal pull-down allows NC for normal operation 00 – Inactive. 01- Permanently deactivates both PROM programming mode, TDK testing modes. 10 – Permanently deactivates the external interface of address and data signals to the processor 11- Permanently deactivates the ISP programming mode. Any combination of the 3 protection modes can be achieved by applying the proper sequence on these pins
SEC2	5			

Pin Name	Pin Number 128 TQFP	Total Pins	Type	Description
VND	11; 37; 65; 90; 123	5	GND	Digital ground
VPD	8; 15; 48; 73; 119	5	Supply	Digital power supply. 2.7V - 3.6V Must be at least equal to 3V when using the USB interface. Each pin to be decoupled to VND with a 0.1μF capacitor.
VNA	6	1	GND	Analog ground
VPA	126	1	Supply	Analog power supply. 2.7V - 3.6V To be decoupled to VNA with a 0.1μF capacitor.
VPG	95	1	Supply	GPIO power supply: 2.7V - 5.5V. Only connect if GPIO used. VPG is the reference voltage for interfacing GPIOs with external devices operating on a voltage different than VPD.
VPC	104; 110	2	Supply	DC/DC Step-up Converter power supply (2.7 - 3.6V). Each pin to be decoupled to VNC with one 0.1μF and one 10μFcapacitor.
VNC	97	1	GND	DC/DC Step-up Converter ground
OSCIN32	13	1	I	32.768KHz crystal input. Can drive clock in and leave OSCOUT32 unconnected
OSCOUT32	14	1	O	32.768KHz crystal output. Leave unconnected if not using a crystal
OSCIN12	9	1	I	12MHz crystal input. Can drive clock in and leave OSCOUT12 unconnected
OSCOUT12	10	1	O	12MHz crystal output. Leave unconnected if not using a crystal
OSCOUT	16	1	O	CPU clock output pin

Pin Name	Pin Number 128 TQFP	Total Pins	Type	Description
ALE	42	1	O	Address latch enable. A pulse for latching the low byte of the address on the AD pins during access to external memory. ALE is internally used to demultiplex the low address byte A(7:0)
$\overline{\text{PSEN}}$	41	1	O	Program store enable. This output goes low during a fetch from program external memory. Active low
$\overline{\text{EA}}$	45	1	I	External Access enable. When this pin is low, the core fetches code from external program memory only
$\overline{\text{RD}}$	47	1	I/O	Read. A strobe, active during an external read. To be used as a read enable for external data memory devices. Active low.
$\overline{\text{WR}}$	46	1	I/O	Write. A strobe, active during an external write. To be used as a read enable for external data memory devices. Active low
AD(7)	49	8	I/O	Multiplexed Low-byte Address bus / 8-bit Data BUS. Address/Data. The low byte of the address and the data byte time multiplexed during external memory accesses. There is no need to use this bus to extract the low-address byte, since it is already demultiplexed and available on the pins A7:0
AD(6)	52			
AD(5)	55			
AD(4)	58			
AD(3)	62			
AD(2)	67			
AD(1)	71			
AD(0)	76			
A(15)	51	16	O	Address pins; address during external memory accesses. A(7:0) are generated internally by demultiplexing of AD(7:0) with ALE
A(14)	54			
A(13)	57			
A(12)	60			
A(11)	61			
A(10)	64			
A(9)	66			
A(8)	69			
A(7)	70			
A(6)	74			
A(5)	75			
A(4)	78			
A(3)	79			
A(2)	80			
A(1)	82			
A(0)	83			

Pin Name	Pin Number 128 TQFP	Total Pins	Type	Description
CLK1	117	1	O	Card interface 1 - Clock signal
IO1	116	1	I/O	Card interface 1 - I/O signal
RST1	113	1	O	Card interface 1 - RST signal
VCC1	112	1	O	Card interface 1 - VCC signal Must be decoupled to GND with a 6.8μF low-ESR capacitor
VCCIN1	108	1		Card interface 1 – voltage supply for interface circuits – take from VCC1 filter capacitor
C41	114	1	I/O	Card interface 1 - Auxiliary I/O signal (card C4 signal)
C81	115	1	I/O	Card interface 1 - Auxiliary I/O signal (card C8 signal)
CLK2	96	1	O	Card interface 2 - Clock signal
IO2	98	1	I/O	Card interface 2 - I/O signal
RST2	101	1	O	Card interface 2 - RST signal
VCC2	102	1	O	Card interface 2 - VCC signal Must be decoupled to GND with a 6.8μF low-ESR capacitor
VCCIN2	106	1		Card interface 2 - voltage supply for interface circuits – take from VCC2 filter capacitor
GND_RTN	107	1		Ground connection for SC power converters
C42	100	1	I/O	Card interface 2 – Auxiliary I/O signal (card C4 signal)
C82	99	1	I/O	Card interface 2 – Auxiliary I/O signal (card C8 signal)
DET_CARD1	81	1	I	Card interface 1 - Presence contact input pin. Programmable polarity (to be connected according to the card presence switch with a pull-up / pull-down)
DET_CARD2	84	1	I	Card interface 2 - Presence contact input pin. Programmable polarity (to be connected according to the card presence switch with a pull-up / pull-down)
SIO	87	1	I/O	Digital I/O line for external card interfaces. Open drain with internal pull-up configuration – no external pull-up required
SCLK	88	1	O	Digital I/O line for external card interfaces.
SC4	85	1	I/O	Digital auxiliary I/O line for external card interfaces (C4 I/O). Open drain with internal pull-up configuration – no external pull-up required
SC8	86	1	I/O	Digital auxiliary I/O line for external card interfaces (C8 I/O). Open drain with internal pull-up configuration – no external pull-up required
TOTAL		**128**		

TYPICAL APPLICATION SCHEMATIC



ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to the device.

PARAMETER	RATING
Supply Voltage (V_{PD}, V_{PA}, V_{PC}, V_{PDPLL})	-0.5V to 4.0V
Supply Voltage (V_{PG})	-0.5V to 6.0V
Pin Input Voltage (except OSCIN12, OSCIN32)	-0.5V to 6.0V
Pin Input Voltage (OSCIN12, OSCIN32)	-0.5V to VPD + 0.5V
Storage Temperature	-60 to 150°C
Pin Current	±75mA
Maximum continuous Total Power Dissipation (at T_A = 85 °C)	1.2W
Maximum Operating Junction Temperature	125 °C
ESD Tolerance – Card interface pins*	+/- 5kV
ESD Tolerance – USB interface pins**	+/- 1.75kV
ESD Tolerance – Other pins	+/- 1kV

Note*: ESD testing on Card pins is HBM condition, 3 pulses, each polarity referenced to ground.
Note**: When an ESD tolerance of up to +/- 6kV is required on the USB interface pins, addition of 6.8V Zener diodes on D+ and D- are recommended. This is shown in the typical application schematic above.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage $V_{PA}/V_{PD}/V_{PC}$ with respect to $V_{NA}/V_{ND}/V_{NC}$ when not using USB I/F	2.7V to 3.6V
Supply Voltage $V_{PA}/V_{PD}/V_{PC}$ with respect to $V_{NA}/V_{ND}/V_{NC}$ when using USB I/F	3.0V to 3.6V
Supply Voltage V_{PD} with respect to V_{ND} for RAM data retention	2.0V to 3.6V
Supply Voltage (V_{PG}) with respect to V_{NG}[1]	2.7V to 5.5V
12MHz Oscillator Frequency	12.000 MHz ±100ppm
32768Hz Oscillator Frequency	32.768 KHz ±20ppm
Operating Temperature	0°C to +85°C
Input Voltage for DP/DM	0V to 3.6V
Input Voltage for ANA_IN(7:0)	0V to 3.6V

THERMAL RESISTANCE

PARAMETER	RATING
$R_{th\ (J-A)}$ Thermal Resistance Junction to Ambient	33º C/W

[1] VPG can be left unconnected if GPIO are not used.

DC CHARACTERISTICS: DIGITAL I/OS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Digital I/O except for OSC12 and OSC32 I/O						
V_{IL1}	Input Low Voltage (Except OSCIN32, OSCIN12)		-0.5		0.8	V
V_{IH1}	Input High Voltage (Except OSCIN32, OSCIN12)		0.7*V_{PD}		5.5	V
V_{OL}	Output Low Voltage (Except OSCOUT32, OSCOUT12)	I_{OL} = 2mA			0.45	V
V_{OH}	Output High Voltage (Except OSCOUT32, OSCOUT12)	I_{OH} = -1mA	V_{PD} - 0.45			V
I_{IL1}	Input Low Leakage Current (Except OSCIN32, OSCIN12)	$V_{SS} < V_{in} < V_{IL1}$ Pull-ups Disabled[2]			1	µA
I_{IH1}	Input High Leakage Current (Except OSCIN32, OSCIN12)	$V_{IH1} < V_{in} < V_{DD}$ Pull-downs Disabled[3]			1	µA
I_{IL3}	Input Low Leakage Current (Except OSCIN32, OSCIN12)	$V_{SS} < V_{in} < V_{IL1}$ Pull-ups Enabled[1]			30	µA
I_{IH3}	Input High Leakage Current (Except OSCIN32, OSCIN12)	$V_{IH1} < V_{in} < 5.5V$ Pull-downs Enabled[2]			100	µA

DC CHARACTERISTICS: OSCILLATOR I/OS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Oscillator (OSC) I/O Parameters						
V_{IL32}	Input Low Voltage - OSCIN32		-0.5		0.2* V_{PD}	V
V_{IH32}	Input High Voltage - OSCIN32		0.7*V_{PD}		V_{PD} + 0.5	V
V_{IL12}	Input Low Voltage - OSCIN12		-0.5		0.075* V_{PD}	V
V_{IH12}	Input High Voltage - OSCIN12		0.7*V_{PD}		V_{PD} + 0.5	V
$V_{OLOSC12}$	Output Low Voltage - OSCOUT12	I_{OL} = 3.0mA			0.7	V
$V_{OHOSC12}$	Output High Voltage - OSCOUT12	I_{OH} =-3.0mA	V_{PD} - 0.9			V
$V_{OLOSC32}$	Output Low Voltage - OSCOUT32	I_{OL} = 5 µA			0.25	V
$V_{OHOSC32}$	Output High Voltage - OSCOUT32	I_{OH} =-5 µA	0.5		V_{PD}	V
I_{IL2}	Input Leakage Current - OSCIN32, OSCIN12	$V_{SS} < V_{in} < V_{IL2}$	1		30	µA
I_{IH2}	Input High Leakage Current - OSCIN12, OSCIN32	$V_{IH2} < V_{in} < V_{DD}$	1		30	µA
$t_{OSC12MStart}$	12MHz Oscillator start up time	Osc V_{PP} = 90% stable V_{PP} @ V_{PC} = 3.3V, 25°C		500		µS
$t_{OSC32KStart}$	32KHz Oscillator start up time	Osc V_{PP} = 90% stable V_{PP} @ V_{PC} = 3.3V, 25°C		300		mS

[2] Pull-ups on USR1(7:0), GPIO(3:0), ROW(5:0)
[3] Pull-downs on ISP_Program, Prom_Program

DC CHARACTERISTICS: USB INTERFACE

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Receiver parameters						
V_{DI}	Differential input sensitivity	|(D+) - (D-)|	0.2			V
V_{CM}	Differential common mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Transmitter levels						
V_{OL}	Low Level Output Voltage	USBCon = 1 (D+ pull-up enabled)			0.3	V
V_{OH}	High Level Output Voltage	15K ohm resistor to ground	V_{PD} - 0.1		V_{PD}	V
Leakage parameters						
I_{OZ}	High-Z state data line leakage current	0V < VIN < 3.6V			±5	nA
Output resistance						
Z_{DRV}	Driver output resistance	Steady state drive	28		44	Ω
Z_{pu}[4]	Pull-up Resistor (to V_{PD})	USBCon = 1	1.2	1.5	1.8	kΩ
Transceiver power requirements (not measurable on tester)						
I_{PSO}	Operating supply current (output)	Outputs enabled			5	mA
I_{PSI}	Operating supply current (input)	Outputs Hi-Z			1	ma
I_{PDN}	Supply current in power down				10	nA
I_{PSS}	Supply current in suspend.				10	nA

[4] USB specifies that this value be 1.5k Ω +/- 5%. An external resistor could be used instead (MIUSCTRL bit 0 set by firmware)

DC CHARACTERISTICS: ICC INTERFACE - CLK AND RST SIGNALS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Clock Lines CLK and /CLK2 (VCC = VCC1 for CLK1 and VCC = VCC2 for CLK2)						
V_{OHC}	High Level Output Voltage	$0 < I_{OH} < 50\mu A$, V_{CC} = Min	V_{CC} - 0.5		V_{CC}	V
V_{OLC}	Low Level Output Voltage	$-50\mu A < I_{OL} < 0$, V_{CC} = Min	0		0.4	V
$t_{r\text{-}clk}$, $t_{f\text{-}clk}$	Rise / Fall time	C_{load} = 30pf max	-		8% of clock period	
P_{ERTLC}	Signal perturbation low	Signal low	- 0.25		0.4	V
P_{ERTHC}	Signal perturbation high	Signal high	V_{CC} - 0.5		V_{CC} + 0.25	V
δ	Duty Cycle	Clocks in stable operation	45		55	%
Reset Lines RST1 and RST2 (VCC = VCC1 for RST1 and VCC = VCC2 for RST2)						
V_{OHR}	High Level Output Voltage	$0 < I_{OH} < 50\mu A$, V_{CC} = Min	V_{CC} - 0.5		V_{CC}	V
V_{OLR}	Low Level Output Voltage	$-50\mu A < I_{OL} < 0$, V_{CC} = Min	0		0.4	V
$t_{r\text{-}RST}$, $t_{f\text{-}RST}$	Rise / Fall time	C_{load} = 30pf Max	-		0.8	µs
P_{ERTLR}	Signal perturbation low	Signal low	- 0.25		0.4	V
P_{ERTHR}	Signal perturbation high	Signal high	V_{CC} - 0.5		V_{CC} + 0.25	V

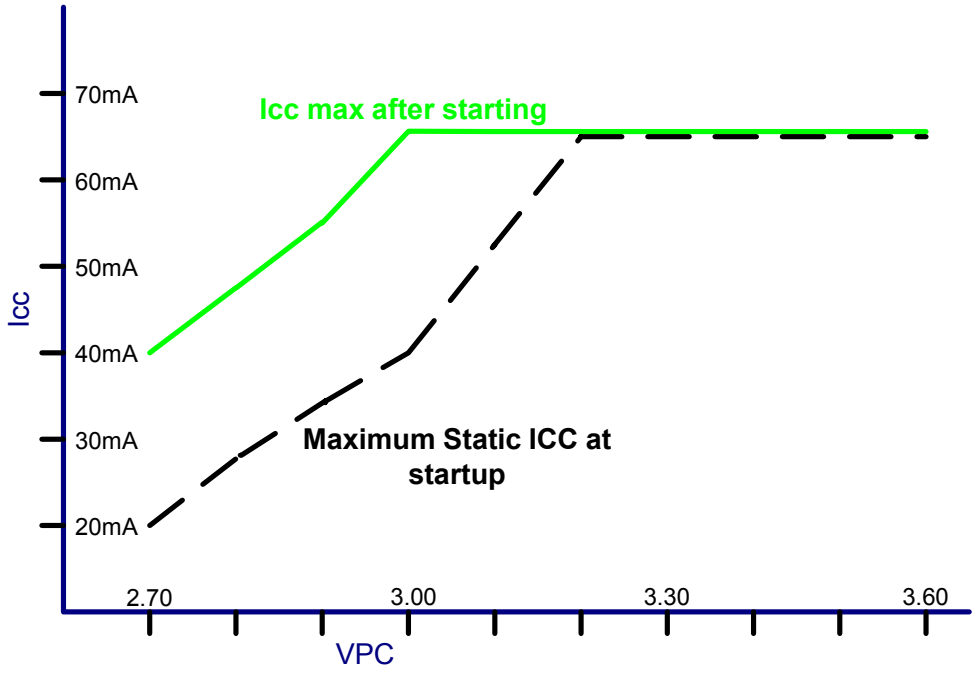
DC CHARACTERISTICS: ICC INTERFACE – I/O SIGNALS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Data Lines IO1/IO2, C41/C81, C42/C82 (VCC = VCC1 or VCC2 as appropriate)						
V_{OHSC}	High Level Output Voltage	$0 < I_{OH} < 20\mu A$, V_{CC} = Min	0.8 * V_{CC}		V_{CC}	V
V_{OLSC}	Low Level Output Voltage	$-1ma < I_{OL} < 0$, V_{CC} = Min	0		0.4	V
$t_{r\text{-}SC}$, $t_{f\text{-}SC}$	Rise / Fall time (Output)	Cload = 30pf Max	-		0.8	µs
P_{ERTLSC}	Signal perturbation low	Signal low	-0.25		0.4	V
P_{ERTHSC}	Signal perturbation high	Signal high	0.8 * V_{CC}		V_{CC} + 0.25	V
$I_{OLS}C$ (Inactive)	Current from I/O when inactive and pin grounded				-500	V
V_{ILSC}	High Level Input Voltage		0.6 * V_{CC}		V_{CC}	V
V_{ILSC}	Low Level Input Voltage		0		0.5	µs
I_{IHSC}	High Level Input Current	V_{in} = V_{IHSC} range	-300		20	µa
I_{ILSC}	Low Level Input Current	V_{in} = V_{ILSC} range	-1000		20	µa
I_{SCSC}	Short Circuit Current	33Ω to opp. supply	-15		15	ma
I_{RTFTSC}	Rise / Fall time (Input)		-		1.2	µs
R_{PUSC}	Pull-up to VCC	Static	10	12.5	17	kΩ

DC CHARACTERISTICS: ICC INTERFACE – VCC SIGNALS (DC-DC CONVERTER)

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Card Power Supply (V_{CC}) (V_{CC} = V_{CC} 1 or V_{CC} 2 as appropriate)						
V_{CC1} V_{CC2}	Output Voltages to ICC1 and ICC2 (with 40nAs dynamic loads and VNOISE included) 2.9V < VPC < 3.6V	5V output	4.6	5.0	5.4	V
		3V output	2.7	3.0	3.3	V
		Deactivated	-0.25	0.0	0.4	V
V_{NOISE}	Peak to peak ripple and noise on VCC	C_L = 6.8 µf and C_{cp} = 0.68 µf		150	200	mV pp
I_{CC1} I_{CC2}	Maximum Output Currents to ICC1 and ICC2	5V output	65		200	mA
		3V output	65		200	mA
I_{OC}	ICC over-current.	Each output measured separately		100	200	mA
I_{CC12}	Combined Current ICC1+ICC2 VPC 2.9V to 3.6V	5V output	65			mA
		3V output	65			mA
$I_{STARTUP}$*	V_{CC} Startup current	Assertion of $\overline{CMDVCC}$			See Curve	mA

Note: The following diagram shows the maximum start up and maximum operating current for V_{CC}. If the load placed on V_{CC} draws more current than line indicated by "Maximum Static ICC at startup" when V_{CC} is asserted, the DC-DC converter may not be able to achieve the minimum voltage levels as specified for V_{CC}2 above. Once the startup load condition has been met, the load can be increased to draw up to the current limit indicated by the line labeled "I_{CC} max after starting". This type of load increase is expected as the clock signal to the card is asserted and data transfer takes place. The diagram shows the worst case condition which is at 85°C.



DC CHARACTERISTICS: VOLTAGE REFERENCE

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
V_{BG}	Bandgap voltage	0.1μf external decoupling capacitor	1.1625	1.250	1.3375	V
V_{REF}	Voltage Reference	0.1μf external decoupling capacitor	2.325	2.500	2.675	V
V_{lvdet}	V_{PD} Low Voltage Flash Erase/Write Protect	Analog enabled (Disable_Analog = 0)	2.350	2.500	2.650	V

DC CHARACTERISTICS: ANALOG INPUTS

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
V_7	Voltage Threshold 7	ACOMP(3:1) =7	2.425	2.50	2.575	V
V_6	Voltage Threshold 6	ACOMP(3:1) =6	2.231	2.30	2.369	V
V_5	Voltage Threshold 5	ACOMP(3:1) =5	1.940	2.00	2.060	V
V_4	Voltage Threshold 4	ACOMP(3:1) =4	1.455	1.50	1.545	V
V_3	Voltage Threshold 3	ACOMP(3:1) =3	1.358	1.40	1.442	V
V_2	Voltage Threshold 2	ACOMP(3:1) =2	1.242	1.28	1.318	V
V_1	Voltage Threshold 1	ACOMP(3:1) =1	1.203	1.24	1.277	V
V_0	Voltage Threshold 0	ACOMP(3:1) =0	0.970	1.00	1.030	V
T_{comp}	Analog Compare time	CHANGE IN ACOMP(7:1)	0.1	0.2	2	μs

DC CHARACTERISTICS: POWER CONSUMPTION ON V_{PA} AND V_{PG}

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Analog (V_{PA}) Current						
$I_{DDA-off}$	Supply current on V_{PA} when Analog and USB Off	Disable_Analog = 1 Disable_USBXcvr=1		1	5	µA
I_{DDA-on}	Supply current on V_{PA} when Analog On and USB Off	Disable_Analog = 0 Disable_USBXcvr=1		1.0	1.5	mA
$I_{DDA-USBon}$	Supply current on V_{PA} when Analog and USB On	Disable_USBXcvr=0 Disable_Analog = 0		1.5	2.5	mA
GPIO interface Current Voltage Reference Current (V_{PG})						
$I_{DDGPIOon}$	Supply current on V_{PG} when GPIO interface active			56	75	µA
$I_{DDGPIOoff}$	Supply current on V_{PG} when GPIO interface inactive			1	5	µA

DC CHARACTERISTICS: POWER CONSUMPTION ON V_{PD}

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Digital (V_{PD}) Current						
I_{DDPD}	Digital supply current on V_{PD}, PD Mode , oscillators and clocks Off	OSCIN12 Off, OSCOUT32 Off, CPU in PD mode, All other clocks Off		1	20	µA
I_{DD32K}	Digital supply current on V_{PD}, PD Mode – Only 32kHz oscillator and RTC interrupt sub-routine running	OSCIN12 Off, OSCIN32 and RTC On, CPU in PD mode, All other clocks Off		10	35	µA
$I_{DDIDLE12M}$	Digital supply current on V_{PD}, IDLE Mode – 12MHz oscillator and clock circuitry (PLL) On, 32kHz oscillator Off	OSCIN12 On, OSCOUT32 Off CPU in IDLE mode, Disable_PLL=0, All other clocks Off, CPU clock=6MHz CPU clock=12MHz CPU clock=24MHz		3.1 3.4 3.8	5 5 5.5	mA
$I_{DDIDLE32K}$	Digital supply current on V_{PD}, IDLE Mode – 12MHz oscillator and clock circuitry (PLL) Off, 32kHz oscillator On	OSCIN12 Off, OSCIN32 and RTC On, CPU in IDLE mode, Disable_PLL=1, All other clocks Off, CPU clock=32kHz		16	50	µA
I_{DDSlow}	Digital supply current on V_{PD}, Normal Mode – 12MHz oscillator and clock circuitry (PLL) Off, 32kHz oscillator On	OSCIN12 Off, OSCIN32 On, CPU in Normal mode, All other clocks Off, CPU clock =32KHz		1.5	2.2	mA
I_{DDRun}	Digital supply current on V_{PD}, Normal Mode – 12MHz oscillator and clock circuitry (PLL) On, 32kHz oscillator Off	OSCIN12 On, OSCIN32 Off, All other clocks Off, CPU clock=6MHz CPU clock=12MHz CPU clock=24MHz		5.5 7.0 10	6.5 9.0 13	mA
$I_{DDSuspend}$	Digital supply current on V_{PD}, USB in Suspend mode	OSCIN12 Off, OSCIN32 Off and RTC Off, USB suspended, All internal clocks Off, CPU in PD mode		11	25	µA
V_{DDDR}	RAM data retention supply voltage		2.0			V

DC CHARACTERISTICS: POWER CONSUMPTION ON V_{PC}

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
DC-to-DC converter Current (V_{PC})						
$I_{DDon565}$	Supply current on V_{PC} when V_{CC}=5V and 65mA load	VCC1 = VCC2 = 5V. ICC1=ICC2 = 65mA, ICC IO, C4, C8 = high		280	300	mA
$I_{DDon365}$	Supply current on V_{PC} when V_{CC}=3V and 65mA load	VCC1 = VCC2 = 3V. ICC1=ICC2 = 65mA, ICC IO, C4, C8 = high		280	300	mA
$I_{DDon527}$	Supply current on V_{PC} when V_{CC}=5V and 27mA load	VCC1 = VCC2 = 5V. ICC1=ICC2 = 27mA, ICC IO, C4, C8 = high		110	125	mA
$I_{DDon327}$	Supply current on V_{PC} when V_{CC}=3V and 27mA load	VCC1 = VCC2 = 3V. ICC1=ICC2 = 27mA, ICC IO, C4, C8 = high		110	125	mA
$I_{DDon502}$	Supply current on V_{PC} when V_{CC}=5V and 2mA load	VCC1 = VCC2 = 5V. ICC1=ICC2 = 2mA, ICC IO, C4, C8 = high		10	13	mA
$I_{DDon302}$	Supply Current on V_{PC} when V_{CC}=3V and 2mA load	VCC1 = VCC2 = 3V, ICC1=ICC2 = 2mA, ICC IO, C4, C8 = high		10	13	mA
$I_{DDSCStdby5}$	Supply current on VPC when V_{CC}=5V and cards are in power down mode	VCC1 = VCC2 = 5V, ICC1=ICC2 = 0mA, ICC IO, C4, C8 = high Card clock stopped		1.5	3	mA
$I_{DDSCStdby3}$	Supply current on V_{PC} when V_{CC}=3V and cards are in power down mode	VCC1 = VCC2 = 3V, ICC1=ICC2 = 0mA, ICC IO, C4, C8 = high Card clock stopped		1.5	3	mA
$I_{DDSCOff}$	Supply current on V_{PC} when DC-DC converter is Off	V_{CC1} = V_{CC2} = 0V, 2MHz dc/dc clock Off, Analog circuitry Off		1	5	µA

AC CHARACTERISTICS: 8052 EXTERNAL MEMORY INTERFACE TIMING

SYMBOL	PARAMETER	MIN	Typ.	MAX	UNIT
F_{OSC}	Processor Clock Frequency	0	12.00	24	MHz
T_{OSC}	Processor Clock Period		83.33		ns
T_{LHLL}	ALE Pulse Width	$2T_{OSC}$ - 10			ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC}			ns
T_{LLAX}	Address Valid to ALE Low	T_{OSC} - 10			ns
T_{LLPL}	ALE Low to $\overline{PSEN}$ Low	T_{OSC} - 10			ns
T_{PLPH}	$\overline{PSEN}$ Pulse Width Low	$3T_{OSC}$ - 20			ns
T_{PLIV}	$\overline{PSEN}$ Low to Valid Inst In			$3T_{OSC}$ - 50	ns
T_{AVIV}	Address to Valid Inst In			$6T_{OSC}$ - 50	ns
T_{PXIX}	Input Instr Hold-$\overline{PSEN}$ High	0			ns
T_{PXIZ}	$\overline{PSEN}$ Instr Float-$\overline{PSEN}$ High			20	ns
T_{PLAZ}	$\overline{PSEN}$ Low to Address HighZ			10	ns
T_{RLRH}	$\overline{RD}$ Pulse Width	$6T_{OSC}$ - 20			ns
T_{WLWH}	$\overline{WR}$ Pulse Width	$6T_{OSC}$ - 20			ns
T_{RLDV}	RD Low to Valid Data In			$5T_{OSC}$ - 50	ns
T_{RHDX}	Data Hold After $\overline{RD}$	0			ns
T_{RHDZ}	Data Float After $\overline{RD}$			20 *	ns
T_{LLDV}	ALE Low to Valid Data In			$8T_{OSC}$ - 50	ns
T_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ Low	$3T_{OSC}$ - 20		$3T_{OSC}$ + 20	ns
T_{QVWX}	Data Valid to $\overline{WR}$ Low	T_{OSC}			ns
T_{WHQZ}	Data Hold After $\overline{WR}$ High	T_{OSC} - 10			ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float			10	ns

AC CHARACTERISTICS: USB INTERFACE

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
C_L = 50pF, series 36Ω, 1% source termination resistor included						
T_{R_USB}	Rise Time	10% to 90%	4		20	ns
T_{F_USB}	Fall Time	90% to 10%	4		20	ns
T_{RFM}	Rise/fall time matching	(USBTR/USBTF)	90		111.11	%
V_{CRS}	Output signal crossover voltage	Includes VDI range	1.3		2.0	V
T_{DJ1}[5,6]	Source Jitter to Next Transition	Measured as in Figure 4.4.2.1 of USB 2.0 Specification	-3.5		3.5	ns
T_{DJ2}[1, 2]	Source Jitter For Paired Transitions	Measured as in Figure 4.4.2.1 of USB 2.0 Specification	-4		4	ns
T_{JR1}	Receiver Jitter to Next Transition	Measured as in Figure 4.4.2.2 of USB 2.0 Specification	-18.5		18.5	ns
T_{JR2}	Receiver Jitter for Paired Transitions	Measured as in Figure 4.4.2.2 of USB 2.0 Specification	-9		9	ns
T_{EOPT}	Source SE0 interval of EOP	Figure 4.4.2.3 of USB 2.0 Specification	160		175	ns
T_{EOPR}[7]	Receiver SEO interval of EOP	Figure 4.4.2.3 of USB 2.0 Specification	82			ns

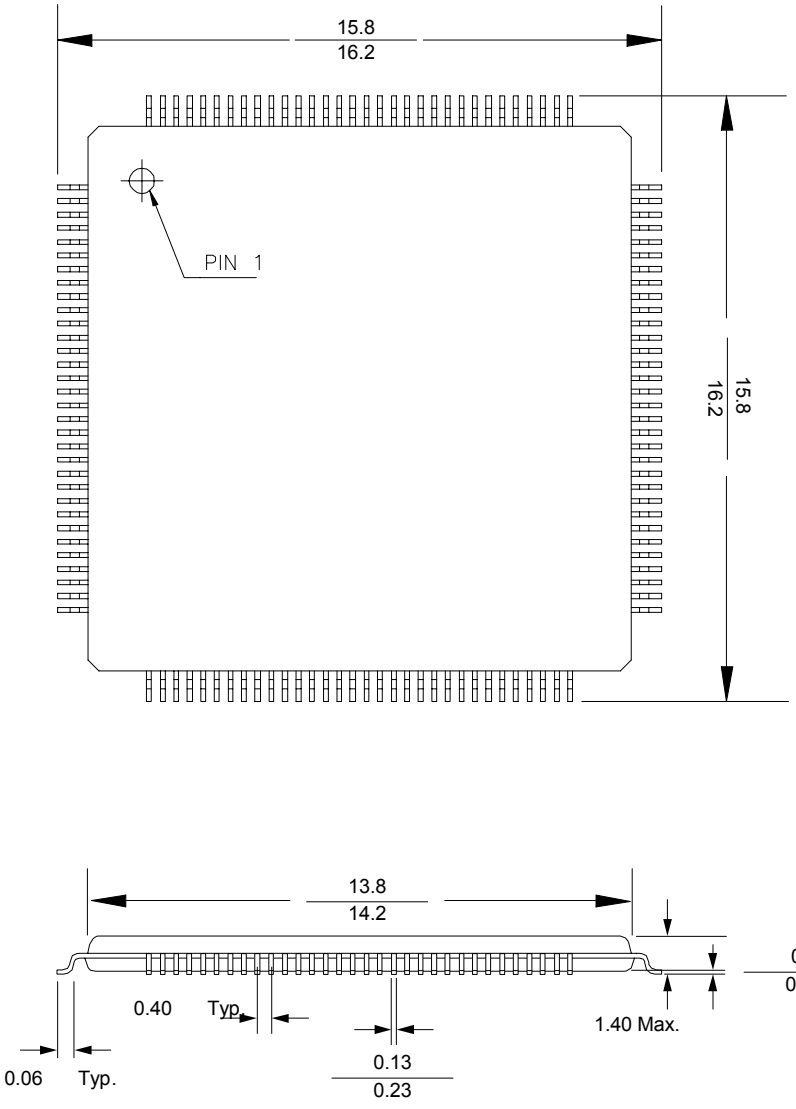
5 For both transitions of differential signaling.
6 Excluding first transition from the Idle state.
[7] Must accept as valid EOP.

MECHANICAL DRAWINGS

CAUTION: Use handling procedures necessary for a static sensitive component

The following figure shows the package outline of the 73S1121F in its TQFP 128-pin packaged form. It is available in both tray and tape-reel conditioning.

The 73S1121F is also available in Die form. Mechanical information is available under NDA. Please contact any TDK Semiconductor representative for further information about it.

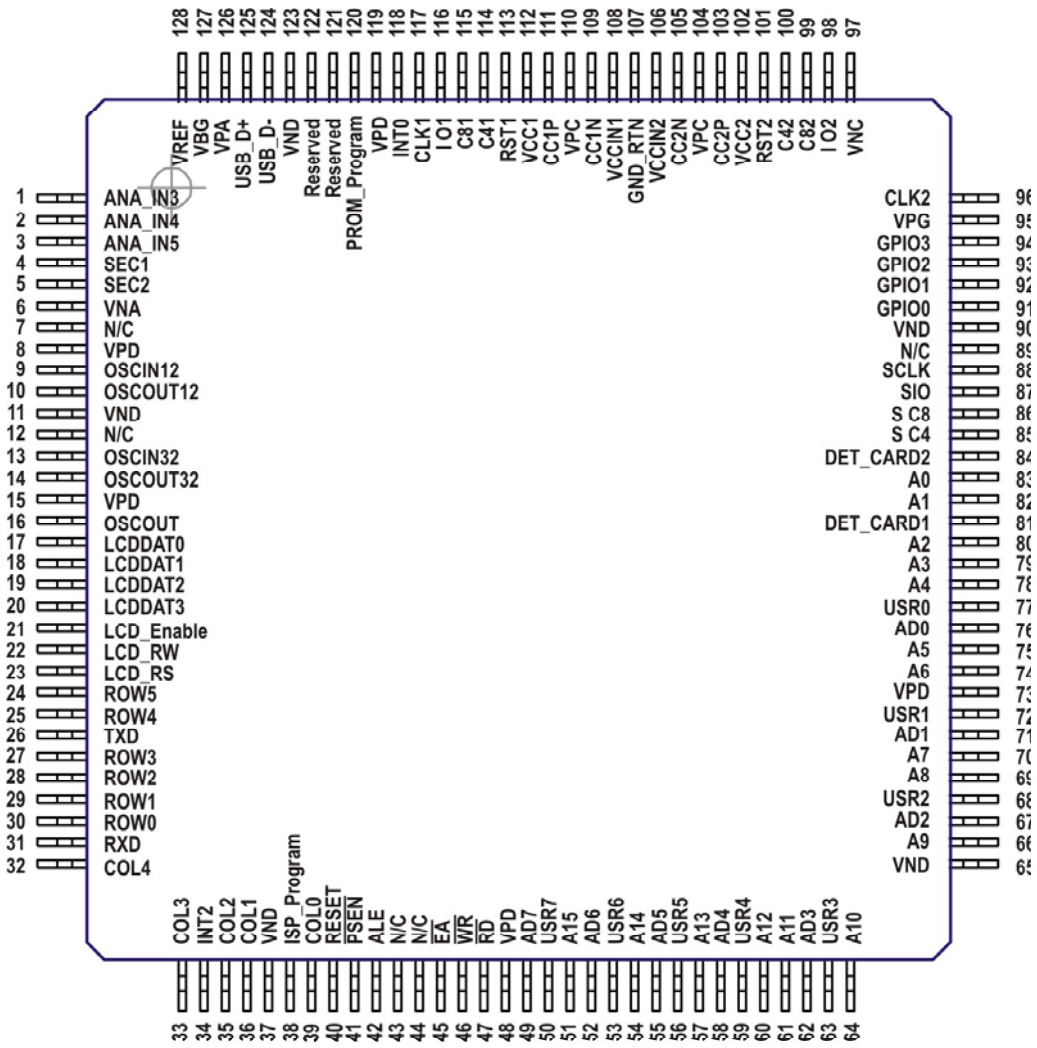


Controlling dimensions in mm

TQFP 128 – Package Outline

PACKAGE PIN DESIGNATIONS

(Top View)



TQFP128 Pin Assignment (Top View)

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGING MARK
73S1121F – Die form	73S1121F-D	N/A
73S1121F - 128 pin TQFP	73S1121F-CGV	73S1121F-CGV
73S1121F - 128 pin TQFP Tape / Reel	73S1121F-CGVR	73S1121F-CGV
73S1121F - 128 pin TQFP Lead-Free	73S1121F-CGV / F	73S1121F-CGV
73S1121F - 128 pin TQFP Lead-Free Tape / Reel	73S1121F-CGVR / F	73S1121F-CGV

Data Sheet

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