

74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Parallel Registered Outputs
- Internal Counters Have Direct Clear
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE
(TOP VIEW)

QB	1	20	QA
QC	2	19	CCK
QD	3	18	CCKEN
GND	4	17	CCLR
GND	5	16	V_{CC}
GND	6	15	V_{CC}
GND	7	14	OE
QE	8	13	RCK
QF	9	12	RCO
QG	10	11	QH

description

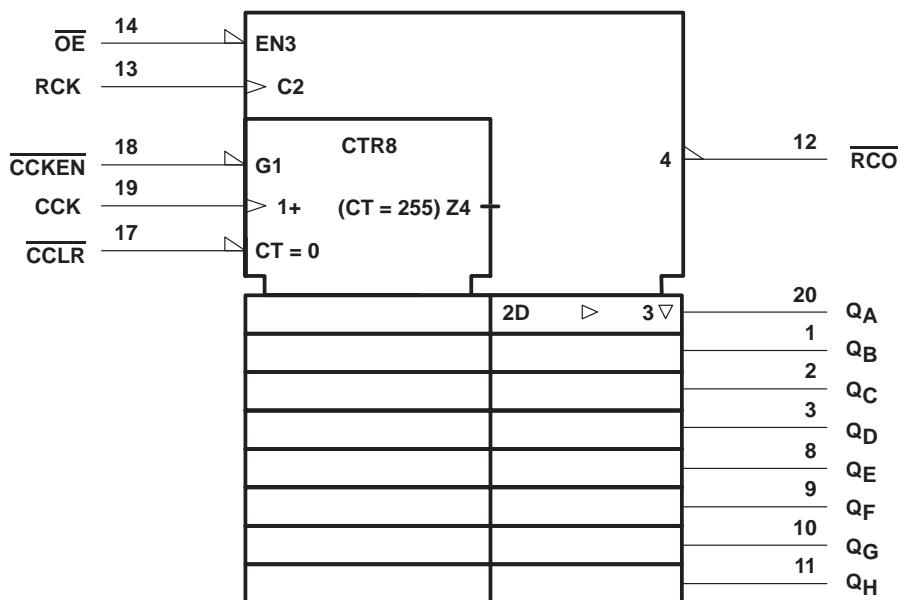
The 74ACT11590 contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register.

The binary counter features a direct clear (\overline{CCLR}) input and a count-enable (\overline{CCKEN}) input. For cascading, a ripple-carry (\overline{RCO}) output is provided. Expansion is easily accomplished for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to \overline{CCK} of the following stage.

Both the register and the counter have individual positive-edge-triggered clocks. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The 74ACT11590 is characterized for operation from -40°C to 85°C .

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPIC is a trademark of Texas Instruments Incorporated.

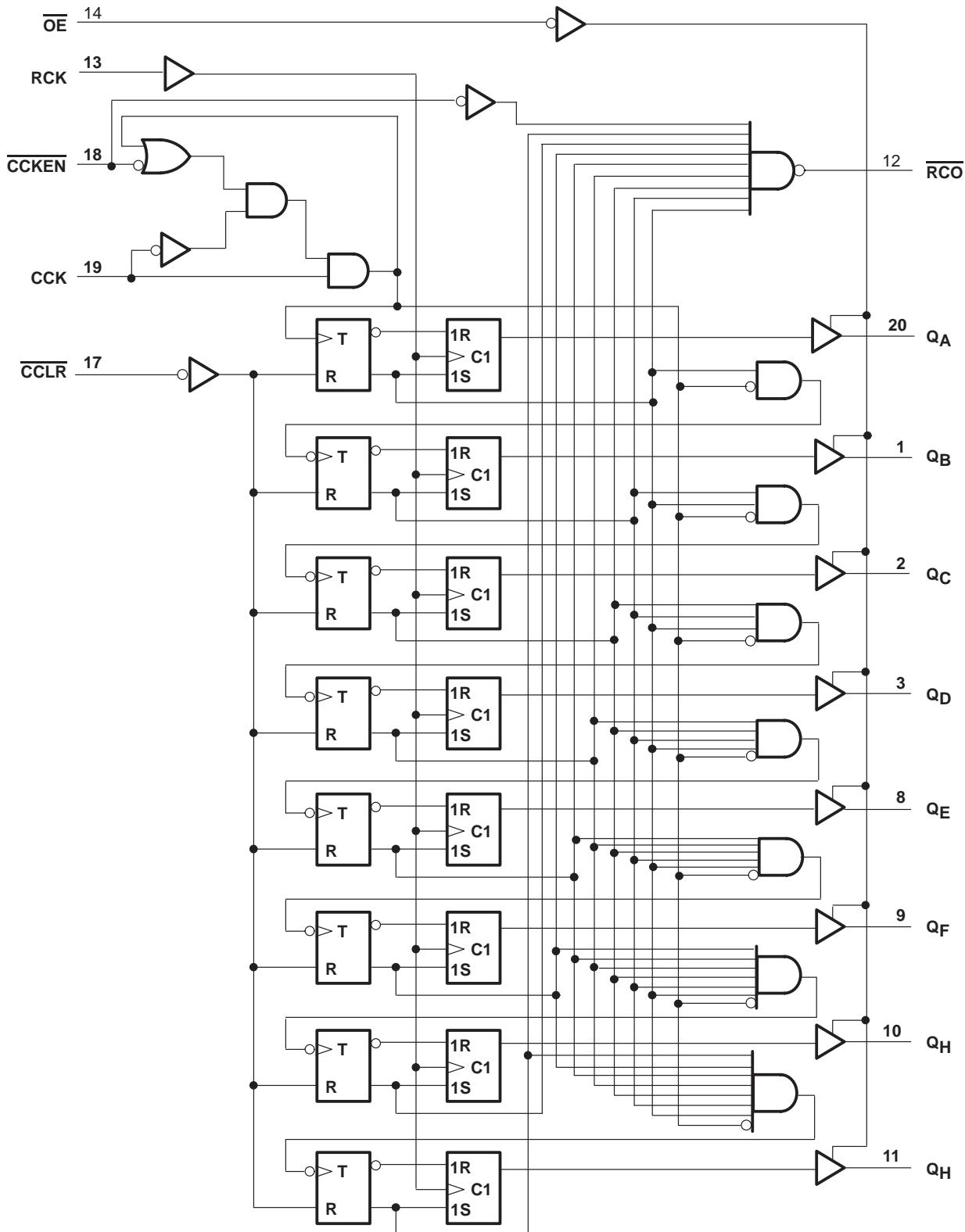
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1993, Texas Instruments Incorporated

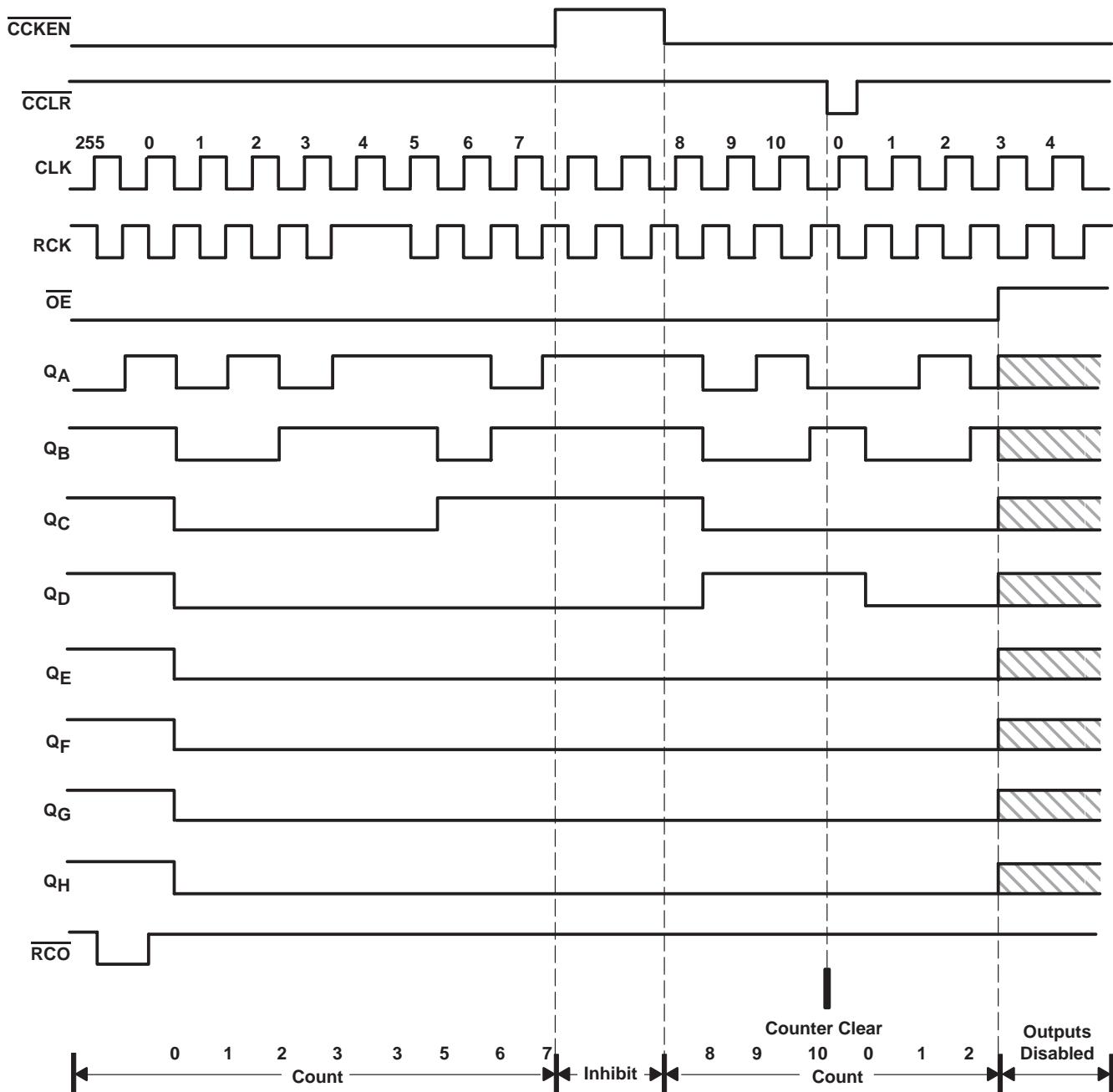
**74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS**

SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

logic diagram (positive logic)



typical operating sequence



74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS

SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±225 mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10		ns/V
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

74ACT11590
8-BIT BINARY COUNTER
WITH REGISTERED 3-STATE OUTPUTS
SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 µA	4.5 V	4.4		4.4	V	5.4	V
		5.5 V	5.4		5.4			
	I _{OH} = -24 mA	4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
	I _{OH} = -75 mA [†]	5.5 V			3.85			
V _{OL}	I _{OL} = 50 µA	4.5 V		0.1	0.1	V	0.1	V
		5.5 V		0.1	0.1			
	I _{OL} = 24 mA	4.5 V		0.36	0.44			
		5.5 V		0.36	0.44			
	I _{OL} = 75 mA [†]	5.5 V						
I _I	V _I = V _{CC} or GND	5.5 V		±0.1	±1	µA		
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5	±5	µA		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8	80	µA		
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V		0.9	1	mA		
C _i	V _I = V _{CC} or GND	5 V		3		pF		
C _o	V _O = V _{CC} or GND	5 V		11		pF		

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f _{clock}	Clock frequency, CCK or RCK		0	80	0	80	MHz
t _w	Pulse duration	CCK or RCK high or low	6.3		6.3	ns	
		CCLR low	8.4		8.4		
t _{su}	Setup time	CCKEN low before CCK↑	5.1		5.1	ns	
		CCLR high before CCK↑	1.6		1.6		
		CCK↑ before RCK↑ [§]	5.5		5.5		
t _h	Hold time	CCKEN low after CCK↑	0.6		0.6	ns	

[§] This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.

74ACT11590

8-BIT BINARY COUNTER

WITH REGISTERED 3-STATE OUTPUTS

SCAS195 – D3989, MARCH 1992 – REVISED APRIL 1993

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		80		80			MHz
t_{PLH}	CCK	\overline{RCO}	4.5	8	11	4.5	13	ns
t_{PHL}			5.1	9	13.8	5.1	16.4	
t_{PLH}	\overline{CCLR}	\overline{RCO}	3.5	7	11	3.5	13.1	ns
t_{PLH}	RCK	Q	4.6	8	11.1	4.6	13	ns
t_{PHL}			3.9	7.6	11.8	3.9	13.9	
t_{PZH}	\overline{OE}	Q	4	8.3	13.2	4	15.6	ns
t_{PZL}			3.8	8.2	13.9	3.8	16.2	
t_{PHZ}	\overline{OE}	Q	5.3	8	10.3	5.3	11.5	ns
t_{PLZ}			6.1	9.1	11.5	6.1	13	
t_{PLH}	\overline{CCKEN}	\overline{RCO}	3.8	6.8	9.7	3.8	11.2	ns
t_{PHL}			2.8	7.6	11	2.8	12.8	

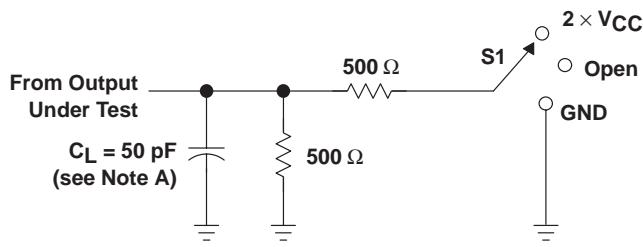
operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	66	pF
		Outputs disabled		42	

TEXAS
INSTRUMENTS

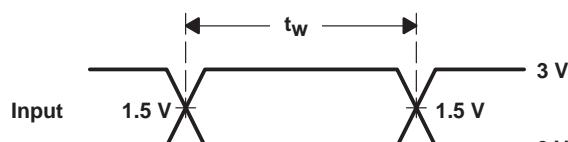
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

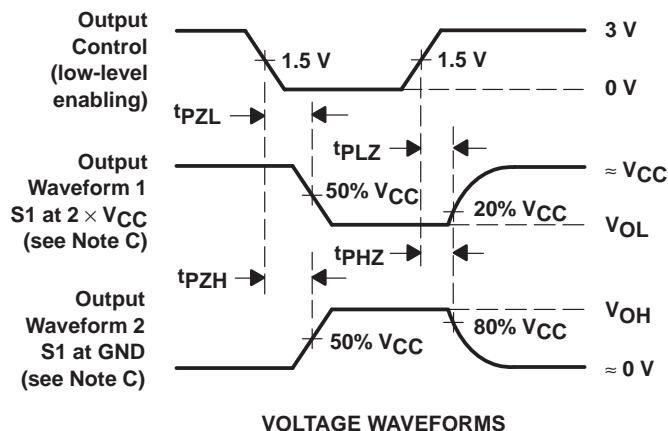
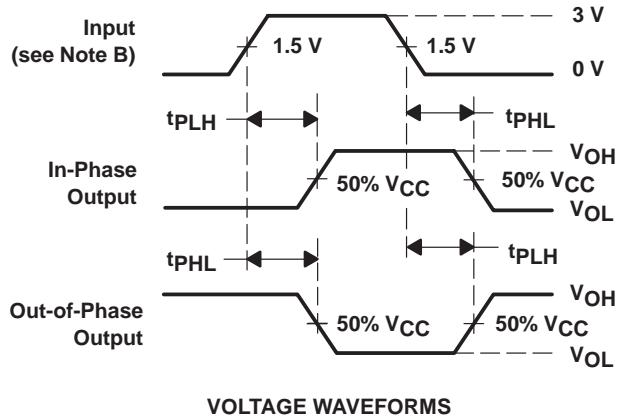
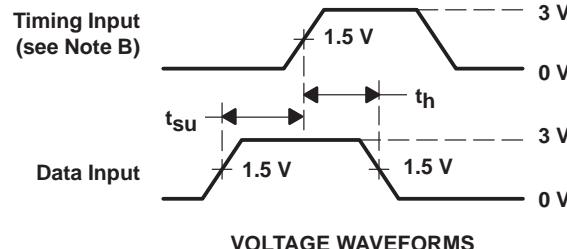


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 \times V _{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated