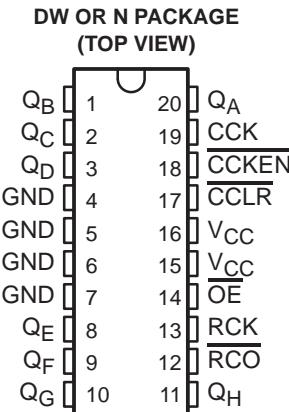


- Parallel Registered Outputs
- Internal Counters Have Direct Clear
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs



description

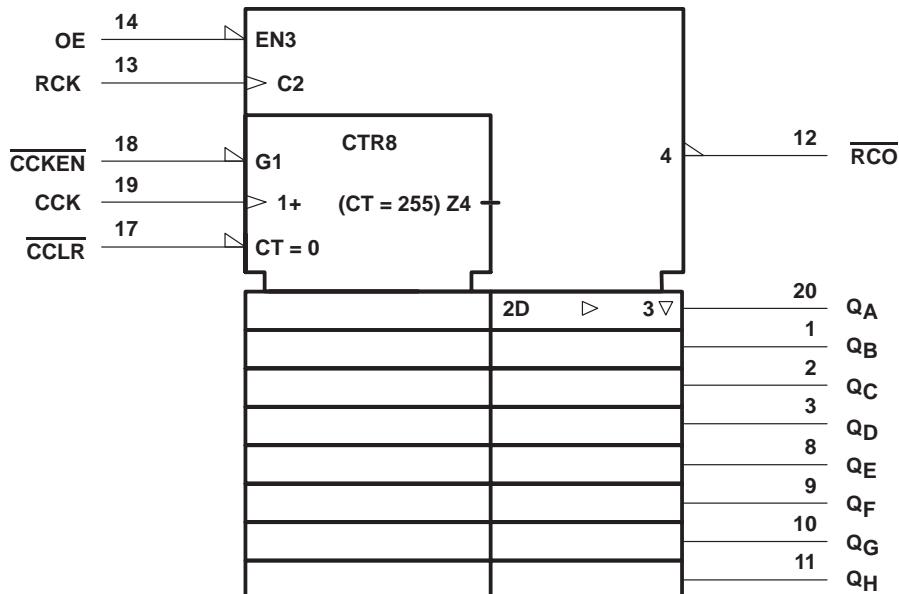
The 74AC11590 contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register.

The binary counter features a direct clear (CCLR) input and a count-enable (CCKEN) input. For cascading, a ripple-carry (RCO) output is provided. Expansion is easily accomplished for two stages by connecting RCO of the first stage to CCKEN of the second stage. Cascading for larger count chains can be accomplished by connecting RCO of each stage to CCK of the following stage.

Both the register and the counter have individual positive-edge-triggered clocks. If both clocks are connected together, the counter state is always one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The 74AC11590 is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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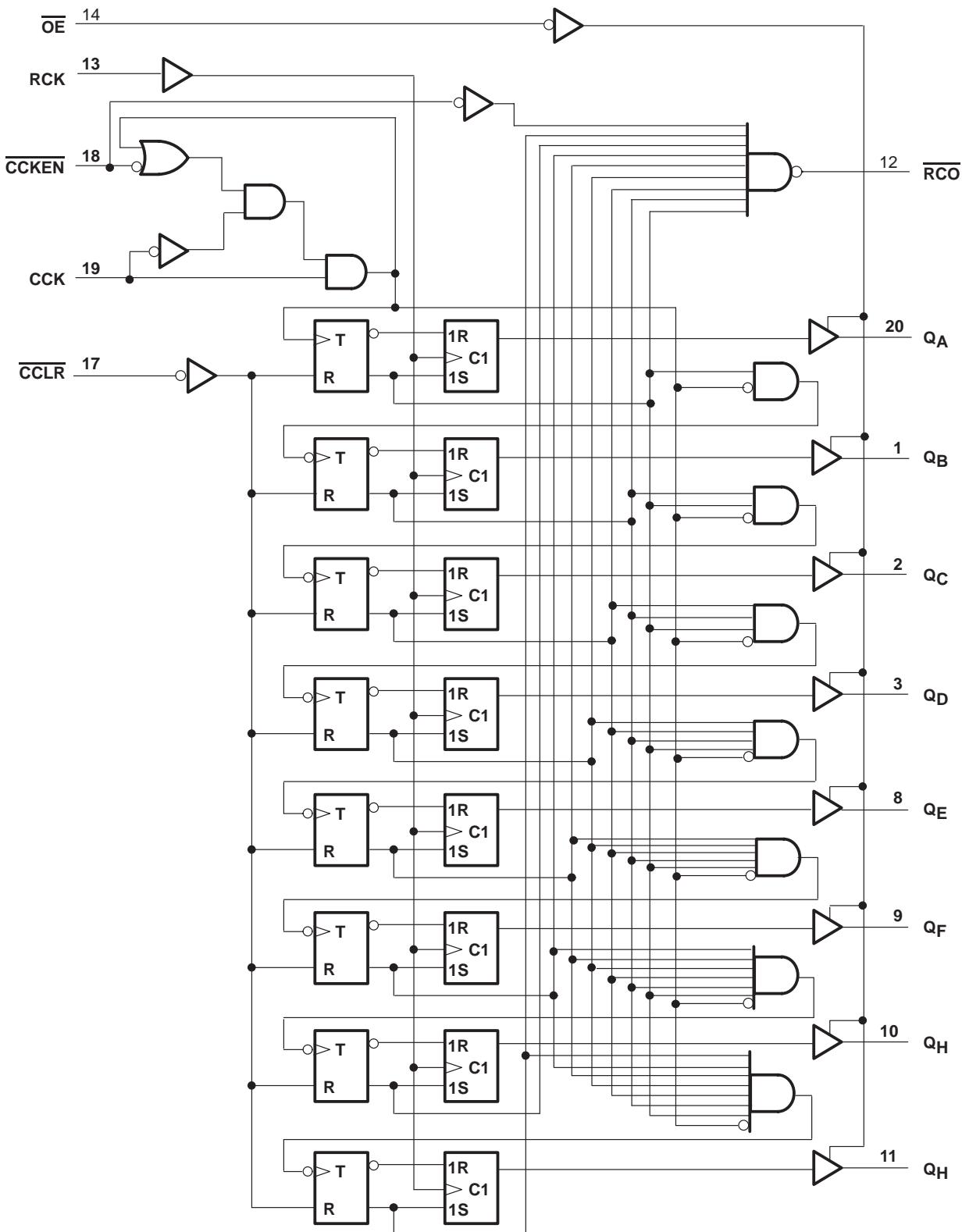
74AC11590

8-BIT BINARY COUNTER

WITH REGISTERED 3-STATE OUTPUTS

SCAS194 – D3988, MARCH 1992 – REVISED APRIL 1993

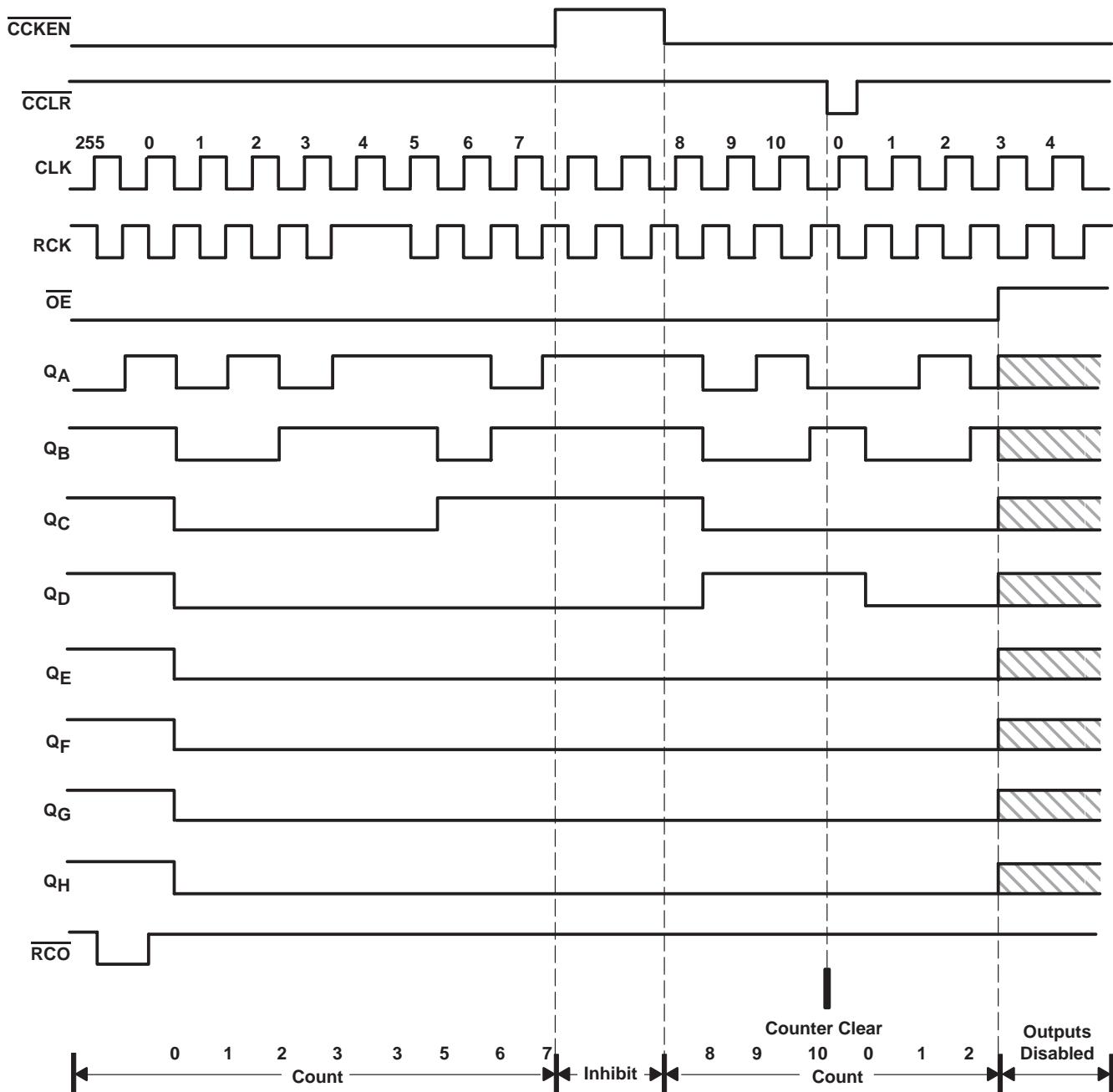
logic diagram (positive logic)



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typical operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	-0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±225 mA
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 5.5$ V	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V	0.9		V
		$V_{CC} = 4.5$ V	1.35		
		$V_{CC} = 5.5$ V	1.65		
V_I	Input voltage	0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		V
I_{OH}	High-level output current	$V_{CC} = 3$ V	-4		mA
		$V_{CC} = 4.5$ V	-24		
		$V_{CC} = 5.5$ V	-24		
I_{OL}	Low-level output current	$V_{CC} = 3$ V	12		mA
		$V_{CC} = 4.5$ V	24		
		$V_{CC} = 5.5$ V	24		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V	
T_A	Operating free-air temperature	-40	85		°C

NOTE 2: Unused or floating inputs must be held high or low.

74AC11590
**8-BIT BINARY COUNTER
 WITH REGISTERED 3-STATE OUTPUTS**
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 µA	3 V	2.9		2.9	V		
		4.5 V	4.4		4.4			
		5.5 V	5.4		5.4			
	I _{OH} = -4 mA	3 V	2.58		2.48			
		4.5 V	3.94		3.8			
	I _{OL} = -24 mA	5.5 V	4.94		4.8			
		5.5 V			3.85			
	I _{OH} = -75 mA†							
V _{OL}	I _{OL} = 50 µA	3 V	0.1		0.1	V		
		4.5 V	0.1		0.1			
		5.5 V	0.1		0.1			
	I _{OL} = 12 mA	3 V	0.36		0.44			
		4.5 V	0.36		0.44			
	I _{OL} = 24 mA	5.5 V	0.36		0.44			
		5.5 V			1.65			
I _I	V _I = V _{CC} or GND	5.5 V		±0.1	±1			µA
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5	±5			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8	80			µA
C _i	V _I = V _{CC} or GND	5 V		3				pF
C _o	V _O = V _{CC} or GND	5 V		11				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		TA = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f _{clock}	Clock frequency, CCK or RCK	0	50	0	50	MHz
t _w	Pulse duration	CCK or RCK high or low	10	10	7.4	ns
		CCLR low	7.4	7.4		
t _{su}	Setup time	CCKEN low before CCK↑	5.2	5.2	8.1	ns
		CCLR high before CCK↑	3.4	3.4		
		CCK↑ before RCK↑‡	8.1	8.1		
t _h	Hold time	CCKEN low after CCK↑	0	0		ns

‡ This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT	
			MIN	MAX				
f_{clock}	Clock frequency, CCK or RCK			0	80	0	80	MHz
t_w	Pulse duration	CCK or RCK high or low	6.3	6.3	ns	ns	ns	
		\overline{CCLR} low	4.9	4.9				
t_{su}	Setup time	CCKEN low before CCK \uparrow	3.7	3.7	ns	ns	ns	
		\overline{CCLR} high before CCK \uparrow	1.6	1.6				
		CCK \uparrow before RCK \uparrow \dagger	5.5	5.5				
t_h	Hold time			CCKEN low after CCK \uparrow	0.5	0.5	ns	ns

\dagger This setup time ensures that the register will see stable data from the counter outputs. The clocks may be tied together, in which case the register will be one clock pulse behind the counter.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		50		50			MHz
t_{PLH}	CCK	\overline{RCO}	7	13.5	15.9	7	18.3	ns
			9	16.9	19.5	9	22.1	
t_{PLH}	\overline{CCLR}	\overline{RCO}	6.2	12.4	14.8	6.2	17.1	ns
t_{PLH}	RCK	Q	7.3	13.7	16.2	7.3	18.7	ns
			7	13.6	15.9	7	17.9	
t_{PZH}	\overline{OE}	Q	7.8	15.5	18.5	7.8	21.1	ns
			8.5	18.2	21.4	8.5	24.5	
t_{PHZ}	\overline{OE}	Q	6.3	10	11.9	6.3	13.2	ns
			6.8	10.8	12.8	6.8	14.1	
t_{PLH}	CCKEN	\overline{RCO}	6	11.7	14	6	16.2	ns
			6	11.6	13.7	6	15.4	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	CCK or RCK		80		80			MHz
t_{PLH}	CCK	RCO	3.6	7.8	10.2	3.6	11.7	ns
			4.7	9.8	12.7	4.7	14.4	
t_{PLH}	\overline{CCLR}	\overline{RCO}	3.2	7.2	9.5	3.2	10.9	ns
t_{PLH}	RCK	Q	3.7	8	10.4	3.7	12	ns
			3.6	8.2	10.7	3.6	12.1	
t_{PZH}	OE	Q	3.8	8.9	11.9	3.8	13.6	ns
			3.7	9.5	12.6	3.7	14.3	
t_{PHZ}	OE	Q	4.5	7.5	9.4	4.5	10.5	ns
			5.4	8.7	10.8	5.4	12	
t_{PLH}	CCKEN	\overline{RCO}	3	6.9	9	3	10.4	ns
			2.9	7	9.2	2.9	10.4	

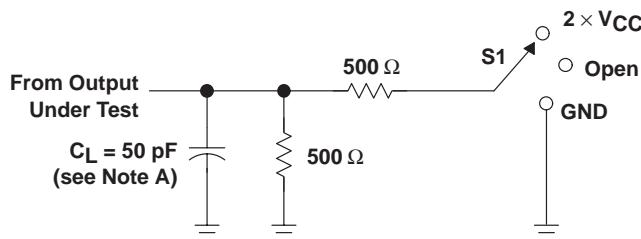
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operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

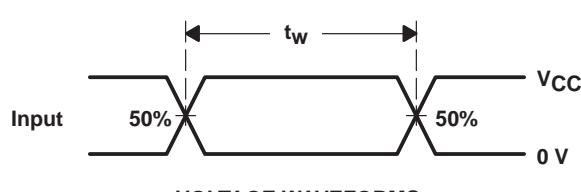
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}, f = 1 \text{ MHz}$	66
		Outputs disabled		43

PARAMETER MEASUREMENT INFORMATION

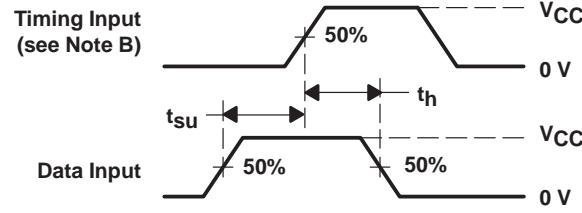


TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	$2 \times V_{CC}$
tPHZ/tPZH	GND

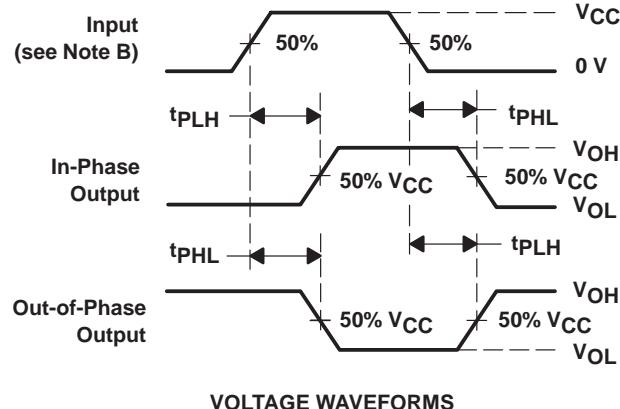
LOAD CIRCUIT



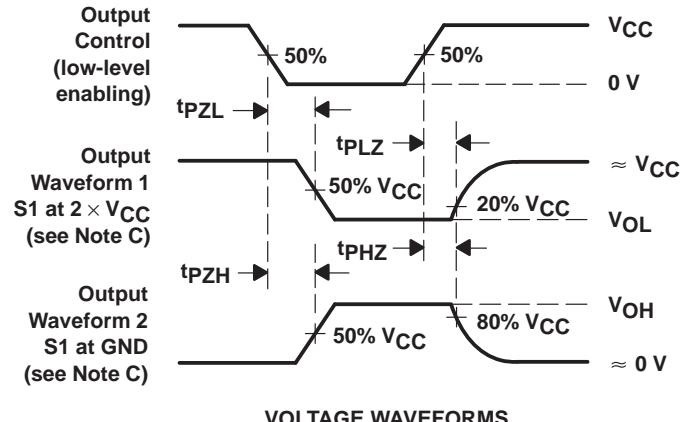
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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