National Semiconductor

MICROCIRCUIT DATA SHEET

CN74F164A-X REV 0A0

Original Creation Date: 04/14/97
Last Update Date: 05/06/97
Last Major Revision Date: 04/14/97

SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

General Description

The F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. The 'F164A is a faster version of the 'F164.

Industry Part Number

74F164A

NS Part Numbers

74F164ADC

Prime Die

M164A

Processing

Quality Conformance Inspection

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+70
3	Static tests at	0
4	Dynamic tests at	+25
5	Dynamic tests at	+70
6	Dynamic tests at	0
7	Functional tests at	+25
8A	Functional tests at	+70
8B	Functional tests at	0
9	Switching tests at	+25
10	Switching tests at	+70
11	Switching tests at	0

Features

- Typical Shift Frequency of 90 MHZ
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- Guaranteed 4000V Minimum ESD Protection

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0 C to +70 C
Supply Voltage	
Commercial	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VIH	Input HIGH Voltage	Recognized as a HIGH Signal	1	INPUTS	2.0		V	1, 2, 3
VIL	Input LOW Voltage	Recognized as a LOW Signal	1	INPUTS		0.8	V	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IIN=-18mA	2, 3	INPUTS		-1.2	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, IOH=-1.0mA	2, 3	OUTPUTS	2.5		V	1, 2, 3
		VCC=4.75V, IOH=-1.0mA	2, 3	OUTPUTS	2.7		V	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, IOL = 20mA	2, 3	OUTPUTS		0.5	V	1, 2, 3
IIH	Input HIGH Current	VCC=5.5V, VIN=2.7V	2, 3	INPUTS		5.0	uA	1, 2, 3
IBVI	Input HIGH Current Breakdown Test	VCC=5.5V, VIN=7.0V	2, 3	INPUTS		7.0	uA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VOUT = VCC	2, 3	OUTPUTS		100	uA	1, 2, 3
VID	Input Leakage Test	VCC = 0.0V, IID = 1.9uA, All other pins grounded	2, 3	INPUTS	4.75		V	1, 2, 3
IOD	Output Leakage Circuit Current	VCC = 0.0V, VIOD = 150mV, All other pins grounded	2, 3	OUTPUTS		4.75	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VIN=0.5V	2, 3	INPUTS		-0.6	mA	1, 2, 3
IOS	Output Short-Circuit Current	VCC=5.5V, VOUT = 0V	2, 3	OUTPUTS	-60	-150	mA	1, 2, 3
ICC	Power Supply Current	VCC=5.5V, CP=HIGH, $\overline{MR}$=GND, A, B=GND	2, 3	VCC		55	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS. Temp Range: 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
fMAX	Maximum Shift Frequency	VCC=+5.0V @ +25C VCC=4.5V & 5.5V @ 0/+70C	4		80		MHZ	9, 10, 11
tpLH	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	CP to Qn	3.0	7.5	ns	9, 10, 11
tpHL	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	CP to Qn	3.5	8.0	ns	9, 10, 11
tpHL (2)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	$\overline{MR}$ to Qn	5.0	10.0	ns	9
			2, 3	$\overline{MR}$ to Qn	5.0	10.5	ns	10, 11
ts (H)	Setup Time HIGH	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	A/B to CP	4.5		ns	9, 10, 11
ts (L)	Setup Time LOW	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	A/B to CP	4.0		ns	9, 10, 11
th (H/L)	Hold Time HIGH or LOW	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	A/B to CP	1.0		ns	9, 10, 11
tw (H)	Pulse Width HIGH	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	CP	4.0		ns	9, 10, 11
tw (L)	Pulse Width LOW	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	CP	7.0		ns	9, 10, 11
tw (L) (2)	Pulse Width LOW	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	$\overline{MR}$	4.0		ns	9, 10, 11
trec	Recovery Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	$\overline{MR}$ to CP	5.0		ns	9, 10, 11

Note 1: Guaranteed by applying specific input condition and testing VOL & VOH.
Note 2: Screen tested 100% on each device at +75 C temperature only, subgroups A2 & A10.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +75C temperature only, subgroups A2 & A10.
Note 4: Guaranteed but not tested.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0001281	05/06/97	Donald B. Miller	