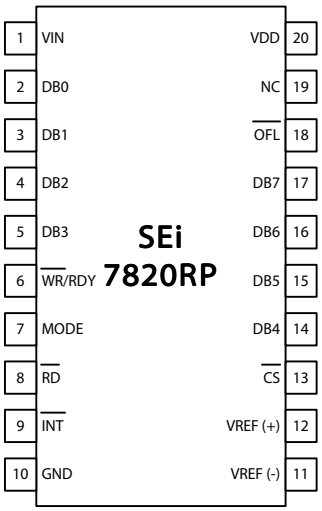
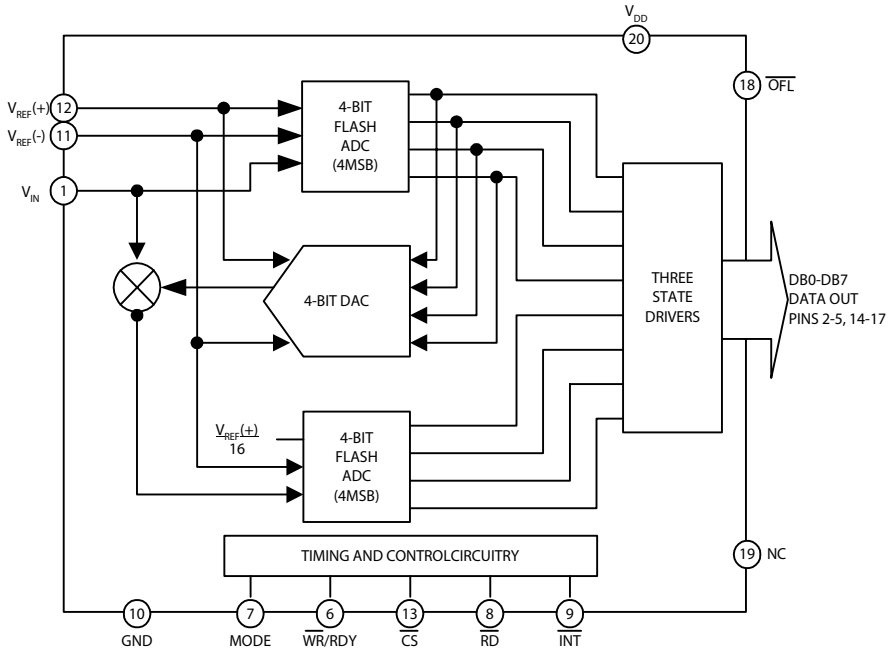
PRELIMINARY

SPACE ELECTRONICS INC.
SPACE PRODUCTS

MICROPROCESSOR-COMPATIBLE 8-BIT ADC

7820RP





FEATURES:

- 1.36uS Conversion Time
- Built-in Track-and-Hold Function
- No Missing Codes
- Single +5 Volt Supply
- No External Clock
- Tri-State Output Buffered
- Total Ionization Dose Enhanced to 100krads (Si) Dependent on Orbit
- Single Event Effects TBD

DESCRIPTION:

The 7820RP is a microprocessor compatible 8-Bit Analog-to-Digital Converter with a 0V to +5V input supply range with a single +5 Volt supply.

The 7820RP incorporates internal sample-and-hold circuitry which eliminates the need for an external S/H for signals with slew rates less than 100mV/uS.

The 7820RP was designed to be easily interfaced with microprocessors appearing as a memory location or I/O port without the need for external interfacing. All outputs are latched, tri-state buffered.

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TABLE 1. 7820RP ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	MIN	MAX	UNITS
V_{DD} to GND	-0	7	V
Digital Input Voltage to GND (Pins 6-80, 13)	-0.3	V_{DD}+0.3	V
Digital Output Voltage to GND (Pins 2-5, 9, 14-18)	-0.3	V_{DD}+0.3	V
V_{REF}(+) to GND	V_{REF}(-)	V_{DD}+0.3	V
V_{REF}(-) to GND	0	V_{REF}(+)	V
V_{IN} to GND	-0.3	V_{DD}+0.3	V
Operating Temperature	-55	+125	°C
Storage Temperature Range	-65	+150	°C
Power Dissipation to 75°C	-	450	mW
Derates above +75°C	-	6	mW/°C

1. **CAUTION**: ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

TABLE 2. 7820RP DC CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution	-	8	-	-	Bits
Total Unadjusted Error [1]	-	-	-	±1/2	LSB
Minimum Resolution for which No Missing Codes are guaranteed	-	-	-	8	Bits
REFERENCE INPUT					
Input Resistance	-	1.0	-	4.0	kΩ
V_{REF}(+) Input voltage Range	-	V_{REF}(-)	-	V_{DD}	V
V_{REF}(-) Input voltage Range	-	GND	-	V_{REF}(+)	V
ANALOG INPUT					
Input Voltage Range	-	V_{REF}(-)	-	V_{REF}(+)	V
Input Leakage Current	-	-	-	±3	µA
Input Capacitance [2]	-	-	45	-	pF
LOGIC INPUTS					
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$					
V_{INH}	-	2.4	-	-	V
V_{INH}	-	-	-	0.8	V

TABLE 2. 7820RP DC CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{INH}($\overline{CS}$, $\overline{RD}$)	-	-	-	1	µA
I_{INH}($\overline{WR}$)	-	-	-	3	µA
I_{INL}($\overline{WR}$)	-	-	-	-1	µA
Input Capacitance [2]	-	-	5	8	pF
MODE					
V_{INH}	-	3.5	-	-	V
V_{INH}	-	-	-	1.5	V
I_{INH}	-	-	50	200	µA
I_{INL}	-	-	-	-1	µA
Input Capacitance [2]	-	-	5	8	pF
LOGIC OUTPUTS					
DB0-DB7, $\overline{OFL}$, $\overline{INT}$					
V_{OH}	I_{SOURCE} = 360µA	4	-	-	V
V_{OL}	I_{SINK} = 1.6mA	-	-	0.4	V
I_{OUT}(DB0-DB7)	Floating State Leakage	-	-	±3	µA
Output Capacitance [2]	-	-	5	8	pF
RDY					
V_{OL}	I_{SINK} = 2.6mA	-	-	0.4	V
I_{OUT}	Floating State Leakage	-	-	±3	V
Output Capacitance	-	-	5	8	pF
SLEW RATE, TRACKING [2]	-	-	0.2	0.1	V/µs
POWER SUPPLY					
V_{DD}	±5% for specified performance	-	-	5	V
I_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0V	-	-	20	mA
Power Dissipation	-	-	40	-	mW
Power Supply Sensitivity		V_{DD} = 5V ± 5%	±1/16	±1/4	LSB

1. Total unadjusted error includes offset, full scale and linearity error.

2. Not tested.

TABLE 3. 7820RP AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time	t_{CSS}	0	-	-	ns
$\overline{CS}$ to RDWR Hold Time	t_{CSH}	0	-	-	ns
$\overline{CS}$ to Delay Time (Pull-up Resistor = 5kΩ)	t_{RDY}	-	-	100	ns
Conversion Time (RD Mode)	t_{CRD}	-	-	2.5	µs
Data Access time (RD Mode)	t_{ACC0}	-	-	t_{CRD} + 50	ns
$\overline{RD}$ to $\overline{INT}$ delay (RD Mode)	t_{INTH}	-	-	225	ns
Data Hold Time	t_{DH}	-	-	100	ns
Delay time between Conversions	t_P	600	-	-	ns
Write Pulse Width	t_{WR}	600	-	-	ns
				50	µs
Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}	700	-	-	ns
Data Access Time (WR-RD Mode)	t_{ACC1}	-	-	250	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{R1}	-	-	225	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	-	-	1700	ns
Data Access Time (WR-RD Mode)	t_{ACC2}	-	-	110	ns
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-alone Operation)	t_{IHWR}	-	-	150	ns
Data Access time after $\overline{INT}$ (Stand-alone Operation)	t_{ID}	-	-	75	ns

TABLE 4. 7820RP PIN DESCRIPTION

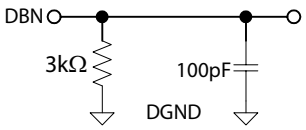
PIN NUMBER	PIN NAME	FUNCTION
1	V_{IN}	Analog Input, Range: $V_{REF}(-)$ to $V_{REF}(+)$.
2	DB0	Data Output. Three State Output, bit 0 (LSB).
3	DB1	Data Output. Three State Output, bit 1.
4	DB2	Data Output. Three State Output, bit 2.
5	DB3	Data Output. Three State Output, bit 3.
6	$\overline{WR}$/RDY	WRITE control input/READY status output.
7	Mode	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. It is internally tied to GND through a 50µA current source.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete.
10	GND	Ground.
11	$V_{REF}(-)$	Lower limit of reference span. Range: $GND \le V_{REF}(-) \le V_{REF}(+)$.
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) \le V_{REF}(+) \le V_{DD}$.
13	$\overline{CS}$	Chip Select Input. $\overline{CS}$, the decoded device address, must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.

TABLE 4. 7820RP PIN DESCRIPTION

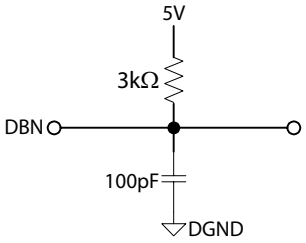
PIN NUMBER	PIN NAME	FUNCTION
14	DB4	Data Output. Three State Output, bit 4.
15	DB5	Data Output. Three State Output, bit 5.
16	DB6	Data Output. Three State Output, bit 6.
17	DB7	Data Output. Three State Output, bit 7.
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than (V_{REF}(+)-1/2LSB, $\overline{OFL}$ will be low at the end of conversion. It is a non three state output which can be used to cascade 2 or more devices to increase resolution.
19	NC	Not connected.
20	V_{DD}	Power supply voltage, +5V

TEST CIRCUITS

FIGURE 1. LOAD CIRCUITS FOR DATA ACCESS TIME TEST

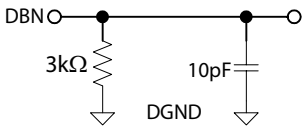


High-Z to V_{OH}

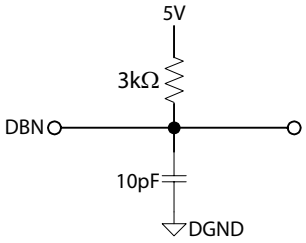


High-Z to V_{OL}

FIGURE 2. LOAD CIRCUITS FOR DATA HOLD TIME TEST

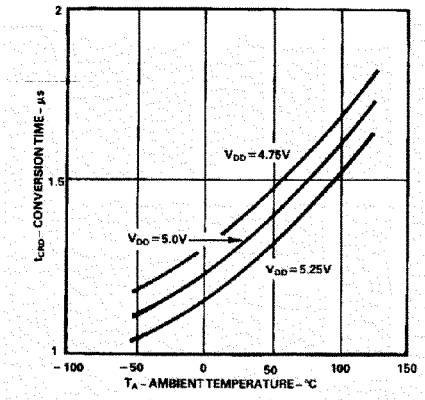


V_{OH} to High-Z

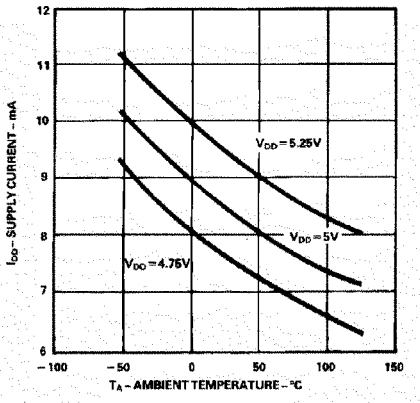


V_{OL} to High-Z

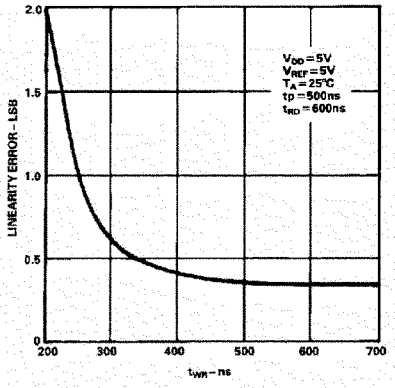
7820RP TYPICAL PERFORMANCE CHARACTERISTICS



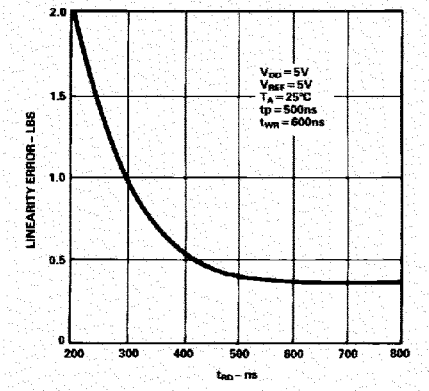
Conversion Time (RD Mode) vs. Temperature



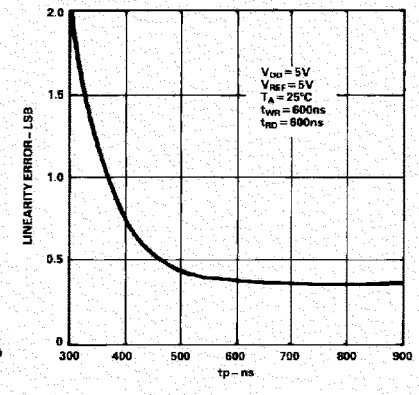
Power Supply Current vs. Temperature (not including reference ladder)



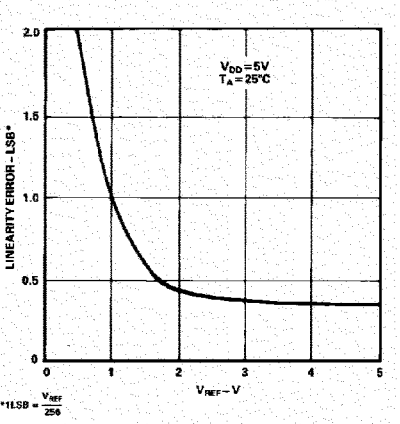
Accuracy vs. t_{WR}



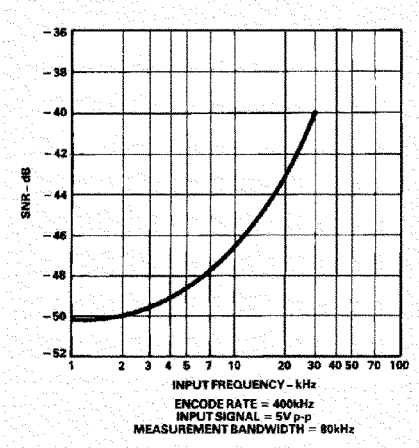
Accuracy vs. t_{RD}



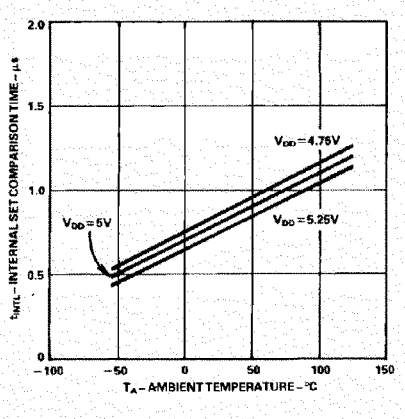
Accuracy vs. tp



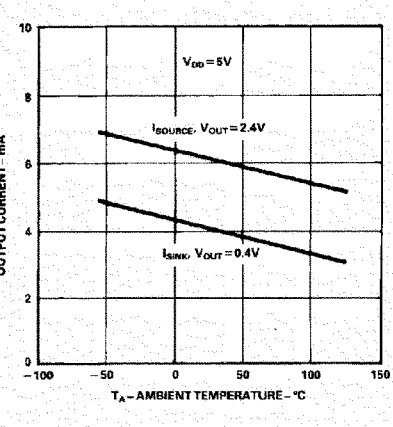
Accuracy vs V_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



Signal-Noise Ratio vs. Input Frequency



t_{INTL}, Internal Time Delay vs. Temperature



Output Current vs. Temperature

FIGURE 3. OPERATING SEQUENCE (WR-RD MODE)

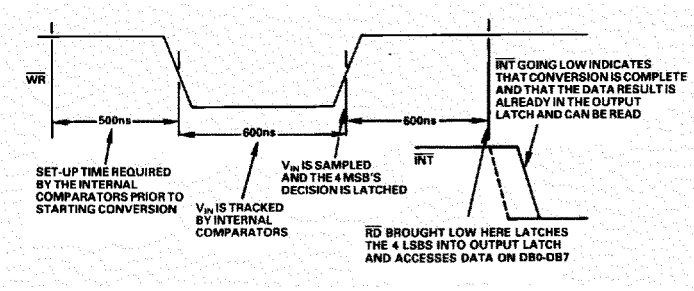


FIGURE 4. RD MODE

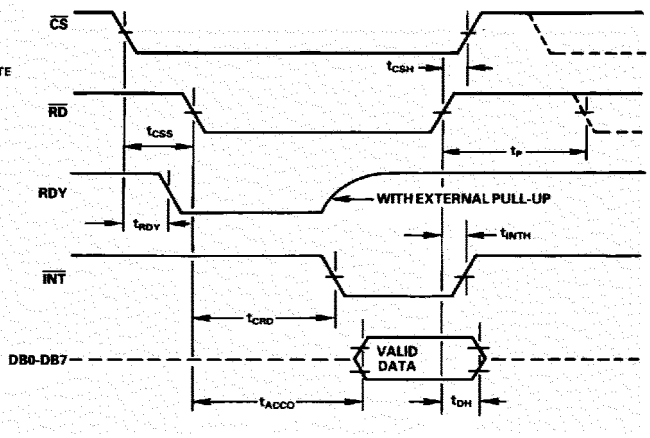


FIGURE 5. WR-RD MODE ($t_{RD}>t_{INTL}$)

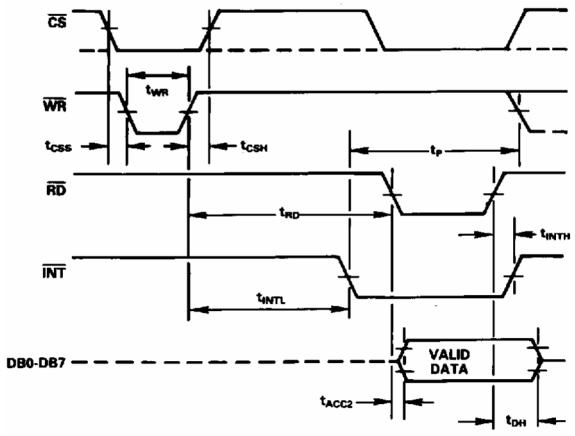


FIGURE 6. WR-RD MODE ($t_{RD}<t_{INTL}$)

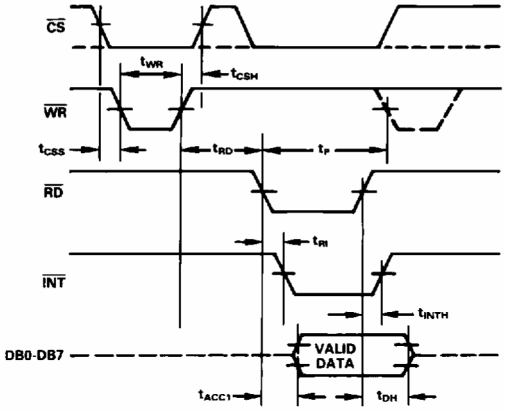


FIGURE 7. WR-RD MODE STAND-ALONE OPERATION ($\overline{CS}=\overline{RD}=0$)

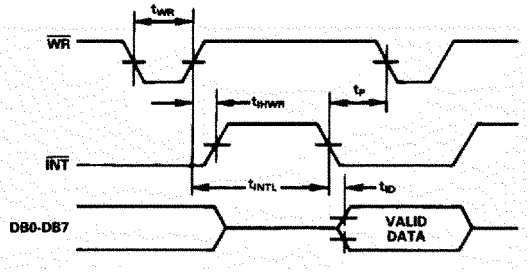


FIGURE 8. POWER SUPPLY AS REFERENCE

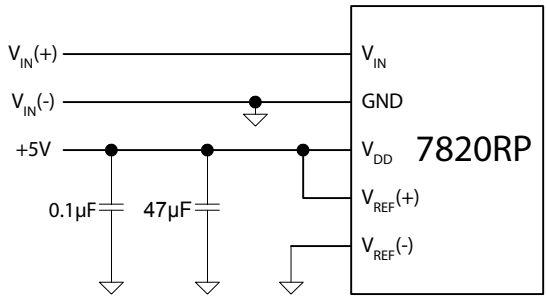


FIGURE 9. INPUT NOT REFERENCED TO GND

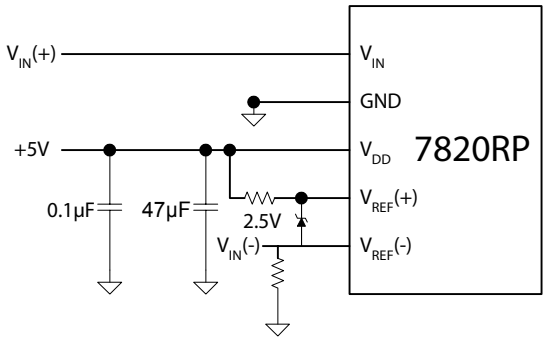


FIGURE 10. EQUIVALENT INPUT CIRCUIT

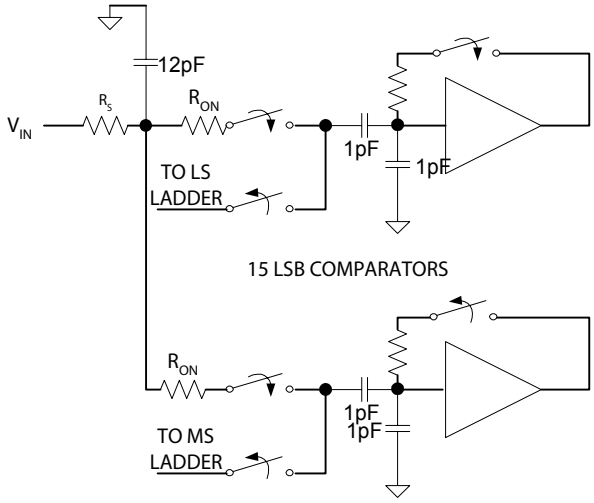


FIGURE 11. RC NETWORK MODEL