TDK SEMICONDUCTOR CORP.

78Q2124/R
Quad 10/100BASE-TX/FX Ethernet Transceiver with MII/RMII Interface

Target Specification

March 1999

DESCRIPTION

The 78Q2124 and the 78Q2124R are Quad 10/100BASE-TX/FX Ethernet transceivers designed for dual speed Fast Ethernet switch or hub applications. The transceiver includes four ENDECs, scrambler/descrambler, dual-speed clock recovery, full-featured auto-negotiation functions and four media independent interface ports. The 78Q2124 can be configured to operate with MII or RMII based controllers. The 78Q2124R is configured for RMII operation only. The 78Q2124 and the 78Q2124R are generically referred to in the following text as the 78Q2124/R except as noted.

Each of the four ports on the 78Q2124/R can interface to Category-5 unshielded twisted pair (Cat-5 UTP) cabling via 1:1 isolation transformers or to fiber-optic cabling with external fiber optic transmit and receive devices. The 10/100BASETX transmitters include on-chip pulse-shapers and a low-power line driver. Each of the receivers utilizes an adaptive equalizer and a baseline restoration circuit required for accurate clock and data recovery. The 100BASE-FX transceivers interface to 5V or 3.3V external fiber-optic devices through a PECL driver.

A dual mode interface is provided which can be configured to operate as an IEEE-802.3u compliant media independent interface (MII) or as an RMII Consortium compliant reduced media independent interface (RMII). The 78Q2124R supports RMII only and is packaged in a space-saving 128-pin TQFP package.

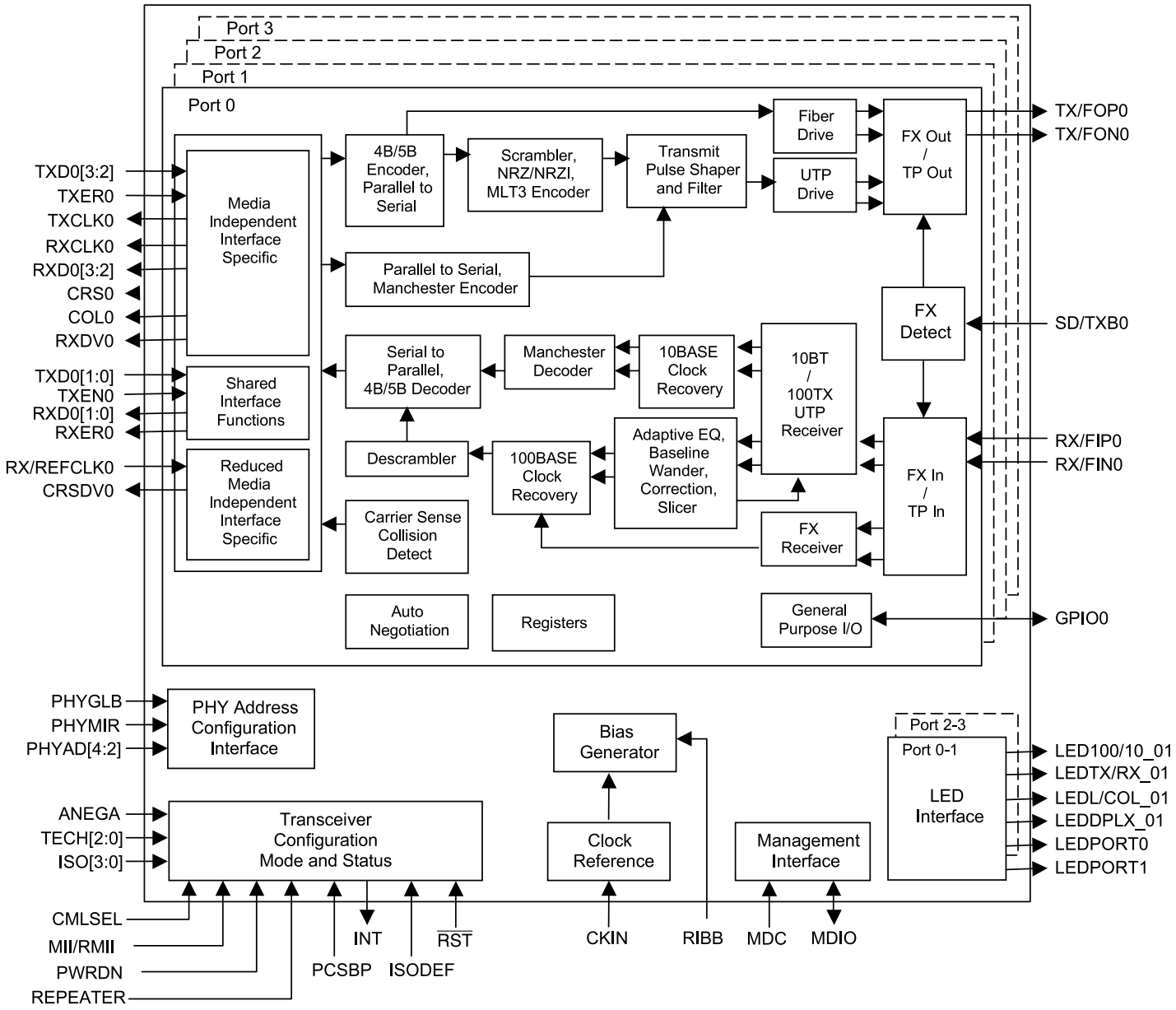
The product is fabricated in a BiCMOS process for high performance and low power operation. The 78Q2124 can operate from a single 3.3 V or 5 V supply. The 78Q2124R operates from a single 3.3V supply.

FEATURES

- **Quad 10/100BASE-TX/FX IEEE-802.3 compliant TX & RX functions on a single chip**
- **Complete 10BASE-T/100BASE-TX PCS, PMA, and PMD functions and full-featured auto-negotiation function**
- **Full duplex operation capable**
- **Dual speed clock recovery**
- **Automatic polarity correction during auto-negotiation and 10BASE-T signal reception**
- **The 78Q2124 has four Independent Interfaces configurable to operate in MII or RMII modes in a 160 Lead MQFP package**
- **The 78Q2124R has four Independent RMII ports in a 128 Lead TQFP package**
- **Up to 7 operational states conveyed on 4 LED indicators per port**
- **User programmable Interrupt pin**
- **General Purpose I/O provided per port**
- **Continuous time analog filtering facilitates FCC conformance**
- **PHY Address Mirror feature simplifies board layout**
- **Resistor-less LED design feature**
- **Individual port power-saving and power-down modes provide low power 10/100BASE-TX/FX operation**

78Q2124/R
Quad 10/100BASE-TX/FX Ethernet Transceiver with MII/RMII Interface

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

GENERAL

The following descriptions apply to both the 78Q2124 and the 78Q2124R except as noted. The device description that follows generically references the 78Q2124/R. In the following documentation, the terms “per port” and “global” are frequently used. The term “per port” refers to a function that is controllable for each port and “global” refers to a function that controls all of the ports when it is enabled.

Supply Voltage

The 78Q2124 can operate from either a single 3.3V (± 0.3V) or 5.0V (± 0.5V) power supply. The chip automatically adapts to the supply voltage used without a change to the external configuration.

The 78Q2124R operates from a single 3.3V (± 0.3V) power supply.

Power Management

The 78Q2124/R has four power saving modes:

- Chip Power-Down
- Receive Power Management
- Transmit High Impedance Mode
- CML PECL

Port power-down is activated by setting the per port PWRDN bit in the register (MR0.11). Pulling high the global PWRDN pin will power down all four ports. When the chip is in power-down mode, all on-chip circuitry is shut off, and the device consumes minimum power. While in power-down state, the 78Q2124/R will still respond to management transactions.

Per port receive power management (RXCC mode) is activated by setting the RXCC bit in the register (MR16.0). In this mode of operation, the adaptive equalizer, the clock recovery phase lock loop (PLL), and all other receive circuitry will be powered down when no valid signal is present at the UTP receive line interface. As soon as a valid signal is detected, all circuits will automatically be powered up to resume normal operation. During this mode of operation, RX/REFCLK will be inactive when there is no data being received. Note that the RXCC mode is not supported during 10BASE-T operation or in RMII mode.

Per port transmit high impedance mode is activated by setting the TXHIM bit in the MII register (MR16.12). In this mode of operation, the transmit UTP drivers are in a high impedance state and in MII mode the TXCLKn pins are tri-stated. The receive circuitry remains fully operational. The default state of MR16.12 is a logic low for disabling the transmit high impedance mode. Only a reset condition will automatically clear MR16.12. The transmitter is fully functional when MR16.12 is cleared.

CML PECL mode is enabled by setting the CMLSEL pin. This feature, which can be activated in fiber mode only, changes the standard emitter coupled PECL output to a current driven, low power CML output. This output mode requires less than half of the current used by conventional 50 ohm terminated PECL.

Analog Biasing

The 78Q2124/R uses the reference clock and an external resistor to generate accurate bias voltages for the chip.

Clock

An externally generated 25MHz ±100ppm clock is connected to the CKIN pin when the 78Q2124 is in MII mode. The 78Q2124, in RMII mode, and the 78Q2124R use the per port RMII input, RX/REFCLKn, as its clock source. In this mode the clock provided on RX/REFCLKn must be 50MHz +/- 50ppm. RX/REFCLKn is provided as a per port connection to minimize data skew for large configurations. CKIN is not used in RMII mode and must be left unconnected.

Transmit Clock Generation

The transmitter uses an on-chip frequency synthesizer to generate the transmit clock. In 100BASE-TX/FX, MII operation, the synthesizer multiplies the reference clock by 5 to obtain the internal 125MHz serial transmit clock. In 10BASE-T mode, it generates an internal 20MHz transmit clock by multiplying the reference 25MHz clock by 4/5. In RMII mode the 50MHz reference clock is multiplied by 5/2 and 2/5 to achieve the internal clock frequencies for 100BASE-TX/FX and 10BASE-T operation respectively.

Receive Signal Qualification

The integrated signal qualifier has separate squelch and un-squelch thresholds, and includes a built-in timer to ensure fast and accurate signal detection and receive noise rejection. Upon detection of two or more valid 10BASE-T or 100BASE-TX pulses on the line receive port, the *pass* indication, indicating the presence of valid receive signals or data, will be asserted. When *pass* is asserted, the signal detect

threshold is lowered by about 60%, and all adaptive circuits are released from their quiescent operating conditions, allowing them to lock onto the incoming data. In 100BASE-TX operation, *pass* will be de-asserted when no signal is presented for a period of about 1.2us. In 10BASE-T operation, *pass* will be de-asserted whenever no Manchester data is received. In either case, the signal detect threshold will return to the squelched level whenever the *pass* indication is de-asserted. The *pass* signal is used internally to control the operation of the receive clock recovery.

Receive Clock Recovery

In 100BASE-TX mode, the 125MHz receive clock is extracted using a narrow-band PLL. When no receive signal is present, the PLL is directed to lock onto the transmit 125 MHz clock. When *pass* is asserted, the PLL will use the received NRZI signal as the clock reference. The recovered clock is used to re-time the data signal and for conversion of the data to NRZ format.

In 10BASE-T mode, the 10MHz clock is recovered using a PLL. For fast acquisition, the receive PLL is locked onto the transmit reference clock during idle receive periods. When Manchester-coded preambles are detected, the PLL adjusts its phase and re-synchronizes with the incoming Manchester data.

100BASE-TX OPERATION

100BASE-TX General

100BASE-TX ability is selected through the use of the TECH pins as well as the per port SD/TXBn pins. Setting TECH1 allows 100BASE-TX capability to be advertised when autonegotiation is enabled and allows 100BASE-TX technology to be selected through the control register when autonegotiation is not enabled. SD/TXBn is a per port select for either 100BASE-TX or 100BASE-FX technology. 100BASE-TX is selected for a given port when this pin is pulled low.

100BASE-TX Transmit

The 78Q2124 and the 78Q2124R contains all of the necessary circuitry to convert the transmit signaling from a controlling MAC to an IEEE-802.3u compliant data-stream driving Cat-5 UTP cabling. The 78Q2124's internal PCS interface maps 4 bit nibbles from the MII to 5 bit code groups as defined in table 24-1 of IEEE-802.3. The 78Q2124/R in RMII mode performs the same mapping following two, 2 bit deserializers. The 5 bit code groups are then scrambled and converted to a serial stream before being sent to the MLT-3 pulse shaping circuitry and line driver. The seeding data for the scramblers are set using the 5 bit PHYAD data. This reduces the level of radiated emissions from the part, easing FCC conformance. The pulse-shaper uses current modulation to produce the desired output waveform. Controlled rise/fall time in MLT-3 signal is achieved using an accurately controlled C/I filter. The line driver requires an external 1:1 isolation transformer to interface with the line media. The center-tap of the primary side of the transformer should be connected to Vcc.

100BASE-TX Receive

The 78Q2124/R receives a 125MBaud MLT-3 signal through a 1:1 transformer. The signal then goes through a combination of adaptive offset adjustment (baseline wander correction) and adaptive equalization. The effect of these circuits is to sense the amount of dispersion and attenuation caused by the cable and transformer, and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The 78Q2124/R can recover up to a 10dB of loss in signal amplitude at 16 MHz. This loss is represented as test-chan 5 in Annex A of the ANSI X3.263:199X specification and corresponds to approximately 140m of Cat-5 UTP cabling. The equalized MLT-3 data signal is sliced and the resulting bit-stream is presented to the clock recovery PLL and to a serial to parallel converter. The parallel data from the converter is then descrambled and aligned into 5 bit code groups. The receive PCS interface maps these code groups to 4 bit data for the MII as outlined in table 24-1 in Clause 24 of IEEE-802.3. When in RMII mode, this 4 bit data is presented to an elasticity buffer before being clocked out on the RMII.

PCS Bypass Mode

The Global PCS Bypass mode is entered by pulling the PCSBP pin high. Per port PCS Bypass mode is entered by setting register bit MR 16.1. In PCS Bypass mode the 78Q2124/R accepts scrambled 5 bit code into the pins TXERn and TXDn[3:0]. TXERn is the MSB data input. The 5 bit code groups are converted to an MLT-3 signal.

The received MLT-3 signal is converted to 5 bit NRZ code groups and output from the RXERn and RXDn[3:0] pins. The RXERn pin is the MSB data output. The RXDVn and TXENn pins are unused in PCS Bypass mode.

PCS bypass is not available in RMII mode.

100BASE-FX OPERATION

100BASE-FX General

The 78Q2124/R can interface to both 3.3V and 5V external fiber-optic devices through a PECL driver and receiver. In this mode of operation there are two PECL inputs and one PECL output. The same ports used for 100BASE-TX transmit and receive are used for 100BASE-FX transmit and receive. Signal Detect from the external fiber-optic device is applied to the SD/TXBn pin.

A low power PECL mode is enabled when the CMLSEL pin is set. In this mode the TX/FOP and TX/FON pins sink a differential current through external load resistors. This mode uses less than half of the current required by conventional PECL using 50 ohm equivalent termination. When CMLSEL is low, conventional PECL drivers are enabled. VPE must be tied to the same potential used by the external fiber-optic device. The 78Q2124/R is allowed to operate in three of the four possible combinations of 3.3V and 5V applied to the fiber-optic driver (and VPE) and the 78Q2124/R. The supply configuration not allowed is the case where VPE is set to a lower voltage than VCC. Typical applications are shown in Figure 1.

100BASE-FX Enable/Signal Detect

100BASE-FX ability is selected through the use of the per port SD/TXBn pin. When this mode is selected a number of changes are implemented on the selected port/s:

- The scrambler/descrambler is bypassed
- Autonegotiation is disabled
- 100BASE-TX and 10BASE-T are disabled

SD/TXBn is a single ended, dual function input. 100BASE-TX is selected for a given port when SD/TXBn is pulled low or left unconnected. 100BASE-FX is enabled when a valid PECL signal is applied to this pin. The PECL logic levels are referenced with respect to the potential on the VPE supply pin. The VPE supply pin must be tied to the supply of the external fiber-optic driver. Each of the VPE supply pins must be tied to the same potential. The SD/TXB pin has an internal pulldown current. This pin is connected to the signal detect output of the external fiber-optic device. This pin, when left unterminated in 100BASE-FX mode, will yield typical current savings of 5mA/20mA per port when in the PECL low/high state. This input's speed is not critical in 100BASE-FX applications and therefore conventional PECL terminations are not required. A resistive termination may be added if desired.

100BASE-FX Transmit

The 78Q2124/R contains all of the necessary circuitry to convert the transmit MII or RMII signaling from a controlling MAC to an NRZI serial differential PECL signal used to drive an external fiber-optic driver. The internal PCS interface maps 4 bit nibbles from the MII to 5 bit code groups as defined in table 24-1 of IEEE-802.3. In RMII mode this mapping occurs following two, 2 bit deserializers. The scrambler used in 100BASE-TX mode is bypassed in 100BASE-FX mode. The 5 bit data is serialized, converted to NRZI, and is then sent to the PECL output driver. .

The PECL driver is capable of interfacing to both 3.3V and 5V external fiber-optic drivers. The VPE supply pin must be tied to the supply of the external fiber-optic driver. The state of the CMLSEL pin will determine the method of termination on the TX/FOP and TX/FON pins. CMLSEL, as discussed in the 100BASE-FX General section, provides a low power output drive that will result in a reduction of supply current.

100BASE-FX Receive

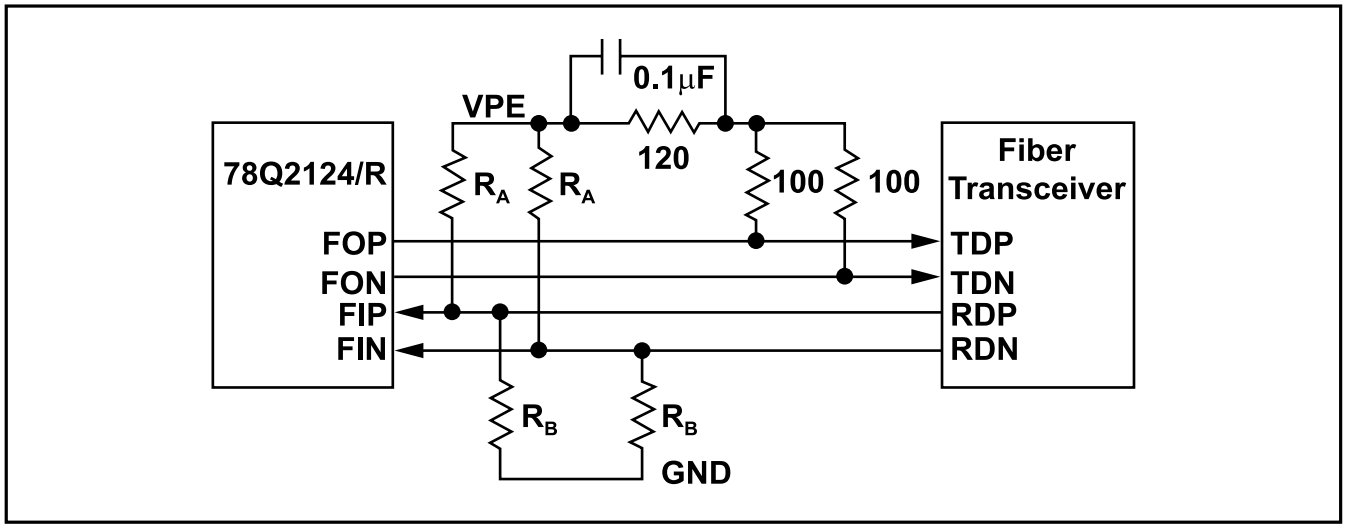
The 78Q2124/R receives a serial differential PECL signal from an external fiber-optic device. The signal is sliced and the resulting bit-stream is presented to the clock recovery PLL and to a serial to parallel converter. In this mode of operation the parallel data from the converter bypasses the 100BASE-TX descrambler. In the 78Q2124 data is aligned into 5 bit code groups and mapped to 4 bit data for the MII as outlined in table 24-1 in Clause 24 of IEEE-802.3. In the 78Q2124R and the 78Q2124 (when in RMII mode) data is aligned into 5 bit code groups, mapped to 4 bit data and presented to an elasticity buffer before being clocked out on the RMII.

The potential present on the VPE supply pin is used to establish the logic levels for the incoming PECL signal and hence must be tied to the same potential used by the external fiber-optic driver.

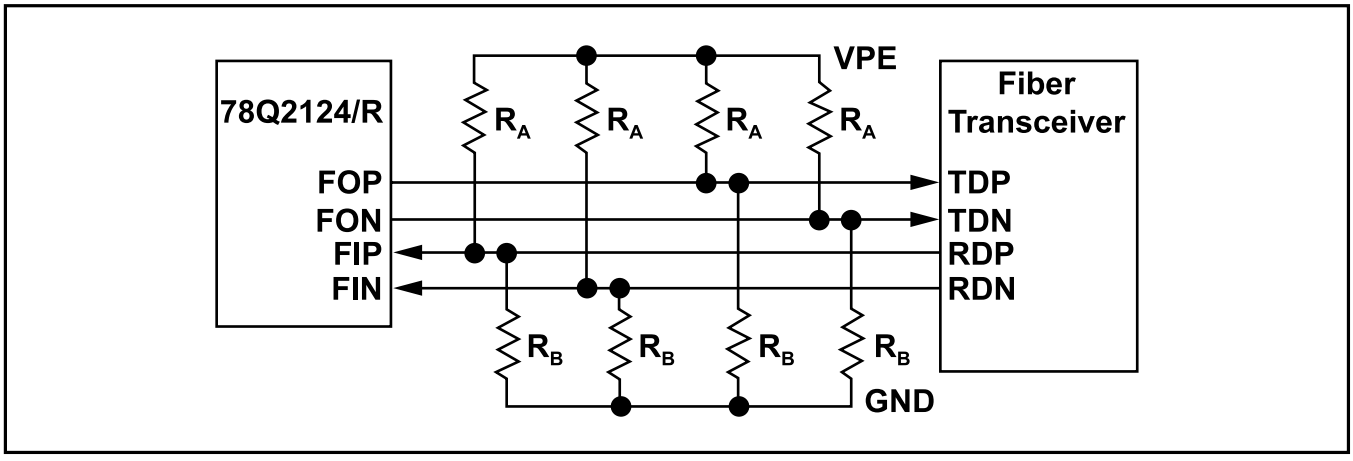
Table 1

CMLSEL	VPE	Vcc	Allowed Termination	Z_L = 50 ohm (R_A/R_B)	Z_L = 100 ohm (R_A/R_B)
0	3.3V	3.3V	Case B, (Case C or D)	127/82.5	255/165
1	3.3V	3.3V	Case A, (Case C or D)	127/82.5	255/165
0	5V	5V	Case B, (Case C or D)	82.5/127	165/255
1	5V	5V	Case A, (Case C or D)	82.5/127	165/255
0	5V	3.3V	Case B, (Case C or D)	82.5/127	165/255
1	5V	3.3V	Case A, (Case C or D)	82.5/127	165/255

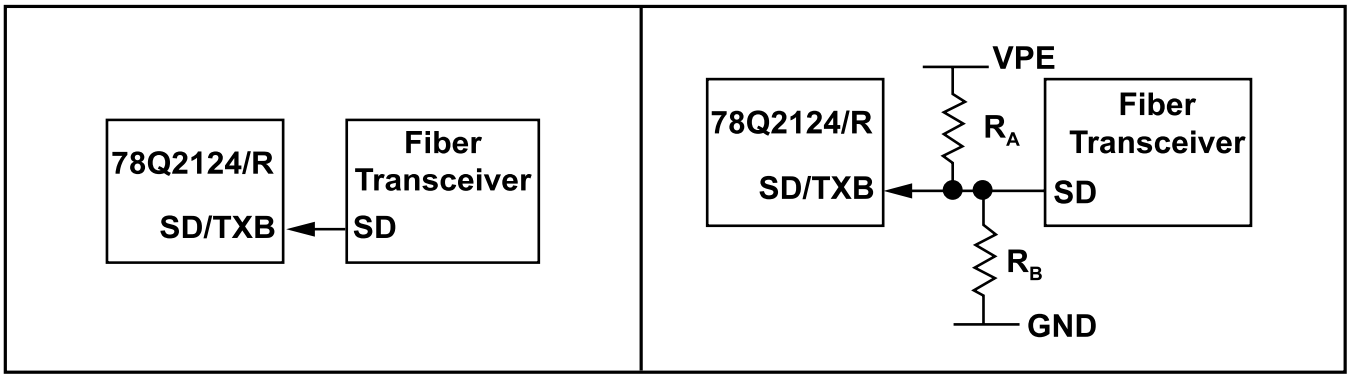
FIGURE 1: Fiber Interface Configuration



Case A



Case B



Case C Case D

10BASE-T OPERATION

10BASE-T General
SQE Test

The 78Q2124 supports the signal quality error (SQE) function detailed in IEEE-802.3. At an interval of 1µs after each negative transition of the TXENn pin in 10BASE-T mode, the COLn pin will go high for a period of 1µs. This per port function can be disabled through register bit MR16.11. This function is not supported in RMII mode.

Natural Loopback

When the 78Q2124 is transmitting and not receiving on the twisted pair media, data on the TXDn pins is looped back onto the RXDn pins. During a collision, data from the RX/FIPn and RX/FINn pins is routed to the RXDn pins. The per port natural loopback function can be enabled through register bit MR16.10. This function is disabled in full-duplex or repeater modes. This function is not supported in RMII mode.

10BASE-T Jabber

The 78Q2124/R employs an onboard timer to prevent the MAC from capturing a network through excessively long transmissions. When this timer is exceeded the chip enters the jabber state, and transmission is disabled. The jabber state is exited after the MII goes idle for 500ms ± 250ms.

Repeater Mode

When the global REPEATER pin is high the 78Q2124 is placed in repeater mode. The per port function is accessed when MR16 register bits MR 16.15 is set In this mode, full duplex operation is prohibited, CRS responds only to receive activity and, in 10BASE-T mode, the SQE test function is disabled. This mode is not available in RMII mode.

10BASE-T Transmit

The 78Q2124/R contains all of the necessary circuitry to convert the transmit MII or RMII signaling from a controlling MAC to an IEEE-802.3 compliant data-stream driving either Cat-3 or Cat-5 UTP cabling. The 78Q2124/R clocks 4 bit parallel NRZ data at 2.5MHz via the MII interface and passes it through a parallel to serial converter.

In RMII mode, 2 bit data is clocked in at 50MHz and passed through 2, 2 bit deserializers. The data on the TXDn[1:0] pins shall be valid in RMII mode such that TXDn[1:0] may be sampled every 10^{th} cycle, regardless of the starting cycle within the group and yield the correct frame data.

The data is clocked into the parallel to serial converter at 2.5MHz. The data is then passed through a Manchester encoder and then on to the twisted pair pulse shaping circuitry and the twisted pair drive circuitry. An advanced pulse shaper employs a Gm-C filter to pre-distort the output waveform to meet the output voltage template and spectral content requirements detailed in Clause 14 of IEEE-802.3. Interface to the twisted pair media is through two external 50 ohm resistors and a center-tapped 1:1 transformer; no external filtering is required. During auto-negotiation and during 10BASE-T idle periods, link pulses are transmitted.

10BASE-T Receive

The 78Q2124/R receives Manchester encoded 10BASE-T data through the twisted pair inputs and re-establishes logic levels through a slicer with a smart squelch function. The slicer automatically

adjusts its squelch level after valid data with the appropriate levels are detected. Data is passed on to the 10BASE-T PLL where the clock is recovered, data is re-timed and passed through a Manchester decoder. From here data enters the serial to parallel converter for transmission to the MAC via the media independent interface. Interface to the twisted pair media is through an external 100 ohm resistor and a 1:1 center-tapped transformer; no external filtering is required. Polarity information is detected and corrected in the internal circuitry.

Polarity Correction

The 78Q2124/R is capable of both automatic and manual polarity reversal for 10BASE-T and auto-negotiation. This per port feature is controlled by register bits MR16.5 and MR16.4. The default is automatic mode where MR16.5 is low and MR16.4 indicates if the detection circuitry has inverted the input signal. To enter manual mode, MR16.5 is set high and MR16.4 will then control the signal polarity.

AUTO-NEGOTIATION

The 78Q2124/R supports the auto-negotiation functions of Clause 28 of IEEE-802.3u. This function can be enabled via a pin strap to the device or through registers. The ANEGA pin is global; its setting affects the operation of all four ports. If the global ANEGA pin is tied high, the auto-negotiation function defaults to on and the per port bit MR0.12, is high after reset. Software can disable the auto-negotiation function by writing to bit MR0.12 If the ANEGA pin is tied low the function defaults to off and bit MR0.12 is set low after reset and cannot be written to.

The contents of register MR4 are sent to the 78Q2124/R's link partner during auto-negotiation, coded in fast link pulses. Per port bits MR4.8:5 reflect the state of the TECH[2:0] pins after reset. The TECH pins configure the allowed modes of operation of the 78Q2124/R. The TECH pins are global; their setting affects the operation of all four ports. TECH2 controls the duplex configuration, TECH1 the 100BASE-TX capability and TECH0 the 10BASE-T capability. If TECH[2:0] = 111, then all 4 MR4.8:5 bits are high. If TECH[2:0] = 001, then only bit 5 is high. After reset, software can change any of these bits from a 1 to a 0; but not from a 0 to a 1. Therefore, a technology permitted by the setting of the TECH pins can be disabled, but one not permitted cannot be enabled.

With auto-negotiation enabled, the 78Q2124/R will start sending fast link pulses at power on, loss of link or a command to restart. At the same time it will look for either 10BASE-T idle, 100BASE-TX idle or fast link pulses from its link partner. If either idle pattern is detected, the 78Q2124/R will configure itself in half-duplex mode at the appropriate speed. If it detects fast link pulses, it decodes and analyzes the link code transmitted by the link partner. When three identical link code words are received (ignoring the acknowledge bit) the link code word is stored in register 5. Upon receiving three more identical link code words, with the acknowledge bit set, the 78Q2124/R configures itself to the highest priority technology common to the two link partners. The technology priorities are, in descending order:

100BASE-TX, Full Duplex
100BASE-TX, Half Duplex
10BASE-T, Full Duplex
10BASE-T, Half Duplex

Once auto-negotiation is complete, register bits MR18.11:10 will reflect the actual speed and duplex that was chosen.

If auto-negotiation fails to establish a link for any reason, register bit MR18.12 will reflect this and auto negotiation will restart from the beginning. Writing a one to per port bit MR0.9, RANEG, will also cause auto-negotiation to restart.

MEDIA INDEPENDENT INTERFACE

General

The 78Q2124R is hardwired to only interface to a RMII compatible MAC. The 78Q2124 is capable of interfacing to both RMII and MII Interfaces. The MII/RMII pin on the 78Q2124 controls the interface that is selected. When this pin is set, the MII interface is selected. RMII is selected when this pin is pulled low.

MII Transmit and Receive Operation

The 78Q2124 provides four independent MII interfaces. This allows each port to operate in a configuration independent from that of an adjacent port allowing switch applications. The MII interface is capable of both 10Mb/s and 100Mb/s data rates as described in Clause 22 of the IEEE-802.3u standard.

The transmit clock, TXCLKn, provides the timing reference for the transfer of TXENn, TXDn[3:0], and TXERn signals from the MAC to the 78Q2124/R. TXDn[3:0] is captured on the rising edge of TXCLKn

when TXENn is asserted. TXERn is also captured on the rising edge of TXCLKn and is asserted by the MAC to request that an error code group be transmitted. The assertion of TXERn has no affect when the 78Q2124 is operating in 10BASE-T mode.

The receive clock, RX/REFCLKn, provides the timing reference to transfer RXDVn, RXDn[3:0], and RXERn signals from the 78Q2124 to the MAC. RXDVn transitions synchronously with respect to RXCLKn and is asserted when the 78Q2124/R is presenting valid data on RXDn[3:0]. RXERn is asserted when a code group violation has been detected in the current receive packet and is also synchronous to RXCLKn.

REDUCED MII

RMII General

The RMI Interface on the 78Q2124/R is fully compliant with the Rev 1.2 RMII Specification published by the RMII Consortium. The intent of the RMII is to provide a reduced pin count alternative to the IEEE 802.3u MII. The RMII uses 8 pins per port while the MII requires 16. The RMII uses 2 bits for transmit and two bits for receive. There is a Transmit Enable, a Receive Error, a Carrier Sense, and a 50MHz Reference Clock. The reference clock is provided on a per port basis to minimize clock to data skew in large configurations.

RMII Transmit and Receive Operation

The 78Q2124/R uses the same signals internally for both the RMII and the MII. The RMII simply maps these signals in a more pin efficient manner. The transmit and receive bits are converted from a 4 bit parallel format to a 2 bit parallel scheme which is clocked at twice the rate. CRS and RXDV are combined into a signal called CRSDV. This signal contains information concerning Carrier Sense, FIFO status, and validity of the data. TXER and COL are not used in RMII mode. The following Table 2 shows the signals present in MII and RMII configurations and the pin name for the signal on the 78Q2124/R.

The 78Q2124/R provides four independent RMII interfaces. This lets each port to operate in a configuration independent from that of an adjacent port allowing switch applications. The RMII interface is capable of both 10Mb/s and 100Mb/s data rates as described in Clause 22 of the IEEE-802.3u standard.

Pin Name	MII Signal	RMII Signal
TXERn	TXER	
TXD3n	TXD3	
TXD2n	TXD2	
TXD1n	TXD1	TXD1
TXD0n	TXD0	TXD0
TXENn	TXEN	TXEN
COLn	COL	
RXD3n	RXD3	
RXD2n	RXD2	
RXD1n	RXD1	RXD1
RXD0n	RXD0	RXD0
RXERn	RXER	RXER
RX/REFCLKn	RXCLK	REFCLK
RXDVn	RXDV	
CRS/CRSDV	CRS	CRSDV

Table 2. MII / RMII Signal Mapping

Station Management Interface

The station management interface consists of circuitry which implements the serial protocol as described in Clause 22.2.4.4 of IEEE-802.3u. There is no difference in this interface between the serial protocol between the MII and RMII modes. A 16-bit shift register receives serial data applied to the MDIO pin at the rising edge of the MDC clock signal. Once the preamble is received, the station management control logic looks for the start-of-frame sequence and a read or write op-code, followed by the PHYAD and REGAD fields. For a read operation, the MDIO port becomes enabled as an output and the register data is loaded into a shift register for transmission. The 78Q2124/R can work with a one bit preamble rather than the 32 bits proscribed by IEEE-802.3. This allows for faster programming of the registers. If a register does not exist at an address indicated by the REGAD field or if the PHYAD field does not match the 78Q2124/R PHYAD indicated by the PHYAD pins, a read of the MDIO port will return all ones. For a write operation, the data is shifted in and loaded into the appropriate register after the sixteenth data bit has been received. Writes to registers not supported by the 78Q2124/R are ignored.

The 3 PHYAD pins, PHYAD(4:2) set the upper three bits of the PHY address. The two LSB of the 5 bit PHYAD detailed in section 22 of the IEEE 802.3u standard are set internally.

PHY Address Mirror

The 78Q2124/R provides a PHYAD control pin, PHYMIR, which controls the mapping of the PHYAD pins. This pin eases the task of using this chip in applications where an alternate PHY or switch IC maps its ports in a different order to the external pins. The state of the pin's setting can be read in MR16.9. Table 3 details the mapping of the two LSB of the 5 bit PHY address:

PHYMIR	PHYAD1	PHYAD0	PORT
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

Table 3. PHY Address Internal Mapping

PHY Global Addressing

The 78Q2124/R provides a PHYAD control pin, PHYGLB, which controls the ability to address all of the ports available given the 5 bit PHYAD address. Section 22 of the IEEE 802.3u standard mandates that a PHYAD[4:0] setting of 00000 is a global broadcast, that is, data written to this address will affect all of the ports to which a given MDIO serial interface line is connected. Given this constraint, when PHYAD[4:2] is set to 000 with PHYMIR pulled low, port 0 is not addressable by itself. To address port 0 a global port write must first be implemented followed by port specific writes to port 1, 2, and 3 to change their configurations back to what they were previous to the global addressing. The same is true with port 3 when PHYMIR is set. When PHYGLB is set, the 78Q2124/R operates in manner proscribed by section 22 of the IEEE 802.3u standard. When PHYGLB is pulled low, port 0 (or port 3, if PHYMIR is set) is addressable by itself, independent from any other port sharing the MDIO serial interface.

The PHYGLB feature can also be implemented with a write to read/write register bit MR16.8. Setting this bit in any of the four ports will cause the 78Q2124/R to enter the global address mode. To disable global addressing, the specific port where the bit was set needs to be cleared. Following reset this bit, for all 4 ports, will reflect the setting of the PHYGLB pin.

This feature is useful in applications where a global configuration is desired following power-up and port specific configurations are required in subsequent operation.

ADDITIONAL FEATURES

LED Indicators

The LEDs are used to display Transmit, Receive, 10Mbit/s Rate Selected, 100Mbit/s Rate Selected, Duplex, Collision, and Link data.

The LEDs are connected by a multiplexed bus arrangement. Since these LEDs are driven by a duty cycle-modulated current source, no external resistors are required.

Figure 2 shows a typical connection for the LEDs.

General Purpose I/O Interface

The 78Q2124/R has a one pin, bi-directional, general purpose interface per port that can be used for external control or to monitor external signals.

The direction of this pin and data that is either driven or read from these pins is configured via bit MR16.7 and MR16.6 as detailed in the Vendor Specific Register description of MR16.

Interrupt Pin

The 78Q2124/R has a global Interrupt pin (INTR) that is asserted whenever any of the eight per port interrupt bits of MR17.7:0 are set. This interrupt bit can be disabled via MR17.15:8 Interrupt Enable bits. The active level of the INTR pin is controlled by the Interrupt Level bit, MR16.14. This bit is ORed between each of the four ports. That is, setting MR16.14 high in one port's register will affect the operation of all other ports. When the INTR pin is not asserted, the pin is held in a high impedance state.

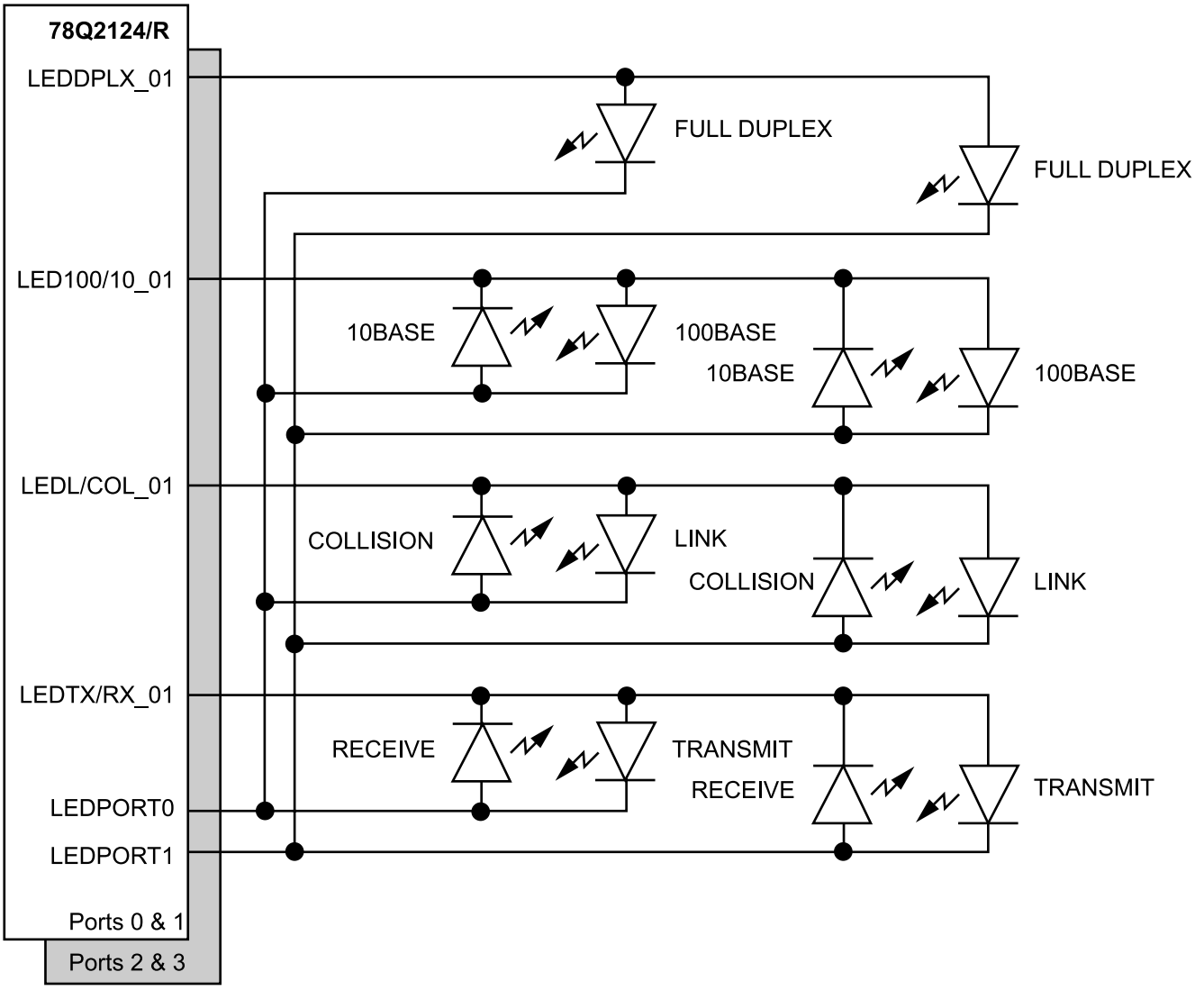


FIGURE 2: LED Connectivity

160 MQFP / 128 TQFP PIN DESCRIPTION

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
A	Analog Pin	I	Digital Input
O	Digital Output	I/O	Digital Bi-directional Pin
S	Supply	OZ	Tri-stateable digital output

R/MII (REDUCED / MEDIA INDEPENDENT INTERFACE)

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
TXCLK0 TXCLK1 TXCLK2 TXCLK3	29 49 73 93		OZ	TRANSMIT CLOCK: - TXCLKn is a continuous clock which provides a timing reference for the TXENn, TXERn and TXDn[3:0] signals from the MAC. The clock frequency is 25MHz in 100BASE-TX mode and 2.5MHz in 10BASE-T mode. This pin is tri-stated in isolate mode. This pin is not used in RMII mode.
TXEN0 TXEN1 TXEN2 TXEN3	30 50 74 94	29 41 57 69	I	TRANSMIT ENABLE: - TXENn is asserted by the MAC to indicate that valid data for transmission is present on the TXDn[3:0] pins in MII mode and on TXDn[1:0] in RMII mode.
TXD0[3:2] TXD0[1:0] TXD1[3:2] TXD1[1:0] TXD2[3:2] TXD2[1:0] TXD3[3:2] TXD3[1:0]	[34:33] [32:31] [54:53] [52:51] [78:77] [76:75] [98:97] [96:95]	 [31:30] [43:42] [59:58] [71:70]	I	TRANSMIT DATA: - In MII mode, TXDn[3:0] receives data from the MAC for transmission on a nibble basis. This data is captured on the rising edge of TXCLK when TXENn is high. - In RMII mode, TXDn[1:0] receives 2 bit wide data from the MAC for transmission. TXDn[3:2] is not used in RMII mode. Details on the specifics of this signal are available in the RMII Specification Revision 1.2.
TXER0 TXER1 TXER2 TXER3	28 48 72 92		I	TRANSMIT ERROR: - TXERn is asserted high to request that an error code-group be transmitted when TXENn is high. In PCS bypass mode this pin becomes the higher-order bit of the transmit 5-bit code group. This pin is not used in RMII mode.
CRS/CRSDV0 CRS/CRSDV1 CRS/CRSDV2 CRS/CRSDV3	36 56 80 100	32 44 60 72	OZ/O	CARRIER SENSE: - In MII mode, when the 78Q2124 is not in repeater mode, CRSn is high whenever a non-idle condition exists on either the transmitter or the receiver. In repeater mode, CRSn is only active when a non-idle condition exists on the receiver. This pin is tri-stated in isolate mode. - In RMII mode CRSDVn is active when a non-idle condition exists on the receiver. Loss of carrier shall result in the de-assertion of this signal. This signal is also conveys the occurrence of a false carrier event. Details on the specifics of this signal are available in the RMII Specification Revision 1.2.

R/MII (continued)

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
COL0 COL1 COL2 COL3	35 55 79 99		OZ	COLLISION: - COLn is asserted high when a collision has been detected on the media. In 10BASE-T mode COLn is also used for the SQE test function. This pin is tri-stated in isolate mode. This pin is not used in RMII mode.
RX/REFCLK0 RX/REFCLK1 RX/REFCLK2 RX/REFCLK3	26 46 70 90	27 39 55 67	OZ/I	RECEIVE CLOCK: - In MII mode, RXCLKn is a continuous clock which provides a timing reference to the MAC for the RXDVn, RXERn and RXDn[3:0] signals. The clock frequency is 25MHz in 100BASE-TX mode and 2.5MHz in 10BASE-T mode. This output pin is tri-stated in isolate mode. - In RMII mode, REFCLKn is an input used to clock in TXDn[1:0], CRSDVn, and TXENn. It is used to clock out RXDn[1:0] and RXER. Details on the specifics of this signal are available in the RMII Specification Revision 1.2.
RXDV0 RXDV1 RXDV2 RXDV3	25 45 69 89		OZ	RECEIVE DATA VALID: - RXDVn is asserted high to indicate that valid data is present on the RXDn[3:0] pins. In 100BASE-TX mode, it transitions high with the first nibble of preamble and is pulled low when the last data nibble has been received. In 10BASE-T mode it transitions high when the start-of-frame delimiter (SFD) is detected. This pin is tri-stated in isolate mode. This pin is not used in RMII mode.
RXD0[3:2] RXD0[1:0] RXD1[3:2] RXD1[1:0] RXD2[3:2] RXD2[1:0] RXD5[3:2] RXD3[1:0]	[21:22] [23:24] [41:42] [43:44] [65:66] [67:68] [85:86] [87:88]	 [25:26] [37:38] [53:54] [65:66]	OZ/O	RECEIVE DATA: - In MII mode, data received from the media is provided to the MAC via RXDn[3:0]. These pins are tri-stated in isolate mode. - In RMII mode, data received from the media is provided to the MAC via RXDn[1:0]. RXDn[3:2] is not used in RMII mode. Details on the specifics of this signal are available in the RMII Specification Revision 1.2.
RXER0 RXER1 RXER2 RXER3	27 47 71 91	28 40 56 68	OZ	RECEIVE ERROR: - RXERn is asserted high when an error is detected during frame reception for both MII and RMII modes. - In MII mode only this pin becomes the higher-order bit of the receive 5-bit code group when placed PCS bypass mode. This pin is tri-stated in isolate mode.
MDC	63	51	I	MANAGEMENT DATA CLOCK: - MDC is the clock used for transferring data via the MDIO pin.
MDIO	62	50	I/O	MANAGEMENT DATA INPUT/OUTPUT: - MDIO is a bi-directional port used to access management registers within the 78Q2124/R. This pin requires an external pull-up resistor as specified in IEEE-802.3u.

PHY ADDRESS

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
PHYMIR	116	90	I	PHY ADDRESS MIRROR CONTROL: - PHYMIR controls the internal mapping of the 2 LSB PHYAD bits as described by Table 2. The pin's setting is readable in MR16.9
PHYGLB	115	89	I	PHY GLOBAL ADDRESS: - PHYGLB when set allows the global broadcast address of 00000 to address all ports as proscribed by section 22 of the IEEE 802.3u standard. In this setting only 31 of the 32 possible ports are uniquely addressable. - When PHYGLB is pulled low, port 0 (or port 3, if PHYMIR is set) is addressable by itself, independent from any other port sharing the MDIO serial interface. In this setting all 32 of the 32 possible ports are uniquely addressable. - The PHYGLB feature can be implemented with a write to read/write register bit MR16.8. Setting this bit in any of the four ports will cause the 78Q2124/R to enter the global address mode. To disable global addressing, the specific port where the bit was set needs to be cleared. Following reset this bit, for all 4 ports, will reflect the setting of the PHYGLB pin.
PHYAD4 PHYAD3 PHYAD2	112 113 114	86 87 88	I	PHY ADDRESS: - Allows 32 configurable PHY addresses. PHYAD[1:0] are set internally in the manner described by Table 2.

PMA (PHYSICAL MEDIA ATTACHMENT) INTERFACE

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
PCSBP	159		I	PCS BYPASS: - When high, the 100BASE-TX PCS is bypassed, as well as the scrambler and descrambler functions. Scrambled 5-bit code groups for transmission are applied to the TXERn, TXDn[3:0] pins and received on the RXERn, RXDn[3:0] pins. The RXDVn and TXENn signals are not valid in this mode. PCS bypass mode is only valid when 100BASE-TX is enabled. This mode can also be entered with a write to any of the MR16 register bits MR16.1. This pin is not used in RMII mode.

CONTROL AND STATUS

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
$\overline{RST}$	8	10	I	$\overline{RESET}$: $\overline{RST}$, when pulled low, resets the chip. There are 2 other ways to reset the chip: through the internal power-on-reset (activated when the chip is being powered up) through the per port MII register bit (MR 0.15)
PWRDN	7	9	I	POWER-DOWN: - PWRDN is a global pin that when set, places the 78Q2124/R in a low power consumption state by setting this signal to logic high. While in power-down state, the 78Q2124/R still responds to management transactions. The same power-down state can also be achieved through the per port PWRDN bit in the MII register (MR0.11).
ANEGA	120	94	I	AUTO-NEGOTIATION ABILITY: Strapped to logic high to allow auto-negotiation function. When strapped to logic low, auto-negotiation logic is disabled and manual technology selection is done through TECH[2:0]. This pin is reflected as ANEGA bit (MR1.3).
TECH2 TECH1 TECH0	117 118 119	91 92 93	I	AUTONEGOTIATION TECHNOLOGY ABILITY/SELECT: - TECH[2:0] sets the technology ability of the chip which is reflected in MR0.13,8 MR1.14:11 and MR4.12:5 for 10BASE-T and 100BASE-TX operation when Autonegotiation is enabled. - TECH[2:0] sets the default ability of the chip when Autonegotiation is disabled. This is reflected in MR0.13 and MRR0.8. When multiple technologies are selected, the 78Q2124/R will select the highest technology defined in Section 28B.3 of the IEEE 803.3u standard.
				TECH[2:0] Technology ability 000 Sets ability to both 10BASE-T and 100BASE-TX, both half and full duplex Sets 100BASE-FX default ability to half duplex 001 Sets ability to 10BASE-T, half duplex 010 Sets ability to 100BASE-TX, half duplex 011 Sets ability to both 10BASE-T and 100BASE-TX, half duplex 100 No ability advertised or enabled 101 Sets ability to 10BASE-T, both half and full duplex 110 Sets ability to 100BASE-TX, both half and full duplex 111 Sets ability to both 10BASE-T and 100BASE-TX, both half and full duplex Sets 100BASE-FX default ability to full duplex. Duplex can be set to half duplex by clearing control bit MR0.8
REPEATER	123		I	REPEATER MODE: - REPEATER is a global pin that, when set, places the chip into repeater mode. In this mode, full duplex is prohibited, CRS responds to receive activity only and, in 10BASE-T mode, the SQE test function is disabled. This mode can also be entered by setting the per port register bit, MR16.15. This pin is not used in RMII mode.

CONTROL AND STATUS (continued)

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
MII/RMII	122		I	INTERFACE SELECT: - The 78Q2124 is capable of interfacing to both RMI and MI Interfaces. The MII/RMII pin on the 78Q2124 controls the interface that is selected. When this pin is set, the MII interface is selected. RMII is selected when this pin is pulled low. This pin is not used in RMII mode.
CMLSEL	1	4	I	COMMON MODE PECL OUTPUT SELECT: - CMLSEL enables a low power PECL mode when set. In this mode the TX/FOP and TX/FON pins sink a current through external load resistors. When CMLSEL is low, conventional PECL drivers are used with 50 ohm equivalent termination.
ISO0 ISO1 ISO2 ISO3	2 3 4 5	5 6 7 8	I/O	ISOLATE: - ISOn, when set, will cause the 78Q2124/R to present a high impedance on its RMII and MII output pins. This allows for multiple PHY to be attached to the same MII interface. The isolate function is intended for MII bussed applications. The bussed application in RMII is not supported. When the 78Q2124/R is isolated, it stills responds to management transactions. The default value of this bit depends on the state of the ISODEF pin.
ISODEF	160		I	ISOLATE POLARITY DEFINITION: - ISODEF when set causes the ISO bit in MR0 to default to high. When ISODEF pin is tied low, the ISO bit defaults to low. This pin is not used in RMII mode.

MDI (MEDIA DEPENDENT INTERFACE)

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
TX/FOP0	155	127	A	TRANSMIT OUTPUT: - In 100BASE-TX and 10BASE-T modes, TXOPn is the positive transmit output and TXONn is the negative output. - In 100BASE-FX mode, FOPn is the positive fiber-optic transmit output and FONn is the negative output.
TX/FON0	156	128		
TX/FOP1	147	119		
TX/FON1	148	120		
TX/FOP2	137	109		
TX/FON2	138	110		
TX/FOP3	129	101		
TX/FON3	130	102		
RX/FIP0	151	123	A	RECEIVE INPUT: - In 100BASE-TX and 10BASE-T modes, RXIPn is the positive receive input and RXINn is the negative input. - In 100BASE-FX mode, FIPn is the positive fiber-optic receive input and FINn is the negative input.
RX/FIN0	152	124		
RX/FIP1	143	115		
RX/FIN1	144	116		
RX/FIP2	133	105		
RX/FIN2	134	106		
RX/FIP3	125	97		
RX/FIN3	126	98		
SD/TXB0	154	126	A	100BASE-FX SIGNAL DETECT ENABLE: - 100BASE-TX is selected for a given port when SD/TXBn is pulled low or left unconnected. - 100BASE-FX is enabled when a valid PECL signal is applied to this pin. The PECL logic levels are referenced with respect to the potential on the VPE supply pin.
SD/TXB1	146	118		
SD/TXB2	136	108		
SD/TXB3	128	100		

LED INDICATORS

The LED pins use standard 3-state logic drivers. They output a logic low when the LED is meant to be on and a logic high when it is meant to be off. The typical configuration for the LEDs is shown in Figure 3.

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
LEDDPLX_01 LEDDPLX _23	15 103	19 75	O	DUPLEX LED: - The LEDDPLX_n pins convey DUPLEX information.
LED100/10_01 LED100/10_23	16 104	20 76	O	100Mbit/s AND 10Mbit/s RATE LEDs: - LED100/10_n pins display 100Mbit/s and 10Mbit/s operational status. When the port is in autonegotiation mode, this pin will be placed in a high Z state.
LEDL/COL_01 LEDL/COL_23	17 105	21 77	O	LINK AND COL LEDs: - LEDL/COL_n pins convey the LINK and COLLISION status of the 78Q2124/R's ports.
LEDTX/RX_01 LEDTX/RX_23	18 106	22 78	O	TRANSMIT AND RECEIVE LEDs: - LEDTX/RX_n pins convey the TRANSMIT and RECEIVE status of the 78Q2124/R's ports.
LEDPORT0	20	24	O	LED PORT 0 SELECT: - LEDPORT0 addresses the operation data for port 0 displaying it on the two sets of seven LED_01 data LEDs.
LEDPORT1	19	23	O	LED PORT 1 SELECT: - LEDPORT1 addresses the operation data for port 1 displaying it on the two sets of seven LED_01 data LEDs.
LEDPORT2	102	74	O	LED PORT 2 SELECT: - LEDPORT2 addresses the operation data for port 2 displaying it on the two sets of seven LED_23 data LEDs.
LEDPORT3	101	73	O	LED PORT 3 SELECT: - LEDPORT3 addresses the operation data for port 3 displaying it on the two sets of seven LED_23 data LEDs.

CLOCK

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
CKIN	6		I	CLOCK INPUT: - In MII mode the 78Q2124 requires a 100ppm 25 MHz clock source. This pin is not used in RMII mode.

MISCELLANEOUS PINS

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
GPIO0	58	46	I/O	GENERAL PURPOSE I/O PIN: - **GPIO0** is configurable as an input or an output via management interface. Setting port 0's bit MR16.6 configures GPIO0 as an input, and clearing the bit configures it as an output. The logic level of the GPIO0 pin is reflected in port 0's MR16.7. This pin has a weak internal pull-down to prevent it from floating when configured as an input (it is configured as an input by default).
GPIO1	59	47	I/O	GENERAL PURPOSE I/O PIN: - **GPIO1** is configurable as an input or an output via management interface. Setting port 1's bit MR16.6 configures GPIO1 as an input, and clearing the bit configures it as an output. The logic level of the GPIO1 pin is reflected in port 1's MR16.7. This pin has a weak internal pull-down to prevent it from floating when configured as an input (it is configured as an input by default).
GPIO2	60	48	I/O	GENERAL PURPOSE I/O PIN: - **GPIO2** is configurable as an input or an output via management interface. Setting port 2's bit MR16.6 configures GPIO2 as an input, and clearing the bit configures it as an output. The logic level of the GPIO2 pin is reflected in port 2's MR16.7. This pin has a weak internal pull-down to prevent it from floating when configured as an input (it is configured as an input by default).
GPIO3	61	49	I/O	GENERAL PURPOSE I/O PIN: **GPIO3** is configurable as an input or an output via management interface. Setting port 3's bit MR16.6 configures GPIO3 as an input, and clearing the bit configures it as an output. The logic level of the GPIO3 pin is reflected in port 3's MR16.7. This pin has a weak internal pull-down to prevent it from floating when configured as an input (it is configured as an input by default).
INTR	111	85	OZ	INTERRUPT PIN: - **INTR** is a global pin that signals an interrupt to the media access controller. The pin is held in the high impedance state when an interrupt is not indicated. The state this pin will be driven to is determined by the OR'ed value of the INTR_LEVEL bits (MR16.14). The trigger events can be programmed via the per port Interrupt Control Registers located at address MR17.

REFERENCE PIN

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
RIBB	141	113	A	BIAS CURRENT SETTING RESISTOR: - **RIBB** is to be tied to an external 9.76 kΩ (1%) resistor which is connected to RIBB_RET. This resistor should be placed as close as possible to the package pin.
RIBB_RET	142	114	A	BIAS RESISTOR GROUND RETURN: - To be tied to an external 9.76 kΩ (1%) resistor which is connected to RIBB. This resistor should be placed as close as possible to the package pin.

POWER SUPPLY

PIN NAME	PIN NUMBER		TYPE	DESCRIPTION
	160	128		
Vcc	10,14,37, 40,57,81,84,107, 110, 124, 158	3,12,15,18,33, 36,45, 61,64, 79, 82,84, 95	S	- SUPPLY VOLTAGE: Two supply ranges are supported for the 78Q2124: 5V ± 0.5V, or 3.3V ± 0.3V. One supply voltage is supported for 78Q2124R: 3.3V ± 0.3V.
VPE	132,150	104,122	S	PECL SUPPLY VOLTAGE: Two supply ranges are supported for the 78Q2124/R: 5V ± 0.5V, or 3.3V ± 0.3V. Must be set at supply to which external PECL is referenced. VPE potential must be greater than or equal to Vcc.
GND	9,11,12, 13,38, 39,64,82,83, 108,109, 121,127,131, 135, 139,140,145, 149,153, 157	1,2,11,13, 14, 16, 17, 34, 35, 52,62, 63,81,80, 83,96, 99, 103, 107, 111, 112, 117,121, 125	S	GROUND

REGISTER DESCRIPTION

The 78Q2124/R implements four sets of ten 16-bit registers which are accessible via the MDIO and MDC pins. The supported registers are shown below. Unsupported registers will be read as all zeros.

The MII management 16-bit register set implemented in the 78Q2124/R is as follows:

ADDRESS	SYMBOL	NAME	RESET VALUE (HEX)
0	MR0	Control	(3100)
1	MR1	Status	(7809)
2	MR2	PHY Identifier 1	000E
3	MR3	PHY Identifier 2	7041 (note 1)
4	MR4	Auto-Negotiation Advertisement	(01E1)
5	MR5	Auto-Negotiation Link Partner Ability	0000
6	MR6	Auto-Negotiation Expansion	0000
7	MR7	(Not implemented, read as zero)	0000
8-15	MR8-15	(Reserved, read as zero)	0000
16	MR16	Vendor Specific	0540
17	MR17	Interrupt Control/Status Register	0000
18	MR18	Diagnostic Register	(0000)

Note 1: MR3[3:0] contains revision specific data.

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
R	Readable by management	W	Write-able by management
RC	Cleared on a read operation	SC	Self clearing, write-able
0/1	Default value upon power-up or reset	(0/1)	Default value dependent on pin setting. The value in brackets indicates typical case.

REGISTER DESCRIPTION (continued)

MR0 - CONTROL REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
0.15	RESET	R, W, 0, SC	RESET: Setting this bit to logic one resets the entire 78Q2124/R. This bit is self clearing.
0.14	LOOPBK	R, W, 0	LOOPBACK: When this bit is set, no transmission of data on the network medium occurs and any receive data on the network medium is ignored. By default, the loopback signal path will encompass as much of the 78Q2124/R circuitry as possible.
0.13	SPEEDSL	R, W, (1)	SPEED SELECTION: This bit determines the speed of operation of the 78Q2124/R. A logic one indicates 100BASE-TX operation and a logic zero indicates 10BASE-T. When auto-negotiation is enabled, this bit will have no effect on the 78Q2124/R. At reset, this bit reflects the highest operating speed allowed by the TECH [2:0] pins. The MII can write to this bit, but the bit will change value only if the new value is allowed by the TECH [2:0] pins.
0.12	ANEGEN	R, W, (1)	AUTO-NEGOTIATION ENABLE: The auto-negotiation process is enabled by setting this bit to a logic one. This bit can only be set to logic one if the ANEGA pin is a logic one and will default to a logic one upon reset in this case. If this bit is cleared to logic zero, manual speed and duplex mode selection is accomplished through bits 0.8 (DUPLEX) and 0.13 (SPEEDSL) of the configuration register or the TECH[2:0] pins according to the table shown in the section describing the TECH[2:0] pins. If the ANEGA pin is brought from zero to one and reset is not asserted, this bit will remain at zero until a one is written.
0.11	PWRDN	R, W, 0	POWER-DOWN: The 78Q2124/R ports may be placed in a low power consumption state by setting this bit to logic one. While in power-down state, the 78Q2124/R still responds to management transactions. The global power-down state can also be achieved by setting PWRDN pin high.
0.10	ISO	R, W, (0)	ISOLATE: When set, the 78Q2124 will present a high impedance on its MII output pins. This allows for multiple PHY to be attached to the same MII interface. When the 78Q2124 is isolated, it stills responds to management transactions. The default value of this bit depends on the ISODEF pin. When ISODEF pin is tied high the ISO bit defaults to high. When ISODEF pin is tied low, the ISO bit defaults to low.
0.9	RANEG	R, W, 0, SC	RESTART AUTO-NEGOTIATION: Normally, the auto-negotiation process is started at power-up. The process can be restarted by setting this bit to logic one. This bit is self clearing.

MR0 - CONTROL REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
0.8	DUPLEX	R, W, (0)	DUPLEX MODE: This bit determines whether the 78Q2124/R supports full duplex or half duplex. A logic one indicates full duplex operation and a logic zero indicates half duplex. When auto-negotiation is enabled, this bit will have no effect on the 78Q2124/R. At reset, this bit reflects the highest operating mode allowed by the TECH [2:0] pins. The MII can write to this bit, but the bit will change value only if the new value is allowed by the TECH pins.
0.7	COLT	R, W, 0	COLLISION TEST: When this bit is set to one, the 78Q2124 will assert the COL signal in response to the assertion of TXEN signal. Collision test is disabled in PCS bypass and RMII modes. Collision test is enabled regardless of the duplex mode of operation.
0.6:0	RSVD	R, 0	RESERVED

MR1 - STATUS REGISTER

Bits 1.15 through 1.11 reflect the ability of the 78Q2124 as configured by the TECH[2:0] pins They do not reflect any ability changes made via the MII management interface to bits 0.13 (SPEEDSL), 0.12 (ANEGEN) and 0.8 (DUPLEX).

BIT	SYMBOL	TYPE	DESCRIPTION
1.15	100T4	R, 0	100BASE-T4 ABILITY: This bit is permanently held at logic zero.
1.14	100X_F	R, (1)	100BASE-TX FULL DUPLEX ABILITY: (0 = not able, 1 = able)
1.13	100X_H	R, (1)	100BASE-TX HALF DUPLEX ABILITY: (0 = not able, 1 = able)
1.12	10T_F	R, (1)	10BASE-T FULL DUPLEX ABILITY: (0 = not able, 1 = able)
1.11	10T_H	R, (1)	10BASE-T HALF DUPLEX ABILITY: (0 = not able, 1 = able)
1.10:6	RSVD	R, 0	RESERVED
1.5	ANEGC	R, 0	AUTO-NEGOTIATION COMPLETE: A logic one indicates a) that the auto-negotiation process has completed, b) that the contents of registers MR4, 5, and 6 are valid, and c) that a highest common denominator rate and mode have been found.
1.4	RFAULT	R, 0, RC	REMOTE FAULT: A logic one indicates that a remote fault condition has been detected. It remains set until it is cleared. This bit can only be cleared by reading this register (MR1) via the management interface.
1.3	ANEGA	R, (1)	AUTO-NEGOTIATION ABILITY: This bit, when set, indicates the ability to perform auto-negotiation. The value of this bit is determined by the ANEGA pin.
1.2	LINK	R, 0	LINK STATUS: A logic one indicates that a valid link has been established. If the link status should transition from an OK status to a NOT-OK status, this bit will become cleared and remain cleared until it is read.

MR1 - STATUS REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
1.1	JAB	R, 0, RC	JABBER DETECT: In 10Base-T mode, this bit is set during a jabber event. After a jabber event it remains set until cleared by a read operation.
1.0	EXTD	R, 1	EXTENDED CAPABILITY: This bit is permanently set to logic one to indicate that the 78Q2124/R provides an extended register set (MR2 and beyond).

MR2, 3 - PHY IDENTIFIER REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
2.15:0	OUI	R, 000Eh	ORGANIZATIONALLY UNIQUE IDENTIFIER: This value is 00-C0-39 for TDK Semiconductor Corporation. This translates to a value of 000Eh for this register.
3.15:10	OUI	R, 011100	ORGANIZATIONALLY UNIQUE IDENTIFIER: Remaining 6 bits of the OUI.
3.9:4	MN	R, 000100	MODEL NUMBER: Six bits containing manufacturer's part number. 78Q2124/R is encoded into the 6 bits. (000100)
3.3:0	RN	R,0001	REVISION NUMBER: For example, a value of 0001 corresponds to the first version of the silicon.

MR4 - AUTO-NEGOTIATION ADVERTISEMENT REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
4.15	NP	R,0	NEXT PAGE: Not supported; permanently tied to logic zero.
4.14	RSVD	R,0	RESERVED: This bit is permanently set to logic 0.
4.13	RF	R, W, 0	REMOTE FAULT: When internally set to logic one, the MII management interface indicates to the link partner a remote fault condition.
4.12:5	TAF	R, W, (0Fh)	TECHNOLOGY ABILITY FIELD: The default value of this field is dependent upon MR1.15:11 bits. This field can be overwritten by management to auto-negotiate to an alternate common technology. Writing to this register has no effect until auto-negotiation is enabled.
4.12:10	A7:5	R, 0	Reserved for future technology.
4.9	A4	R, 0	100BASE-T4: The 78Q2124/R does support 100BASE-T4.
4.8	A3	R, W, (1)	100BASE-TX FULL DUPLEX: The default value of this bit follows MR1.14 bit. When the default is zero, this bit set by the management.
4.7	A2	R, W, (1)	100BASE-TX:The default value of this bit follows MR 1.13 bit. When the default is zero, this bit cannot be set by the management.
4.6	A1	R, W, (1)	10BASE-T FULL DUPLEX: The default value of this bit follows MR1.12 bit. When the default is zero, this bit cannot be set by the management.

MR4 - AUTO-NEGOTIATION ADVERTISEMENT REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
4.5	A0	R, W, (1)	10BASE-T: The default value of this bit follows MR1.11 bit. When the default is zero, this bit cannot be set by the management.
4.4:0	S4:0	R, 00001	SELECTOR FIELD: Hard coded with the value of 00001 for IEEE-802.3.

MR5 - AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
5.15	NP	R, 0	NEXT PAGE: When set, it indicates that the link partner wishes to engage in next page exchange.
5.14	ACK	R, 0	ACKNOWLEDGE: When set, it indicates that the link partner has successfully received at least 3 consecutive and consistent FLP bursts.
5.13	RF	R, 0	REMOTE FAULT: When set, it indicates that the link partner has a fault.
5.12:5	A7:0	R, 0	TECHNOLOGY ABILITY FIELD: This field contains the technology ability of the link partner. The bit definition is the same as MR4.12:5.
5.4:0	S4:0	R, 00000	SELECTOR FIELD: This field contains the type of message sent by the link partner. For IEEE-802.3 compliant link partner transceiver, this field should be 00001.

MR6 - AUTO-NEGOTIATION EXPANSION REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
6.15:5	RSVD	R, 0	RESERVED
6.4	PDF	R, 0, RC	PARALLEL DETECTION FAULT: When set, it indicates that more than one technology was detected during link up. This bit is cleared when read.
6.3	LPNPA	R, 0	LINK PARTNER NEXT PAGE ABLE: When set, it indicates that the link partner supports the next page function.
6.2	NPA	R, 0	NEXT PAGE ABLE: Permanently tied to logic zero since the 78Q2124/R does not support next page function.
6.1	PRX	R, 0, RC	PAGE RECEIVED: Set when a properly matched link code word has been received into the Auto-negotiation Link Partner. This bit is cleared when read.
6.0	LPANEGA	R, 0	LINK PARTNER AUTO-NEGOTIATION ABLE: When set it indicates that the link partner is able to participate in the auto-negotiation function.

MR16 - VENDOR SPECIFIC REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
16.15	REPEATER	R, W, (0)	REPEATER MODE: When set, this bit puts the port into repeater mode. In this mode, full duplex is prohibited, CRS responds to receive activity only and, in 10BASE-T mode, the SQE test function is disabled. The 78Q2124 can be placed in a global REPEATER mode via the REPEATER pin.
16.14	INT LEVEL	R, W, 0	When this bit is a zero, the INTR pin is forced low to signal an interrupt. Setting this bit for any of the four ports causes the INTR pin to be forced high to signal an interrupt.
16.13	RSVD	R, 0	RESERVED
16.12	TXHIM	R, W, 0	TRANSMIT HIGH IMPEDANCE: When this per port bit is set, the transmitter UTP driver is in a high impedance state and TXCLKn is tri-stated. The receive circuitry remains fully functional. Only a reset condition will automatically clear this bit.
16.11	SQE TEST INHIBIT	R, W, 0	Setting this per port bit disables 10BASE-T SQE testing. By default, when this bit is a zero, the SQE test is performed by generating a COL pulse following the completion of a packet transmission.
16.10	10BT NATURAL LOOPBACK	R, W, 0	Setting this per port bit causes transmitted data on TXD to be automatically looped back to the RXD receive signals when 10BASE-T mode is enabled.
16.9	PHYMIR	R, (0)	PHY MIRROR: PHYMIR controls the internal mapping of the 2 LSB PHYAD bits as described by Table 2. This bit reflects the setting of the external PHYMIR pin upon power up.
16.8	PHYGLB	R, W, (0)	PHY GLOBAL: Setting this bit in any of the four ports will cause the 78Q2124/R to enter the global address mode. To disable global addressing, this bit was set needs to be cleared. Following reset this bit will reflect the setting of the PHYGLB pin.
16.7	GPIO_DAT	R, W, 0	GENERAL PURPOSE I/O 1 DATA BIT: When the GPIO_DIR is set, this bit reflects the value of the GPIO1 pin. When the GPIO1_DIR is reset, the value of this bit is driven onto the GPIO1 pin.
16.6	GPIO_DIR	R, W, 1	GENERAL PURPOSE I/O 1 DIRECTION BIT: Setting this bit configures the GPIO1 pin as an input. Clearing this bit configures GPIO as an output.
16.5	$\overline{\text{APOL}}$	R, W, 0	AUTO POLARITY: During auto-negotiation and 10BASE-T mode, the 78Q2124 is able to automatically invert the received signal - both the Manchester data and link pulses - if necessary. Setting this per port bit disables this feature.
16.4	RVSPOL	R, (W), 0	REVERSE POLARITY: The reverse polarity is detected either through 8 inverted 10BASE-T link pulses (NLP) or through one burst of inverted fast link pulses (FLP). When the reverse polarity is detected, the 78Q2124 will invert the receive data path and set this bit to logic one if the feature is not disabled. If $\overline{\text{APOL}}$ is a logic 1, then this bit is write-able. Setting this per port bit forces the polarity to be reversed.

MR16 - VENDOR SPECIFIC REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
16.3:2	RSVD	R,W,0	RESERVED. Must be zero.
16.1	PCSBP	R,W,0	PCS BYPASS: When this per port bit is set, the 100BASE-TX PCS is bypassed, as are the scrambler and descrambler functions. Scrambled 5-bit code groups for transmission are applied to the TXER, TXD[3:0] pins and received on the RXER, RXD[3:0] pins. The RXDV and TXEN signals are not valid in this mode. PCSBP mode is only valid when 100BASE-TX is enabled. This mode can also be entered with the use of the global PCSBP pin.
16.0	RXCC	R,W,0	RECEIVE CLOCK CONTROL: When this per port bit is set, the RXCLK signal will be held in logic low (only in 100BASE-TX mode) when there is no data being received (to save power). The RXCLK signal will restart 1 clock cycle before the assertion of RXDV and be shut off 64 clock cycles after RXDV goes low. RXCC is disabled when loopback mode is enabled (MR0.14 is high). This bit should be kept at logic zero when the chip is in PCS Bypass mode.

MR17 - INTERRUPT CONTROL/STATUS REGISTER

The Interrupt Control/Status Register provides the means for controlling and observing the events which trigger an interrupt on the INTR pin. This register can also be used in a polling mode via the MII serial interface as a means to observe key events within the PHY via one register address. These bits are cleared after the register is read. Bits 8-15 of this register, when set to logic one, enable their corresponding bit in the lower byte to signal an interrupt on the INTR pin. The level of this interrupt can be set via MR16.14. The Interrupts enabled in each of the four Interrupt Control/Status Registers are ORed to the Global INTR pin.

BIT	SYMBOL	TYPE	DESCRIPTION
17.15	JABBER IE	R, W, 0	JABBER INTERRUPT ENABLE BIT
17.14	RXER IE	R, W, 0	RECEIVE ERROR INTERRUPT ENABLE BIT
17.13	PRX IE	R, W, 0	PAGE RECEIVED INTERRUPT ENABLE BIT
17.12	PFD IE	R, W, 0	PARALLEL DETECT FAULT INTERRUPT ENABLE BIT
17.11	LP-AC K IE	R, W, 0	LINK PARTNER ACKNOWLEDGE INTERRUPT ENABLE BIT
17.10	LS-CHG IE	R, W, 0	LINK STATUS CHANGE INTERRUPT ENABLE BIT
17.9	RFAULT IE	R, W, 0	REMOTE FAULT INTERRUPT ENABLE BIT
17.8	ANEG-COMP IE	R, W, 0	AUTO-NEGOTIATION COMPLETE INTERRUPT ENABLE BIT
17.7	JABBER INT	RC, 0	JABBER INTERRUPT: This bit is set when a jabber event is indicated by the 10BASE-T circuitry.
17.6	RXER INT	RC, 0	RECEIVE ERROR INTERRUPT: This bit is set when the RXER signal transitions high.
17.5	PRX INT	RC, 0	PAGE RECEIVE INTERRUPT: This bit is set when a new page has been received from the link partner during auto-negotiation.
17.4	PDF INT	RC, 0	PARALLEL DETECT FAULT INTERRUPT: This bit is set by the auto-negotiation logic when a parallel detect fault condition is indicated.

MR17 - INTERRUPT CONTROL/STATUS REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
17.3	LP-ACK INT	RC, 0	LINK PARTNER ACKNOWLEDGE INTERRUPT: This bit is set by the auto-negotiation logic when FLP bursts are received with the acknowledge bit set.
17.2	LS-CHG INT	RC, 0	LINK STATUS CHANGE INTERRUPT: This bit is set when the link transitions from an OK status to a fail status or vice versa.
17.1	RFAULT INT	RC, 0	REMOTE FAULT INTERRUPT: This bit is set when a remote fault condition has been indicated by the link partner.
17.0	ANEG-COMP INT	RC, 0	AUTO-NEGOTIATION COMPLETE INTERRUPT: This bit is set by the auto-negotiation logic upon successful completion of auto-negotiation.

MR18 - DIAGNOSTIC REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
18.15:14	RSVD	R, 0	RESERVED
18.13	FIBER	R,0	FIBER MODE: This bit indicates that 100BASE-FX mode has been selected for this port.
18.12	ANEGF	R,0,RC	AUTO-NEGOTIATION FAIL: This bit is set when auto-negotiation completes and no common technology was found. It remains set until read.
18.11	DPLX	R, 0	DUPLEX: This bit indicates the result of the auto-negotiation for duplex arbitration. If set it indicates that full-duplex was the highest common denominator. If clear it indicates that half-duplex was the highest common denominator.
18.10	RATE	R, 0	RATE: This bit indicates the result of the auto-negotiation for data rate arbitration. If set it indicates that 100BASE-TX was the highest common denominator. If clear it indicates that 10BASE-T was the highest common denominator.
18.9	RX-PASS	R, 0	RECEIVE PASS: In 10BASE-T mode, this bit indicates that Manchester data has been detected. In 100BASE-TX mode, it indicates that a valid received signal has been detected (but not necessarily locked on to).
18.8	RX-LOCK	R, 0	RECEIVE LOCK: Indicates that the receive PLL has locked onto the received signal for the selected speed of operation (10BASE-T or 100BASE-TX). This bit is cleared whenever a cycle-slip occurs, and will remain cleared until it is read.
18.7:0	RSVD	R, W, 0	RESERVED. Must be zero.
18.4:0	RSVD	R, W,0	RESERVED. Must be zero.

PULL-UP/PULL-DOWN RESISTORS:
The following pins require a weak resistive pull-up or pull-down. Recommended resistor values are shown:

Pin Name	Resistor	PU/PD
MDIO	1.5 kΩ	PU

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum rating may permanently damage the device.

PARAMETER	RATING
DC Supply Voltage	7 VDC
Storage Temperature	-65 to 150°C
Pin Voltage	-0.3 to (Vcc+0.3) VDC
Pin Current	± 100 mA

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges:

DC Voltage Supply, Vcc	3.3 V ± 0.3V, 5 V ± 0.5V VDC
Ambient Operating Temperature, Ta	0 - 70°C

DC CHARATERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	I_{CC}	V_{CC} = 3.3V; Auto-Negotiation (All Ports Autonegotiating) 10BT (Idle, All Ports) 10BT (Normal Activity) 100BTX (All Ports) Transmit High Impedance		 100 340 380 120	 120 400 520 460 140	mA
Supply Current	I_{CC}	V_{CC} = 5.0V; Auto-Negotiation (All Ports Autonegotiating) 10BT (Idle, All Ports) 10BT (Normal Activity) 100BTX Transmit High Impedance		 120 360 420 140	 140 460 560 540 160	mA
Supply Current	I_{CC}	Powerdown mode		2	2.5	mA

ELECTRICAL SPECIFICATIONS (continued)

DIGITAL INPUT CHARACTERISTICS

Pins of type I, I/O

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
TTL Input Voltage Low	V_{IL}				0.8	V
TTL Input Voltage High	V_{IH}		2.0			V
TTL Input Current	I_{IL}, I_{IH}	V_{CC} = 5.5V	-10		+10	µA
Input Capacitance	C_{IN}			10		pF

DIGITAL INPUT CHARACTERISTICS

Pins of type A

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
PECL Input Voltage Low	V_{IL}		V_{CC} -1.8		V_{CC} -1.6	V
PECL Input Voltage High	V_{IH}		V_{CC} -1.0		V_{CC} -0.8	V
SD/TXB Input Current	I_{in}	Fiber Mode Selected		$\frac{V_{SD}}{3k}$		µA
RX/FIB, RX/FIN Input Current	I_{in}	Fiber Mode Selected		$\frac{Vcc - 7.5}{4.4k}$		µA

DIGITAL OUTPUT CHARACTERISTICS

Pins of type O, OZ

Output Voltage High	V_{OH}	$4.5V \le V_{CC} \le 5.5V$ I_{OH} = 4.0mA	V_{CC}-0.6			V
Output Voltage Low	V_{OL}	$4.5V \le V_{CC} \le 5.5V$ I_{OL} = 4.0mA			0.4	V
Output Transition Time Between V_{OL} and V_{OH}	T_t	$4.5V \le V_{CC} \le 5.5V$ I_{OH}, I_{OL} = 4.0mA		5		ns
Output Voltage High	V_{OH}	$3.0V \le V_{CC} \le 3.6V$ I_{OH} = 2.0mA	V_{CC}-0.4			V
Output Voltage Low	V_{OL}	$3.0V \le V_{CC} \le 3.6V$ I_{OL} = 2.0mA			0.4	V
Output Transition Time Between V_{OL} and V_{OH}	T_t	$3.0V \le V_{CC} \le 3.6V$ I_{OH}, I_{OL} = 2.0mA		5		ns

DIGITAL OUTPUT CHARACTERISTICS

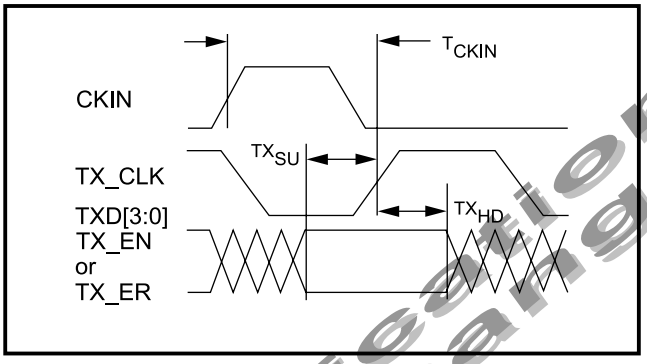
Pins of type A

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Logic Voltage Swing		CMLSEL=0	0.6		0.9	V
PECL Threshold Voltage	*V_{mid}	CMLSEL=0		V_{CC} – 1.3		V
PECL Output Current High	Ioh	CMLSEL=1		8		mA
PECL Output Current Low	Iol	CMLSEL=1		0		mA
Output Transition Time Between V_{OL} and V_{OH}	T_t	CMLSEL=0, Cload=5pF		1		ns
Output Transition Time Between V_{OL} and V_{OH}	T_t	CMLSEL=1, Cload=5pF		2		ns

* $V_{OL} = V_{OH}$

ELECTRICAL SPECIFICATIONS (continued)

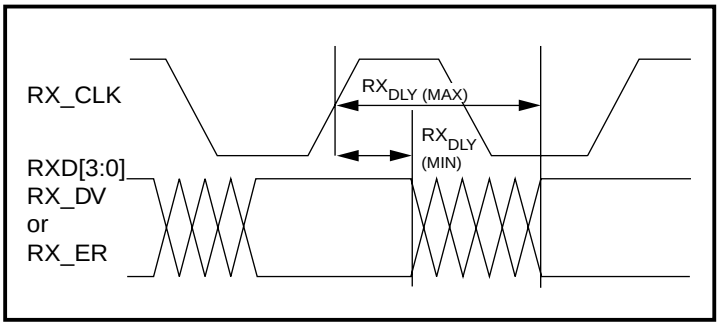
DIGITAL TIMING CHARACTERISTICS



Transmit Inputs to the 78Q2124

MII Transmit Interface

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: TXCLKn to TXDn[3:0], TXENn, TXERn	TX_{SU}		15			ns
Hold Time: TXCLKn to TXDn[3:0], TXENn, TXERn	TX_{HD}		0			ns
CKIN-to-TXCLKn Delay	T_{CKIN}		20		35	ns
TXCLKn Duty-Cycle			40		60	%



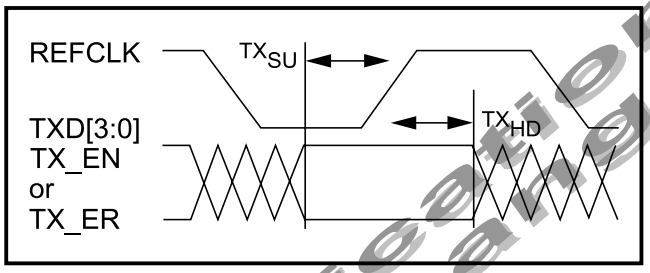
Receive Outputs from the 78Q2124

MII Receive Interface

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Receive Output Delay: RXCLKn to RXDn[3:0], RXDVn, RXERn	RX_{DLY}		10		30	ns
RXCLKn Duty-Cycle			40		60	%

ELECTRICAL SPECIFICATIONS (continued)

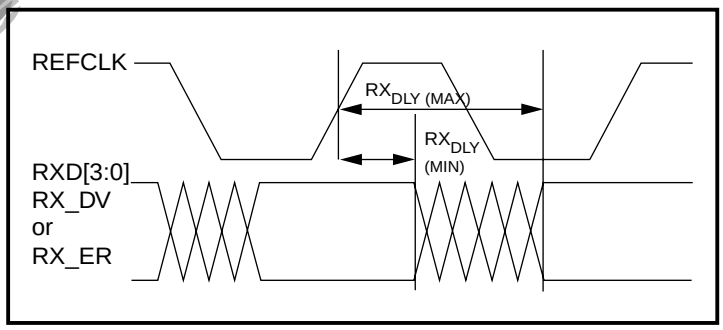
DIGITAL TIMING CHARACTERISTICS



Transmit Inputs to the 78Q2124/R

RMII Transmit Interface

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: REFCLK to TXDn[1:0], TXENn, TXERn	TX_{SU}		4			ns
Hold Time: REFCLK to TXDn[1:0], TXENn	TX_{HD}		2			ns
REFCLK Duty-Cycle			35		65	%

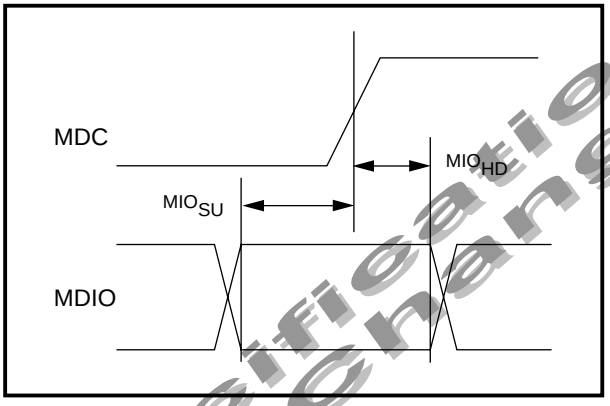


Receive Outputs from the 78Q2124/R

RMII Receive Interface

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Receive Output Delay: REFCLK to RXDn[1:0], CRSDV, RXERn	RX_{DLY}		2		30	ns
REFCLK Duty-Cycle			35		65	%

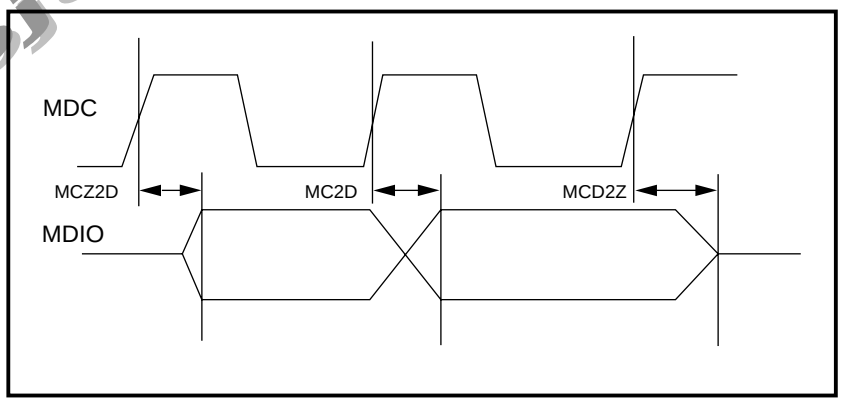
ELECTRICAL SPECIFICATIONS (continued)



MDIO as an Input to the 78Q2124/R

MDIO Interface Input Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: MDC to MDIO	MIO_{SU}		10			ns
Hold Time: MDC to MDIO	MIO_{HD}		0			ns
Max Frequency: MDC	F_{max}				25	MHz



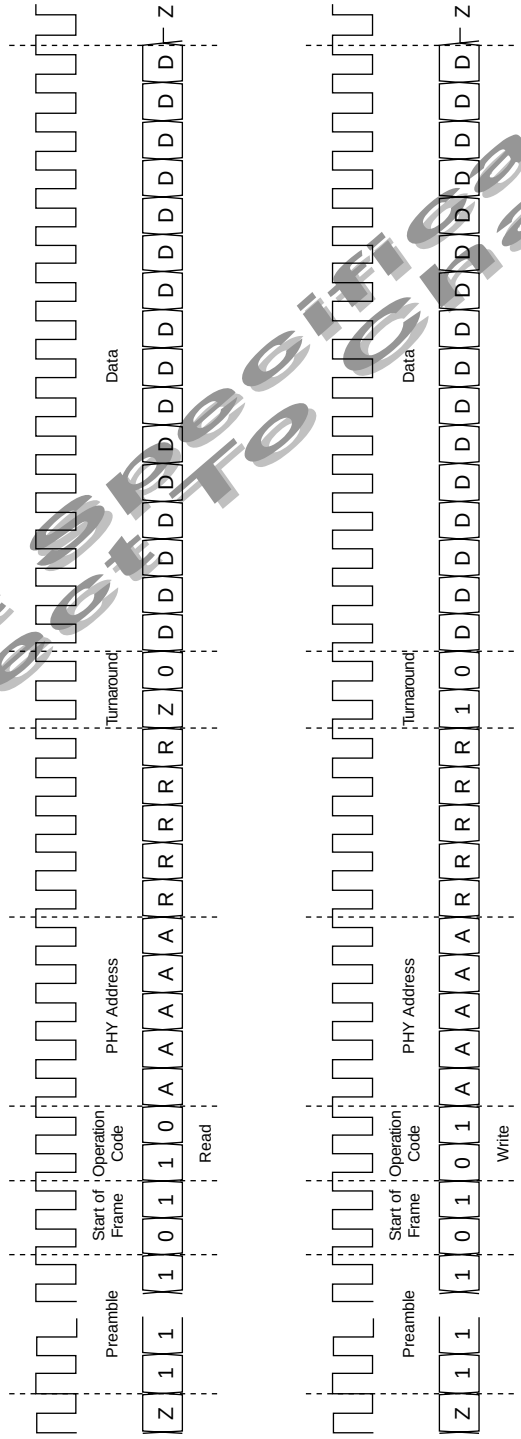
MDIO as an Output from the 78Q2124/R

MDIO Interface Output Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
MDC to MDIO data delay	MC2D				30	ns
MDIO output from high Z to driven after MDC	MCZ2D				30	ns
MDIO output from driven to high Z after MDC	MCD2Z				30	ns

ELECTRICAL SPECIFICATIONS (continued)

MDIO Interface Output Timing



ELECTRICAL SPECIFICATIONS (continued)

100BASE-TX System Timing

System timing requirements for 100BASE-TX operation are listed in table 24-2 of Clause 24 of IEEE 802.3.

PARAMETER	CONDITION	NOM	UNIT
TXENn Sampled to first bit of "J" on MDI output		12	BT
First bit of "J" on MDI input to CRSn assert		15	BT
First bit of "T" on MDI input to CRSn de-assert		23	BT
First bit of "J" on MDI input to COLn assert		16	BT
First bit of "T" on MDI input to COLn de-assert		24	BT
TXENn Sampled to CRS assert	REPEATER = low	4	BT
TXENn sampled to CRS de-assert	REPEATER = low	4	BT

10BASE-T System Timing

TXENn (MII) to TDn Delay				6	BT
RDn to RXDn (MII) Delay				6	BT
Collision delay				9	BT
SQE test wait			1		µs
SQE test duration			1		µs
*Jabber on-time		20		150	ms
*Jabber off-time		250		750	ms

* Guarantee by design. The specifications in the above tables are not tested during production test. They are included for information only.

ELECTRICAL SPECIFICATIONS (continued)

ANALOG ELECTRICAL CHARACTERISTICS

100BASE-TX Transmitter

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
**Peak Output Amplitude, Vp+, Vp-	Best-fit over 14 bit times; 0.5 dB Transformer loss	950		1050	mV
Output Amplitude Symmetry	$\frac{\lvert Vp+\rvert}{\lvert Vp-\rvert}$	0.98		1.02	
Output Overshoot	Percent of Vp+, Vp-			5	%
Rise/Fall time, tr, tf	10 - 90% of Vp+, Vp-	3		5	ns
Rise/Fall time Imbalance	$\lvert tr - tf \rvert$			500	ps
Duty Cycle Distortion	Deviation from best-fit time-grid; 010101... Sequence			±250	ps

** Measured at the line side of the transformer.
Test conditions: Transformer p/n: TLA-6T103
Line Termination: 100Ω ±1%
RIBB: 9.76K ±1% @3.3V

100BASE-TX Transmitter

The specifications in the following table are not tested during production test. They are included for information only.

PARAMETER	CONDITION	MIN	MAX	UNIT
Return Loss	2 < f < 30 MHz 30 < f < 60 MHz 60 < f < 80 MHz	16 $16 - 20\log\left(\frac{f}{30\,MHz}\right)$ 10		dB
Open Circuit Inductance	-8 < Iin < 8 mA	350		µH
Jitter	Scrambled Idle		1.4	ns

The specifications in the following table are not tested during production test. They are included for information only.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Signal Detect Assertion Threshold (pk-pk)		600	900	1000	mV
Signal Detect De-assertion Threshold (pk-pk)		300	350	400	mV
Differential Input Resistance		20			kΩ
PLL Locking Time			5		µs
Jitter Tolerance (pk-pk)			4		ns
Baseline Wander Tracking		-75		+75	%
Signal Detect Assertion Time				200	µs
Signal Detect De-assertion Time				1.4	µs

10BASE-T Transmitter

The Manchester-encoded data pulses, the link pulse and the start-of-idle pulse are tested against the templates and using the procedures found in Clause 14 of IEEE 802.3.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
**Peak Differential Output Signal	All data patterns	2.2		2.8	V
Link Pulse Width			100		ns
Start-of-Idle Pulse Width		300		350	ns

** Measured at the line side of the transformer.
Test conditions: Transformer p/n: TLA-6T103
Line Termination: 100Ω ±1%
RIBB: 9.76K ±1% @3.3V

ELECTRICAL SPECIFICATIONS (continued)

10BASE-T Transmitter

The specifications in the following table are not tested during production test. They are included for information only.

Output return loss		15			dB
Harmonic Content	Any harmonic; dB below fundamental; All ones data	27			dB
Output Impedance Balance	1 MHz < freq < 20 MHz	$29 - 17\log\left(\frac{f}{10}\right)$			dB
Peak Common-mode Output Voltage				50	mV
Common-mode rejection	15 V_{pk}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			100	mV
Common-mode rejection jitter	15 V_{pk}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			1	ns

ELECTRICAL SPECIFICATIONS (continued)

10BASE-T Receiver

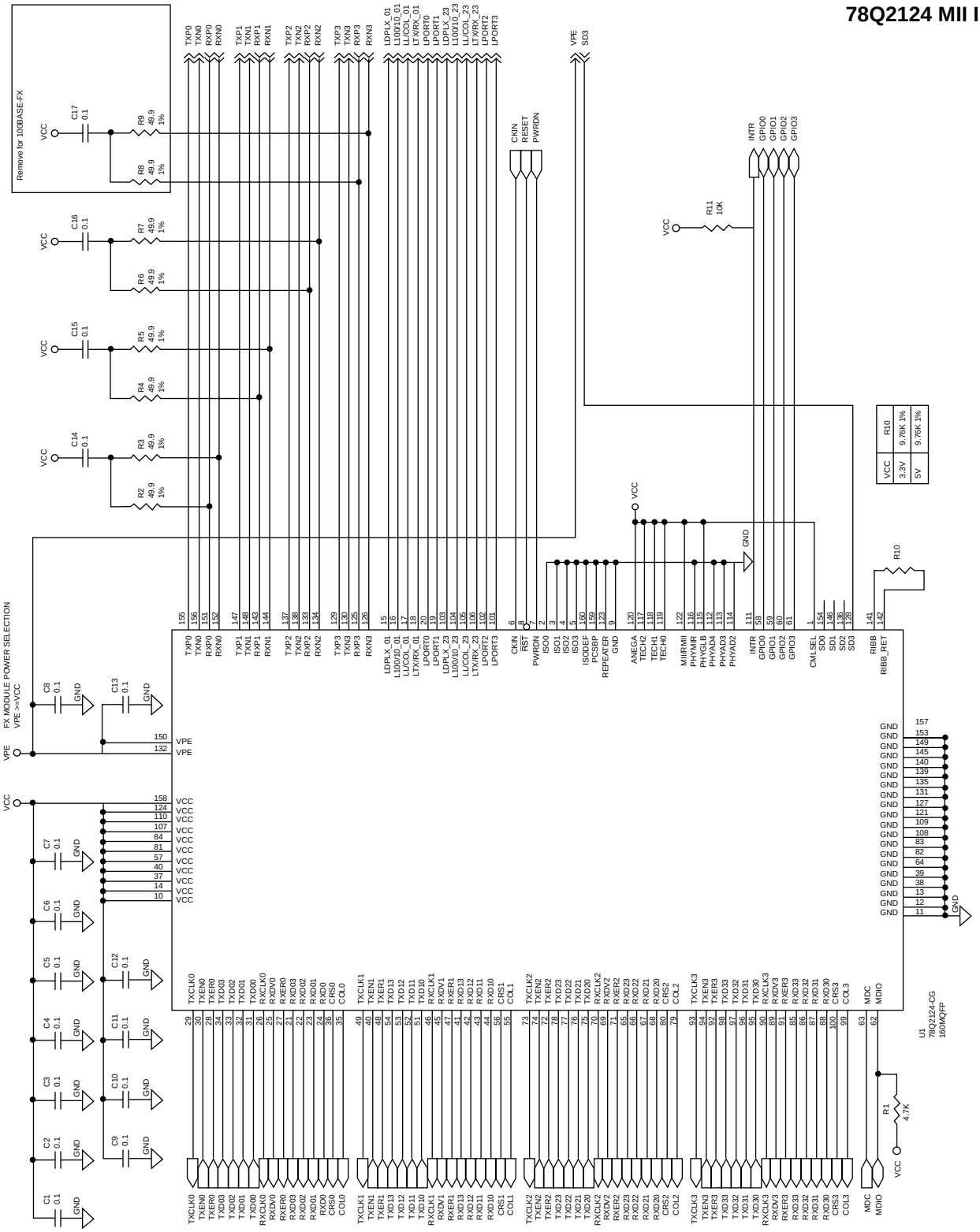
PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PLL Locking Time			1.8		µs
Jitter Tolerance (pk-pk)			32		ns
Input Squelched Threshold		600	900	1000	mV
Input Un-squelch Threshold		300	350	400	mV
Noise immunity	Sine waves: 0 < f < 15MHz 0 < f < 2 MHz Sinusoidal Pulses 2 < f < 15 MHz	 0 0 0		 300 6.2 6.2	 mV V V

10BASE-T Receiver

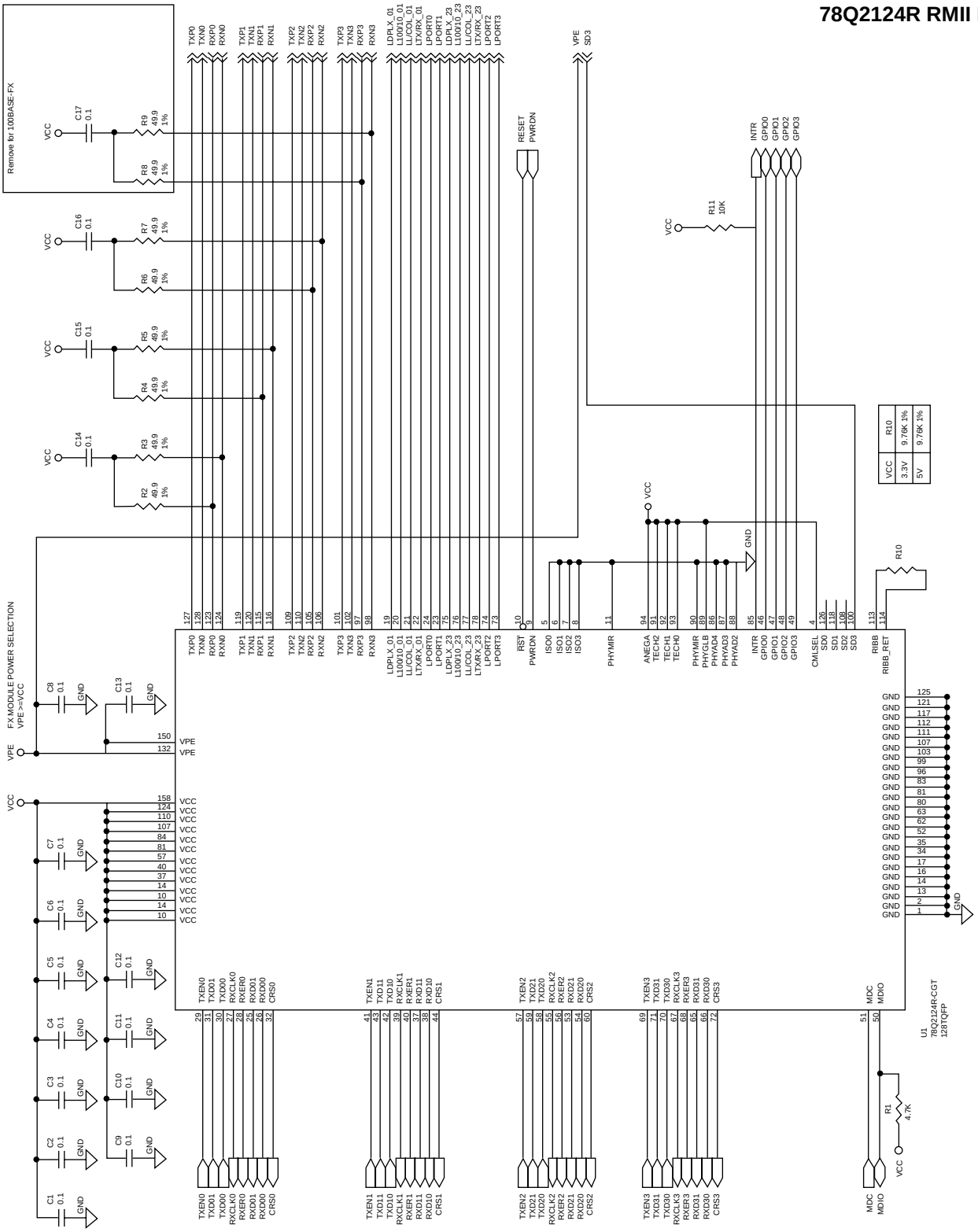
The specifications in the following table are not tested during production test. They are included for information only.

Differential Input Resistance		20			kΩ
Common-mode rejection	Square wave 0 < f < 500 kHz	25			V

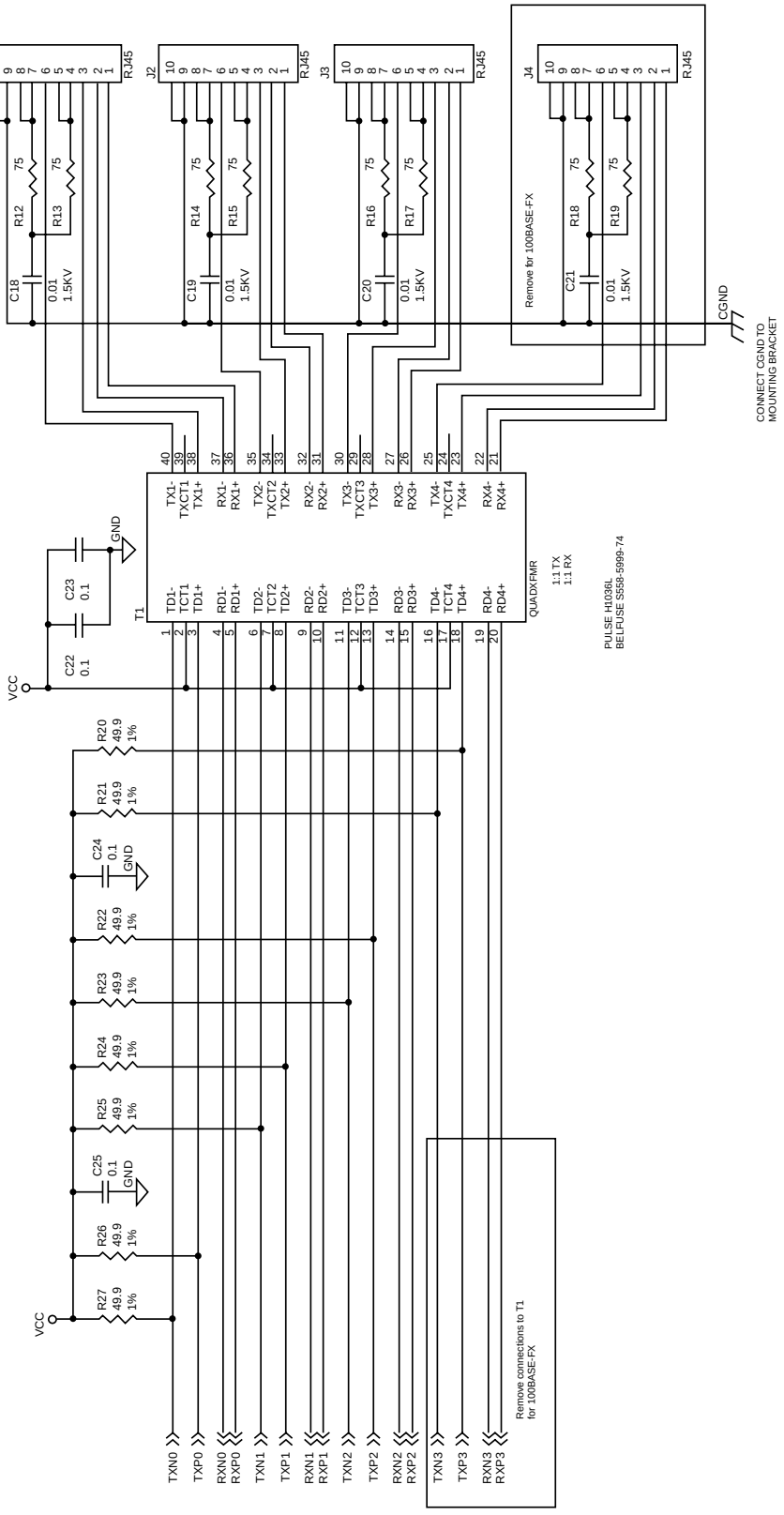
78Q2124 MII Interface



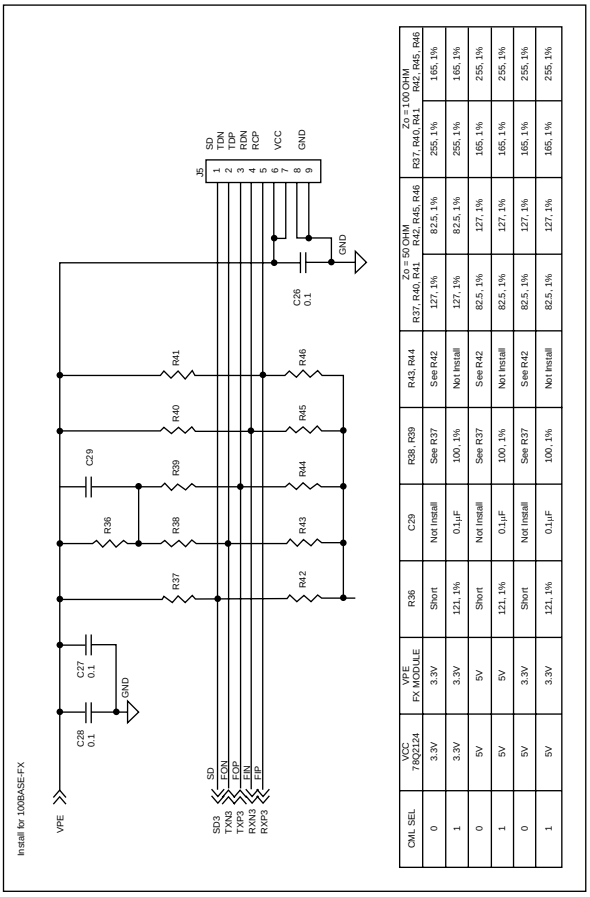
78Q2124R RMII Interface



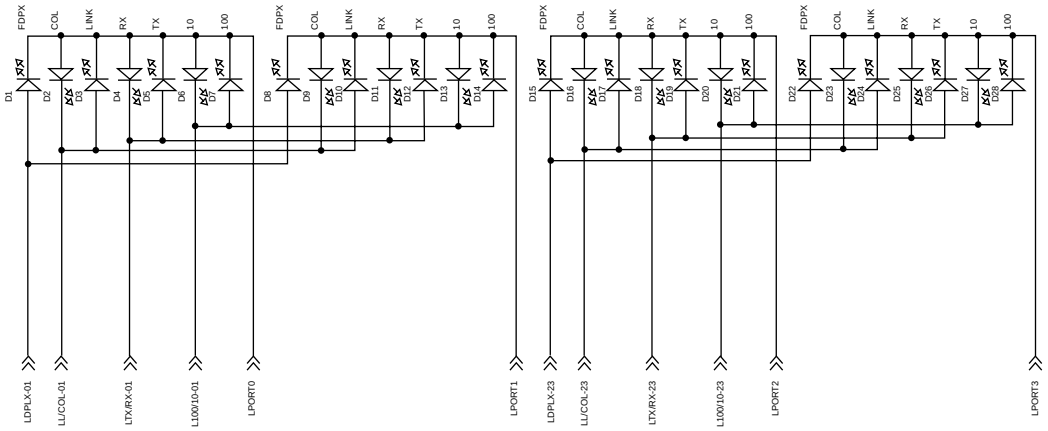
78Q2124/R Transformer Interface



78Q2124/R LED and Fiber Interfaces



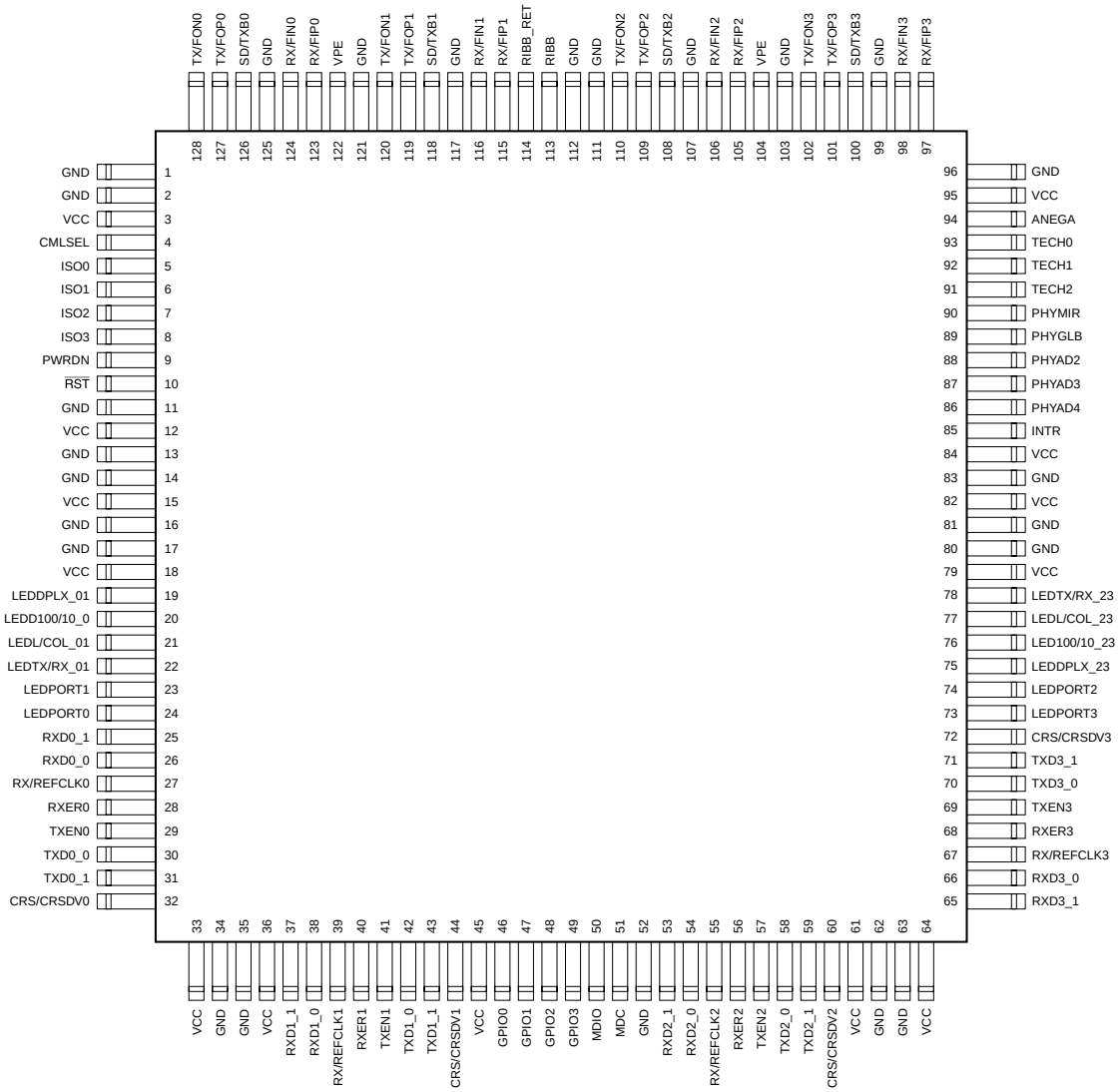
CML SEL	VCC 78Q2124	VPE FX MODULE	R36	C29	R38, R39	R43, R44	Zo = 50 OHM R37, R40, R41	Zo = 50 OHM R42, R45, R46	Zo = 100 OHM R37, R40, R41	Zo = 100 OHM R42, R45, R46
0	3.3V	3.3V	Short	Not Install	See R37	See R42	127, 1%	82.5, 1%	255, 1%	165, 1%
1	3.3V	3.3V	121, 1%	0.1µF	100, 1%	Not Install	127, 1%	82.5, 1%	255, 1%	165, 1%
0	5V	5V	Short	Not Install	See R37	See R42	82.5, 1%	127, 1%	165, 1%	255, 1%
1	5V	5V	121, 1%	0.1µF	100, 1%	Not Install	82.5, 1%	127, 1%	165, 1%	255, 1%
0	5V	3.3V	Short	Not Install	See R37	See R42	82.5, 1%	127, 1%	165, 1%	255, 1%
1	5V	3.3V	121, 1%	0.1µF	100, 1%	Not Install	82.5, 1%	127, 1%	165, 1%	255, 1%



PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

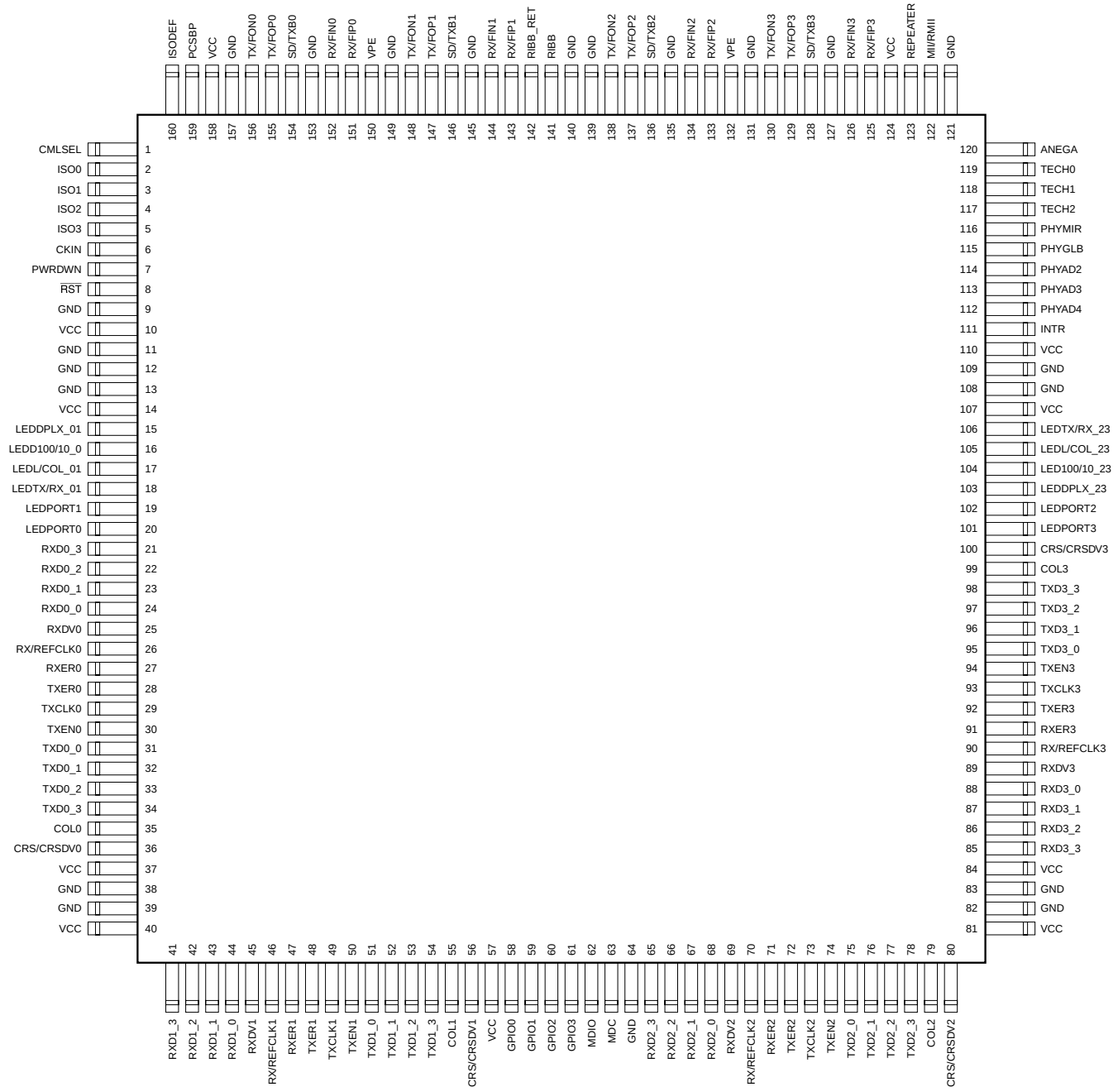


128-Pin TQFP
78Q2124R

PACKAGE PIN DESIGNATIONS (continued)

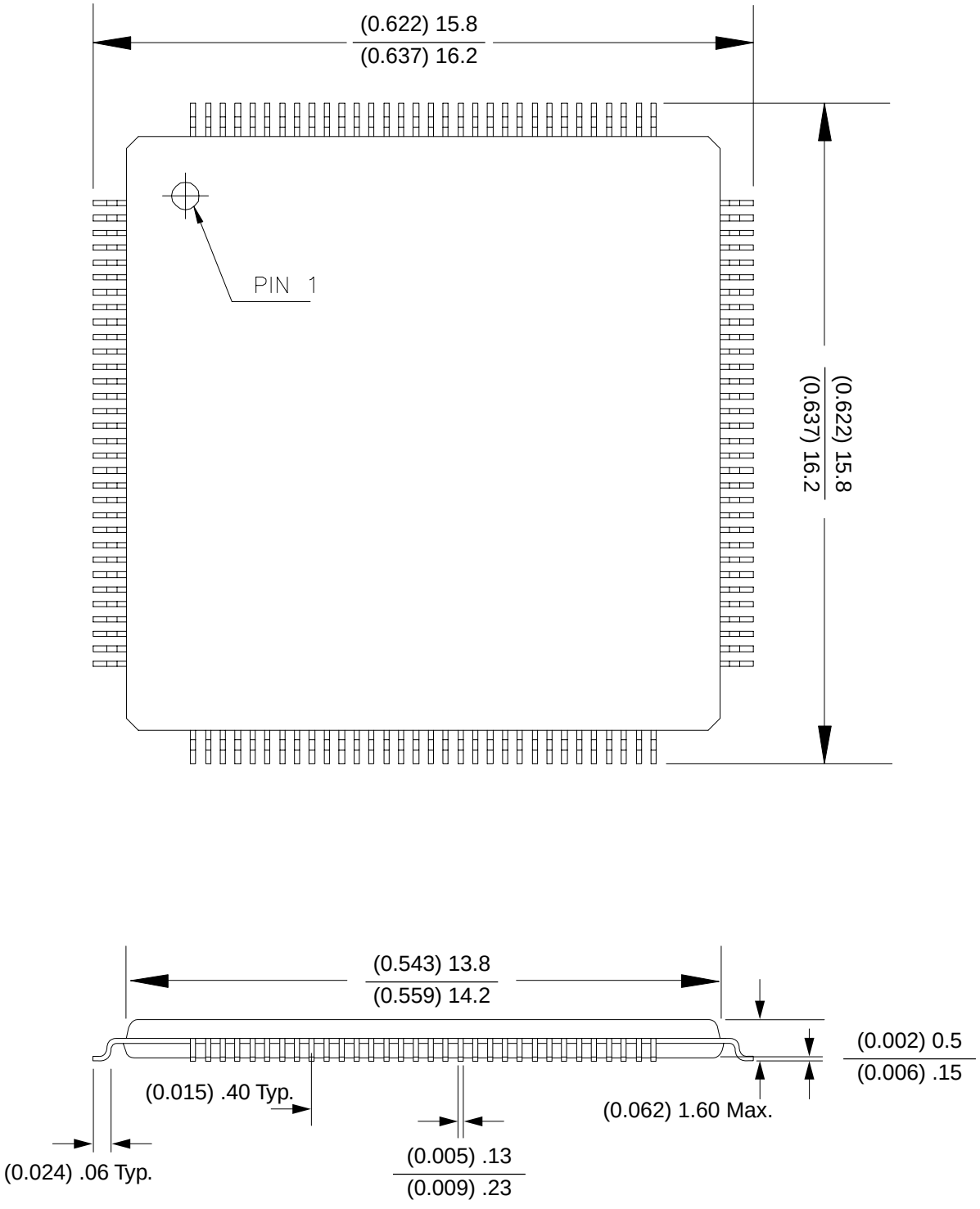
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



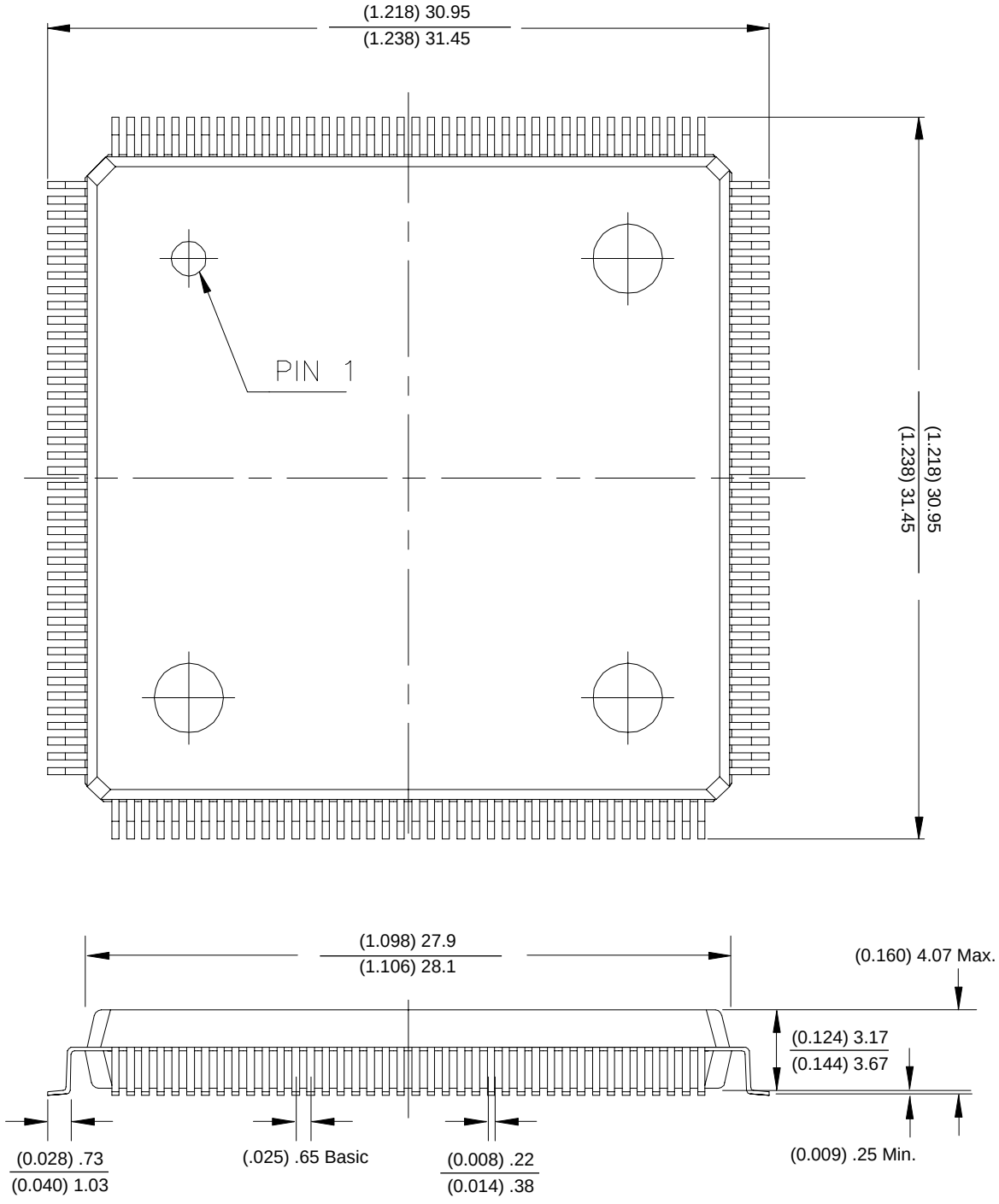
160-Lead MQFP
78Q2124

Mechanical Dimensions



128-TQFP
(14x14x1.4)

Mechanical Dimensions



160-MQFP
(28X28X3.4)

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
78Q2124/R		
128-Pin TQFP	78Q2124R-CGT	78Q2124R-CGT
160-Pin MQFP	78Q2124-CG	78Q2124-CG

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 03/15/99- rev.A