

MITSUBISHI MICROCOMPUTERS 7532 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 7532 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7532 Group has a USB, 8-bit timers, and an A-D converter, and is useful for an input device for personal computer peripherals.

FEATURES

- Basic machine-language instructions 69
- The minimum instruction execution time 0.34 μ s
(at 6 MHz oscillation frequency for the shortest instruction)
- Memory size
 - ROM 8K to 16K bytes
 - RAM 256 to 384 bytes
- Programmable I/O ports 28 (36-pin type)
..... 24 (32-pin type)
- Interrupts 13 sources, 8 vectors
- Timers 8-bit X 3

- Serial I/O1 used only for Low Speed in USB
(USB/UART)
- Serial I/O2 8-bit X 1
(Clock-synchronized)
- A-D converter 10-bit X 8 channels
- Clock generating circuit Built-in type
(connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer 16-bit X 1
- Power source voltage 4.1 to 5.5 V
At 6 MHz XIN oscillation frequency at ceramic resonator
- Power dissipation 30 mW (standard)
- Operating temperature range -20 to 85 °C

APPLICATION

Input device for personal computer peripherals

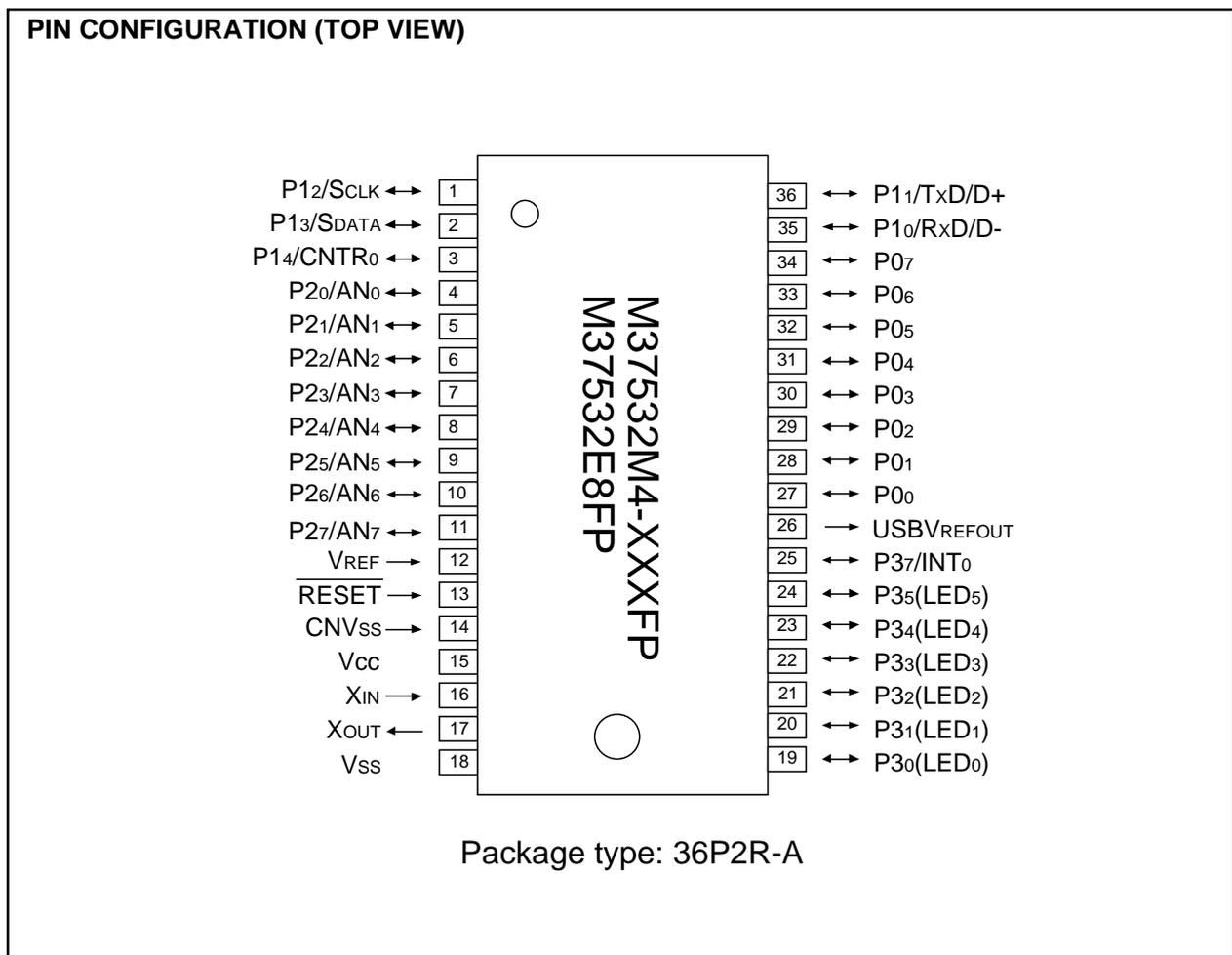


Fig. 1 Pin configuration of M37532M4-XXXXFP, M37532E8FP

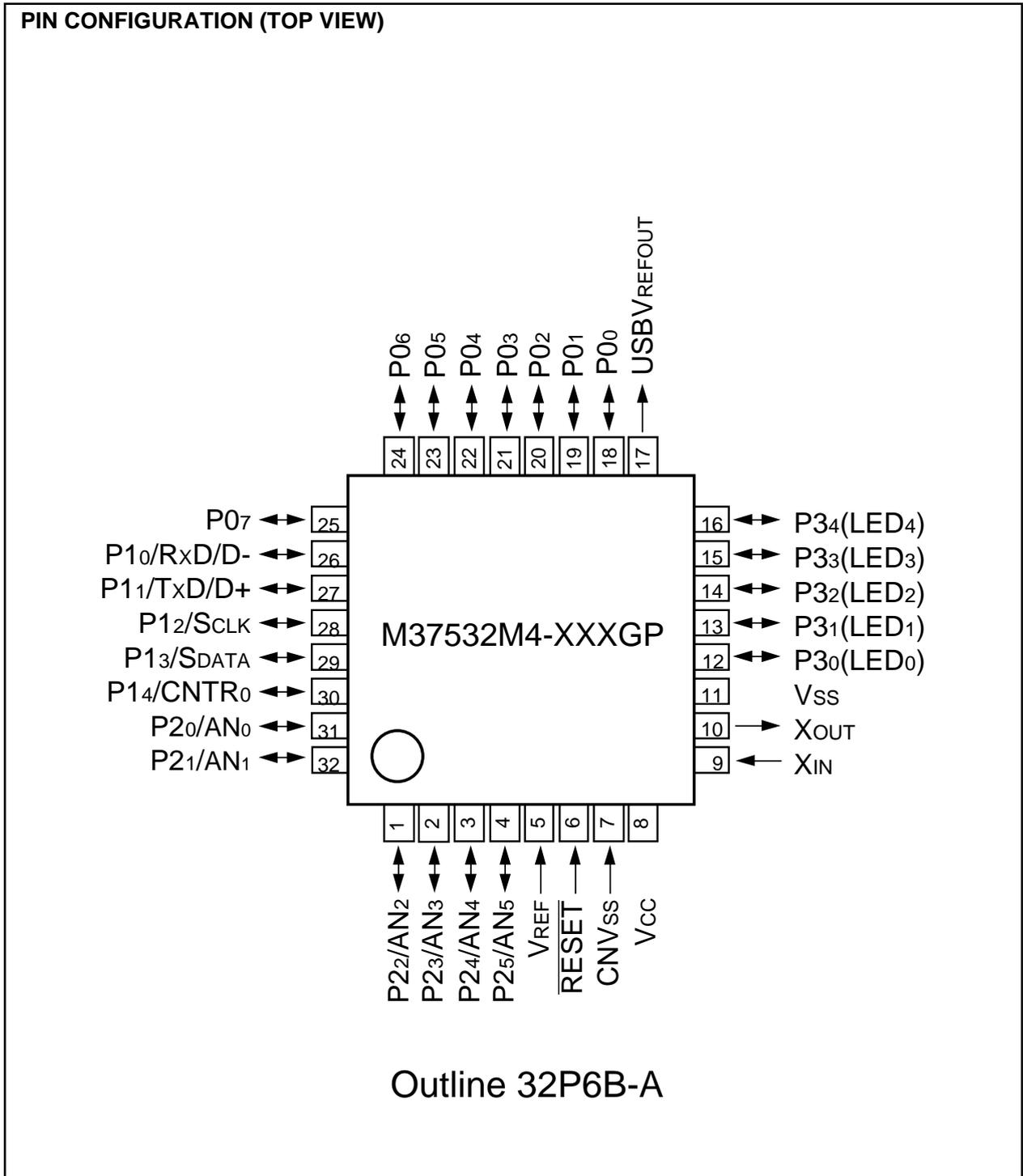


Fig. 2 Pin configuration of M37532M4-XXXGP

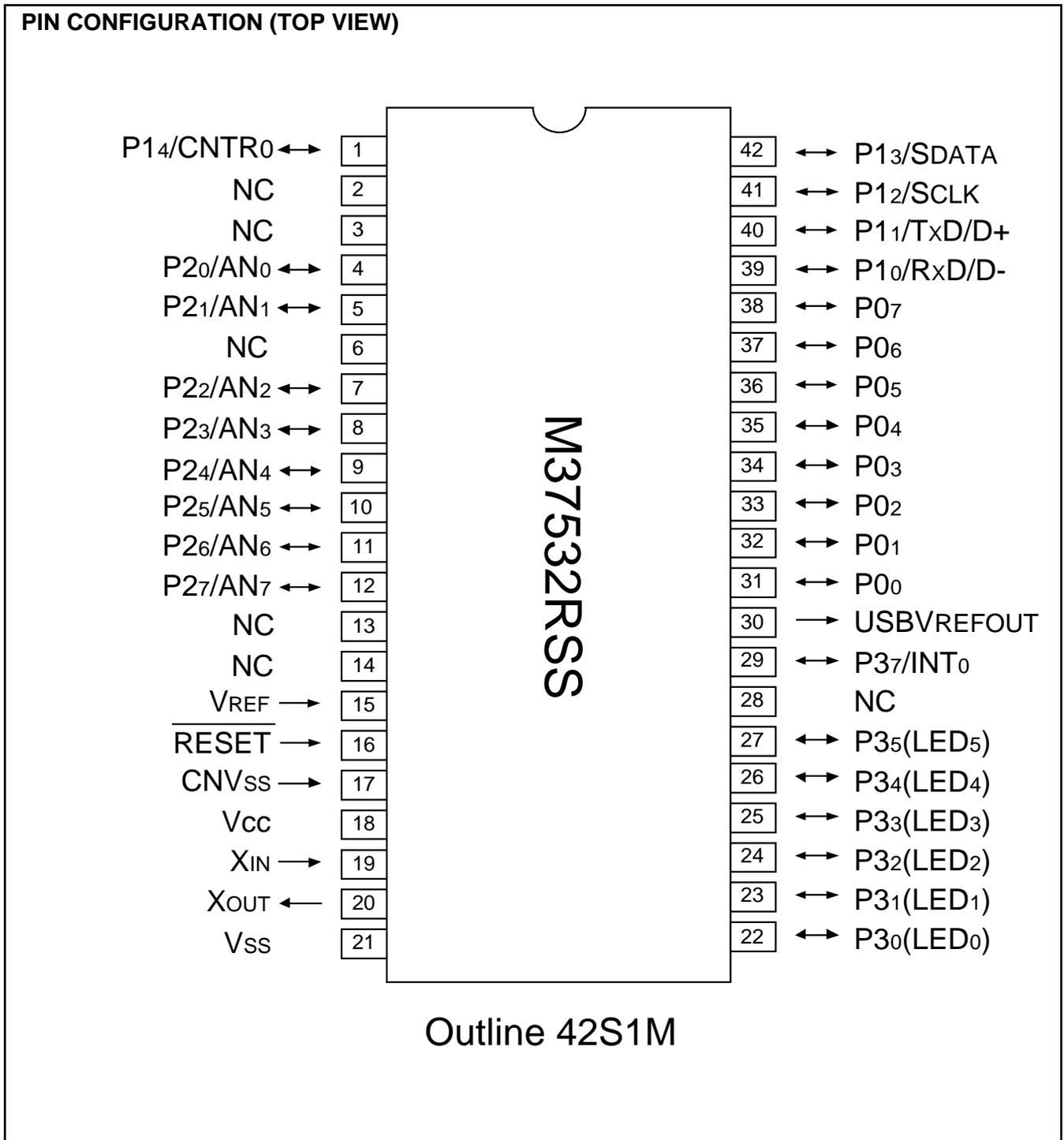


Fig. 3 Pin configuration of M37532RSS

FUNCTIONAL BLOCK

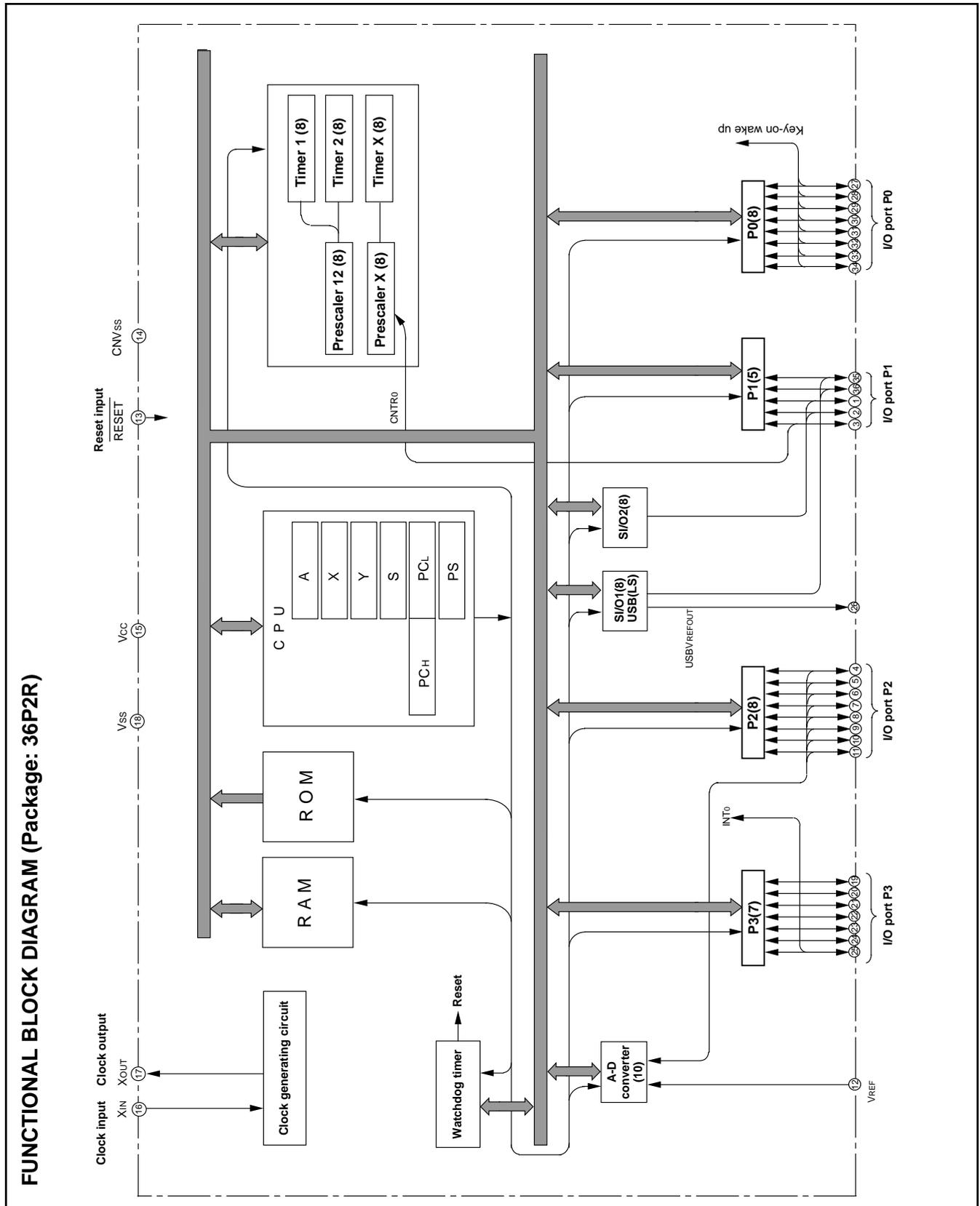


Fig. 4 Functional block diagram

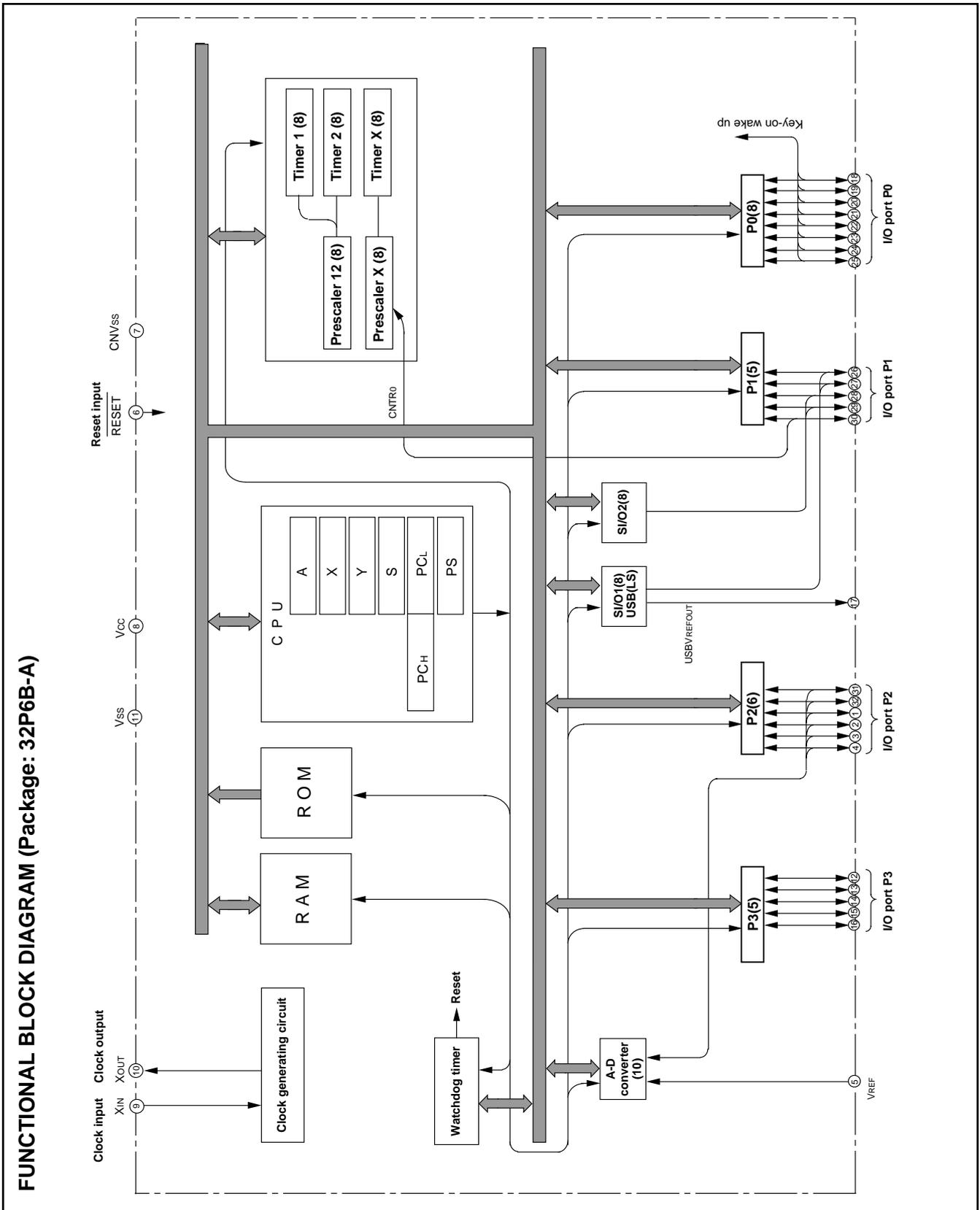


Fig. 5 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source	•Apply voltage of 4.1 to 5.5 V to Vcc, and 0 V to Vss.	
VREF	Analog reference voltage	•Reference voltage input pin for A-D converter	
USBVREFOUT	USB reference voltage output	•Output pin for pulling up a D- line with 1.5 kΩ external resistor	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
RESET	Reset input	•Reset input pin for active “L”	
XIN	Clock input	•Input and output pins for main clock generating circuit	
XOUT	Clock output	•Connect a ceramic resonator or quartz crystal oscillator between the XIN and XOUT pins. •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
P00–P07	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Key-input (key-on wake up interrupt input) pins
P10/RxD/D- P11/TxD/D+ P12/SCLK P13/SDATA P14/CNTR0	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for P10, P12, P13. •When using the USB function, input level of ports P10 and P11 becomes USB input level, and output level of them becomes USB output level.	•Serial I/O1 function pin •Serial I/O2 function pin •Timer X function pin
P20/AN0– P27/AN7	I/O port P2	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	•Input pins for A-D converter
P30–P35 P37/INT0	I/O port P3	•7-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for P37). •CMOS 3-state output structure •P30 to P35 can output a large current for driving LED. •Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Interrupt input pins

GROUP EXPANSION

Mitsubishi plans to expand the 7532 group as follow:

Memory type

Support for Mask ROM version, One Time PROM version, and Emulator MCU .

Memory size

ROM/PROM size 8 K to 16 K bytes
 RAM size 256 to 384 bytes

Package

36P2R-A 0.8 mm-pitch plastic molded SOP
 32P6B-A 0.8 mm-pitch plastic molded LQFP
 42SIM 42 pin shrink ceramic PIGGY BACK

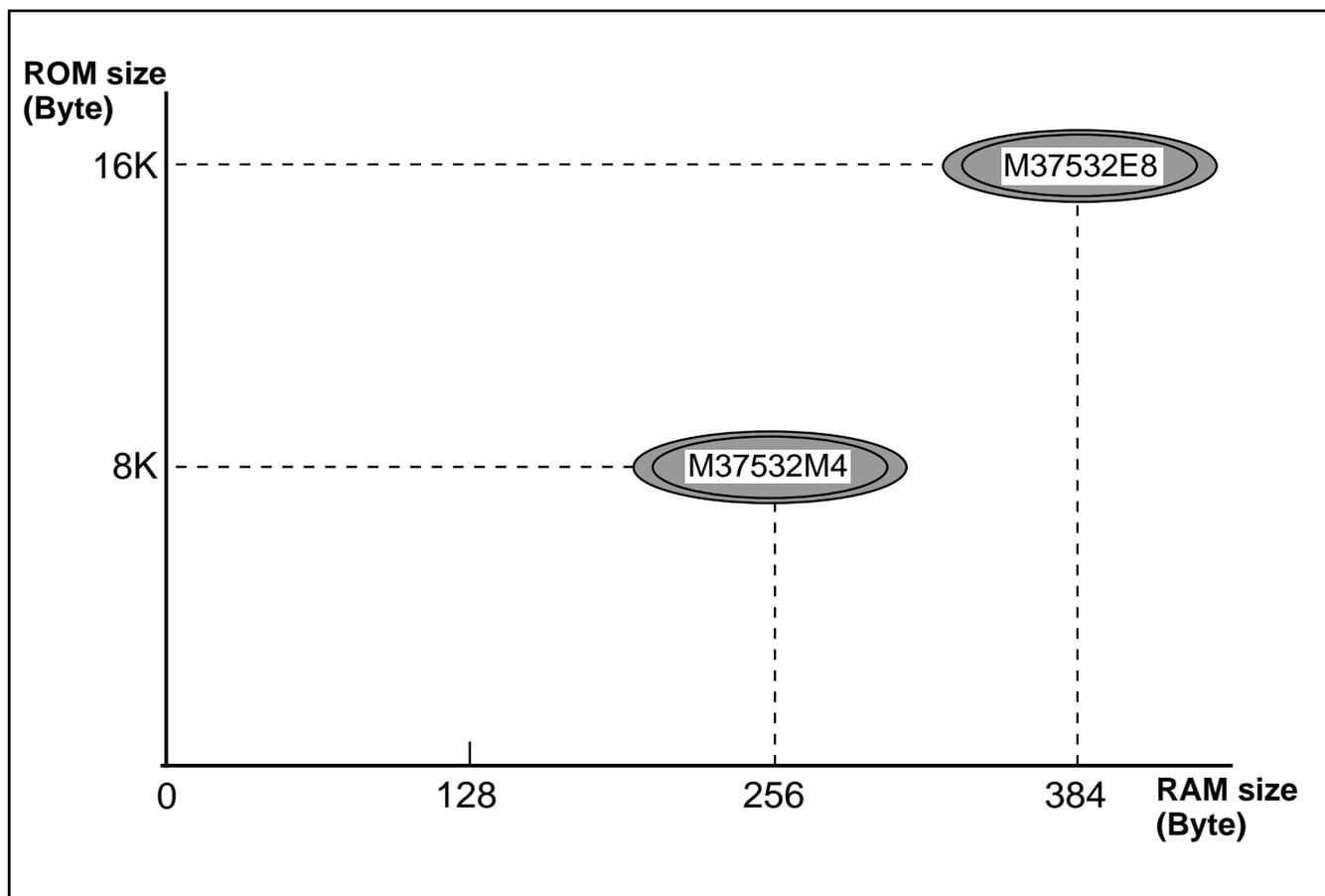


Fig. 6 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37532M4-XXXFP	8192 (8062)	256	36P2R-A	Mask ROM version
M37532M4-XXXGP	8192 (8062)	256	32P6B-A	Mask ROM version
M37532E8FP	16384 (16254)	384	36P2R-A	One Time PROM version (blank)
M37532RSS	—	384	42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 7532 Group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the 740 Family Software Manual for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions cannot be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

[CPU Mode Register] CPUM

The CPU mode register contains the stack page selection bit. This register is allocated at address 003B₁₆.

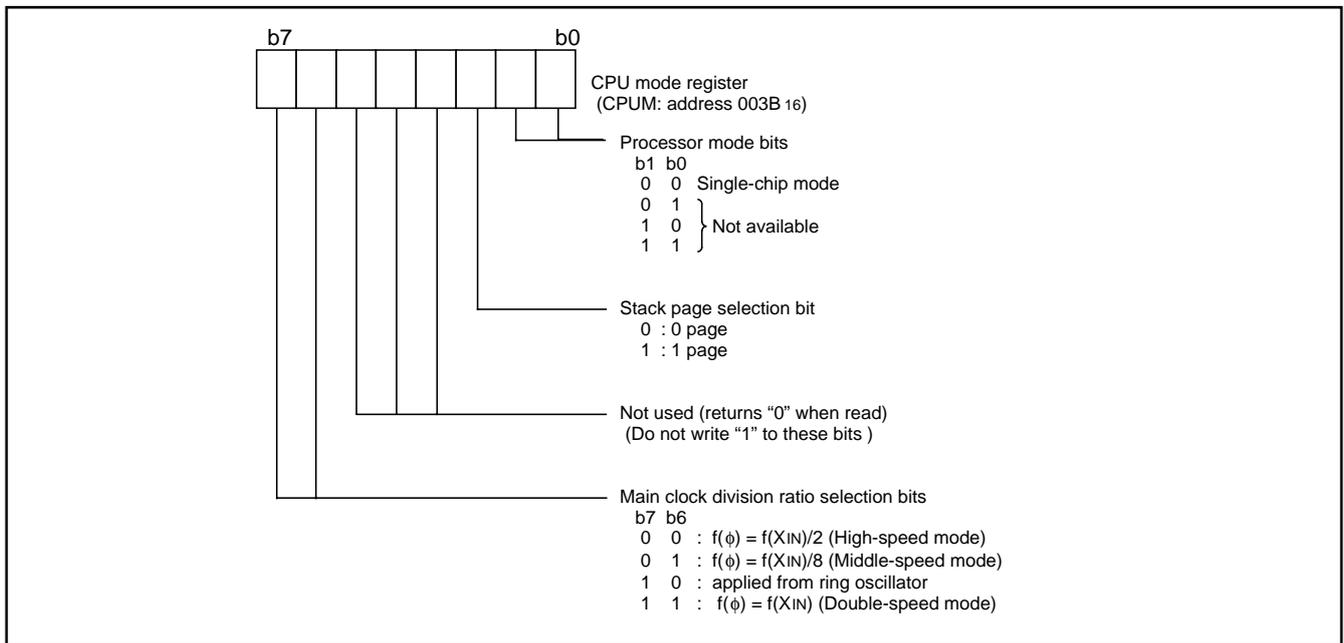
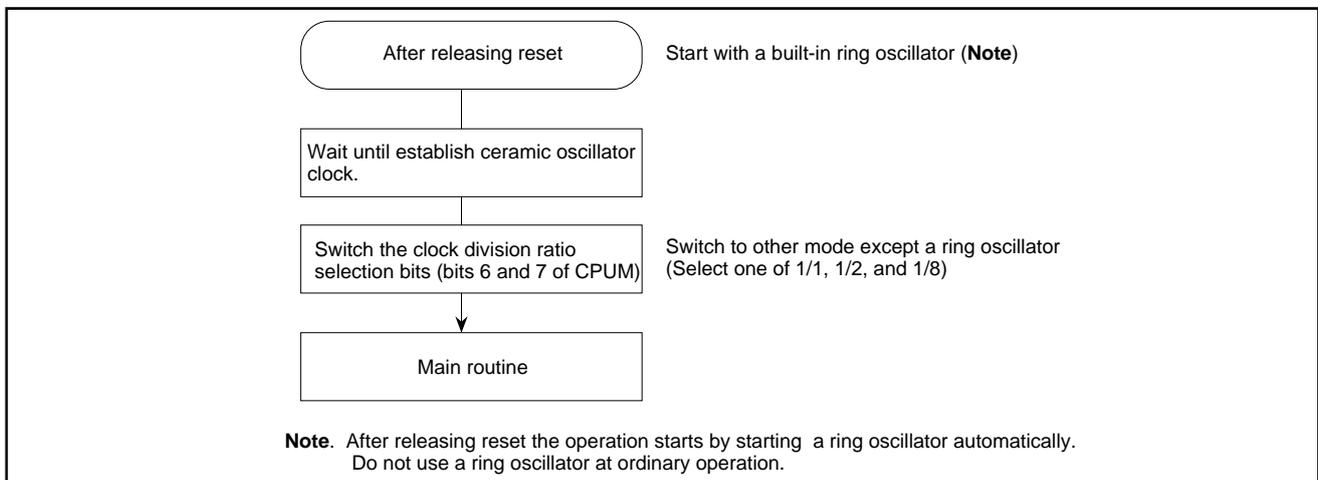


Fig. 7 Structure of CPU mode register

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.



Note. After releasing reset the operation starts by starting a ring oscillator automatically. Do not use a ring oscillator at ordinary operation.

Fig. 8 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

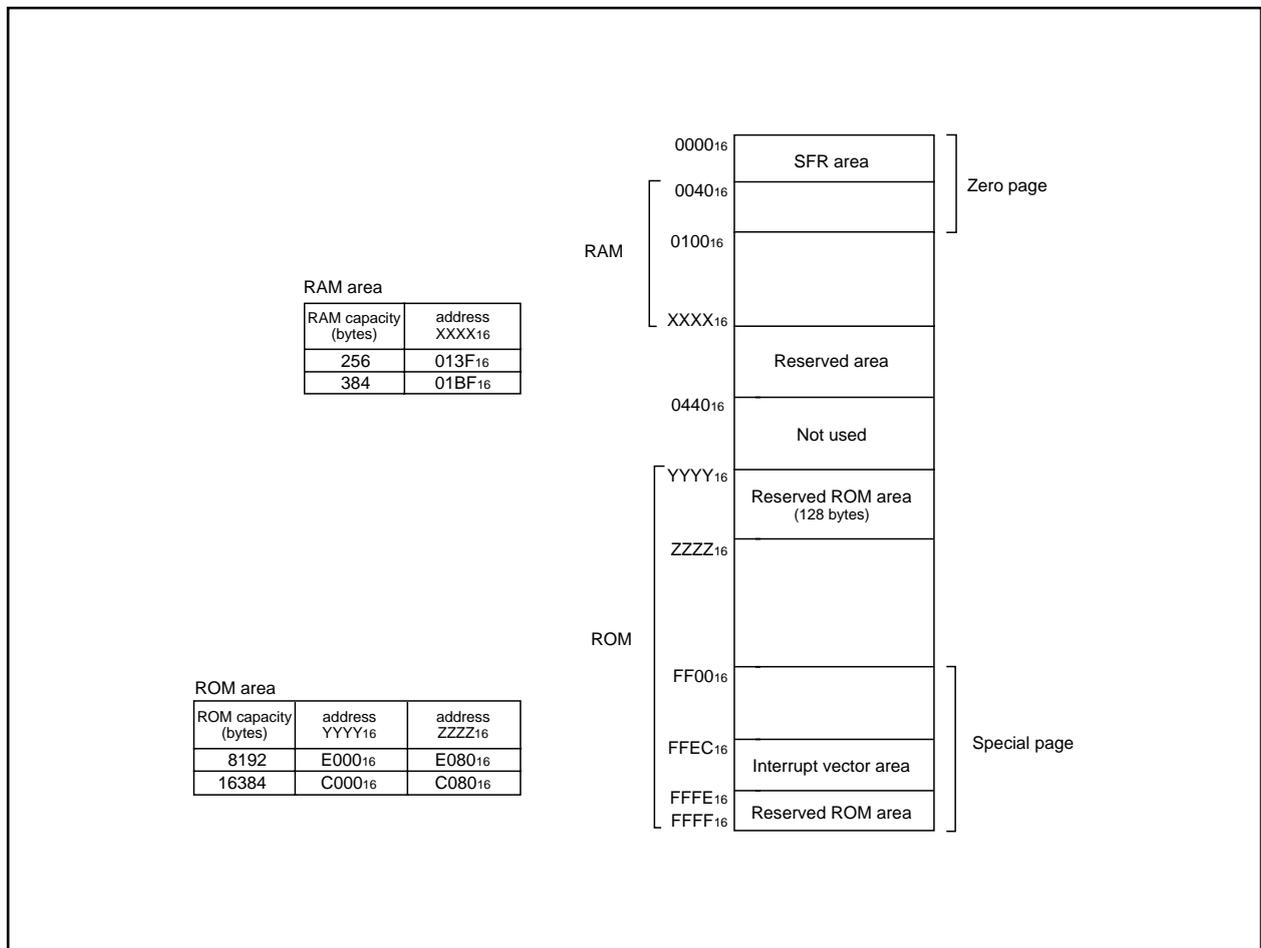


Fig. 9 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	USB interrupt control register (USBICON)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	USB transmit data byte number set register 0 (EP0BYTE)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	USB transmit data byte number set register 1 (EP1BYTE)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	USBPID control register 0 (EP0PID)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	USBPID control register 1 (EP1PID)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	USB address register (USBA)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	USB sequence bit initialization register (INISQ1)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	USB control register (USBCON)
0008 ₁₆		0028 ₁₆	Prescaler 12 (PRE12)
0009 ₁₆		0029 ₁₆	Timer 1 (T1)
000A ₁₆		002A ₁₆	Timer 2 (T2)
000B ₁₆		002B ₁₆	Timer X mode register (TM)
000C ₁₆		002C ₁₆	Prescaler X (PREX)
000D ₁₆		002D ₁₆	Timer X (TX)
000E ₁₆		002E ₁₆	Timer count source set register (TCSS)
000F ₁₆		002F ₁₆	
0010 ₁₆		0030 ₁₆	Serial I/O2 control register (SIO2CON)
0011 ₁₆		0031 ₁₆	Serial I/O2 register (SIO2)
0012 ₁₆		0032 ₁₆	
0013 ₁₆		0033 ₁₆	
0014 ₁₆		0034 ₁₆	A-D control register (ADCON)
0015 ₁₆		0035 ₁₆	A-D conversion register (low-order) (ADL)
0016 ₁₆	Pull-up control register (PULL)	0036 ₁₆	A-D conversion register (high-order) (ADH)
0017 ₁₆	Port P1P3 control register (P1P3C)	0037 ₁₆	
0018 ₁₆	Transmit/Receive buffer register (TB/RB)	0038 ₁₆	MISRG
0019 ₁₆	USB status register (USBSTS)/UART status register (UARTSTS)	0039 ₁₆	Watchdog timer control register (WDTCN)
001A ₁₆	Serial I/O1 control register (SIO1CON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART control register (UARTCON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator (BRG)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	USB data toggle synchronization register (TRSYNC)	003D ₁₆	
001E ₁₆	USB interrupt source discrimination register 1 (USBIR1)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	USB interrupt source discrimination register 2 (USBIR2)	003F ₁₆	

Fig. 10 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port. When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control] PULL

By setting the pull-up control register (address 0016₁₆), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

[Port P1P3 control] P1P3C

By setting the port P1P3 control register (address 0017₁₆), a CMOS input level or a TTL input level can be selected for ports P1₀, P1₂, P1₃, and P3₇ by program.

Then, set "1" to each bit 6 of the port P3 direction register and port P3 register.

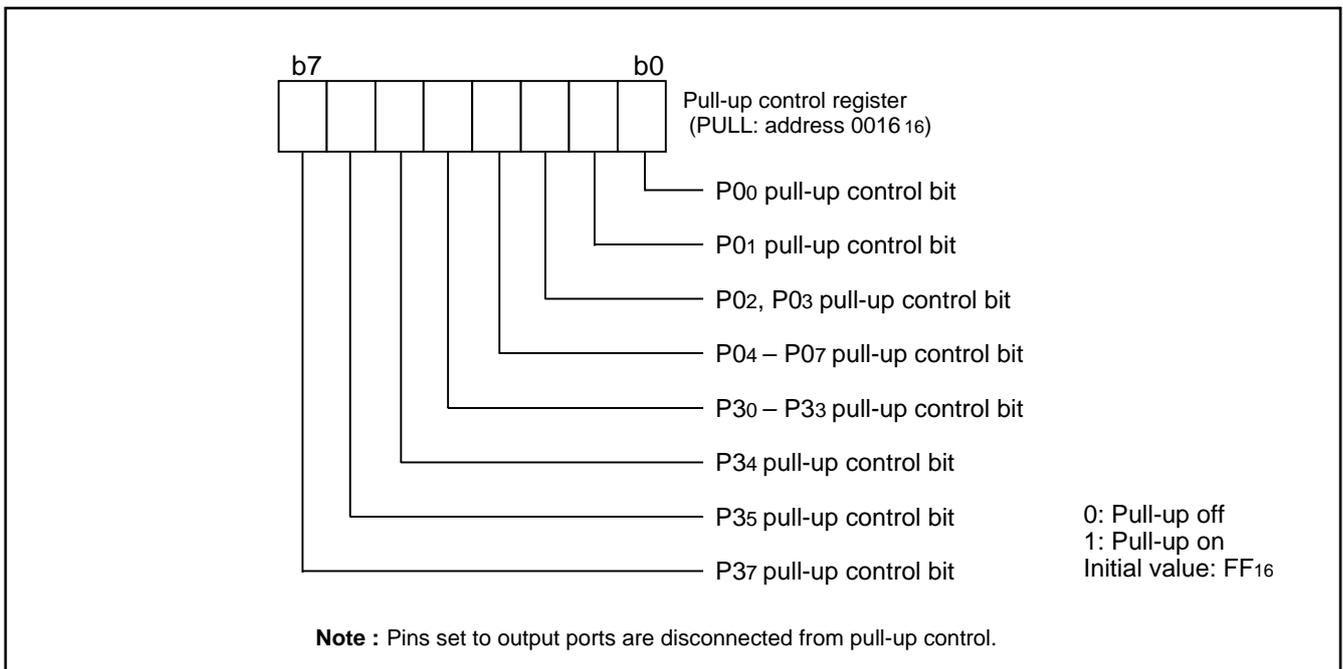


Fig. 11 Structure of pull-up control register

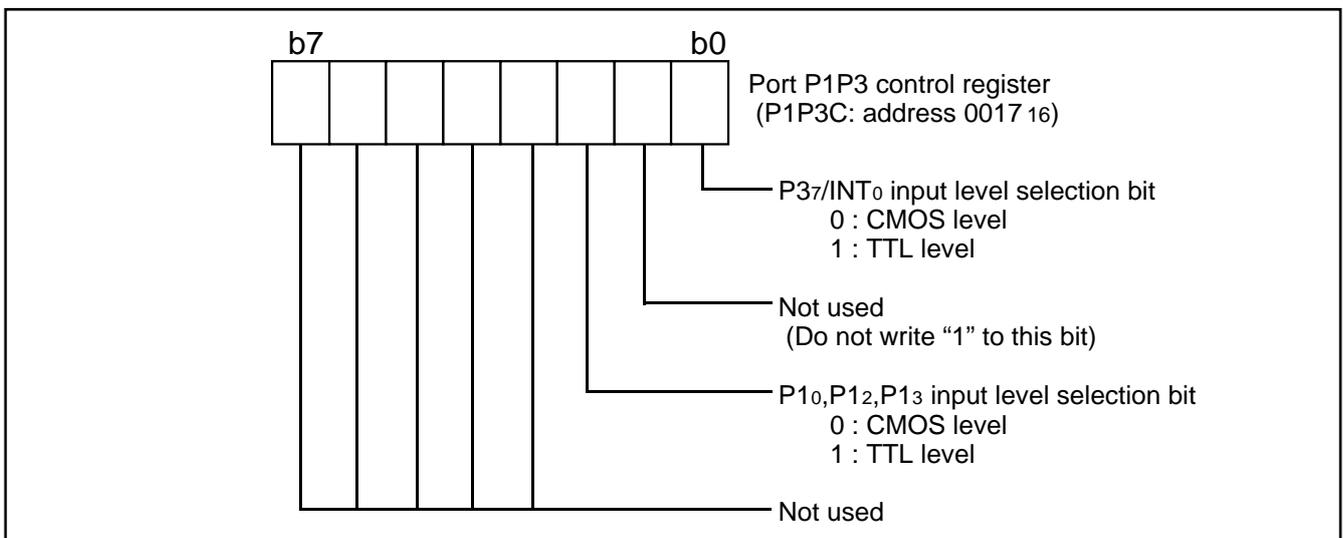


Fig. 12 Structure of port P1P3 control register

Table 3 I/O port function table

Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.	
P0 ₀ –P0 ₇	I/O port P0	I/O individual bits	<ul style="list-style-type: none"> •CMOS compatible input level •CMOS 3-state output 	Key input interrupt	Pull-up control register	(1)	
P1 ₀ /Rx/D-/P1 ₁ /Tx/D/+	I/O port P1			<ul style="list-style-type: none"> •USB input/output level when selecting USB function 	Serial I/O1 function input/output	Serial I/O1 control register	(2) (3)
P1 ₂ /SCLK P1 ₃ /SDATA				<ul style="list-style-type: none"> •CMOS compatible input level •CMOS 3-state output 	Serial I/O2 function input/output	Serial I/O2 control register	(4) (5)
P1 ₄ /CNTR ₀					Timer X function input/output	Timer X mode register	(6)
P2 ₀ /AN ₀ –P2 ₇ /AN ₇	I/O port P2				A-D conversion input	A-D control register	(7)
P3 ₀ –P3 ₅	I/O port P3						(8)
P3 ₇ /INT ₀					External interrupt input	Interrupt edge selection register	(9)

Note: Port P3₇ is CMOS/TTL level.

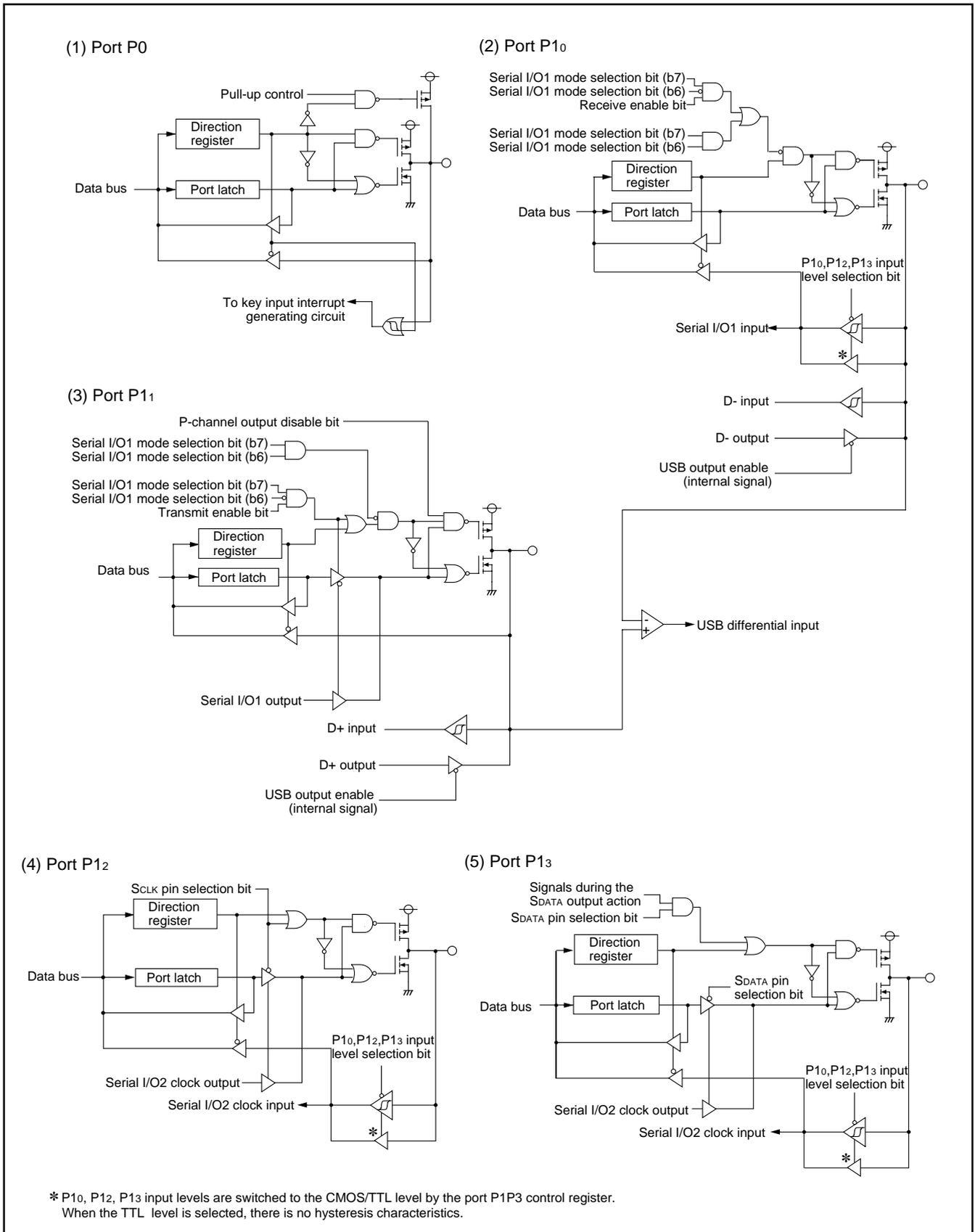


Fig. 13 Block diagram of ports (1)

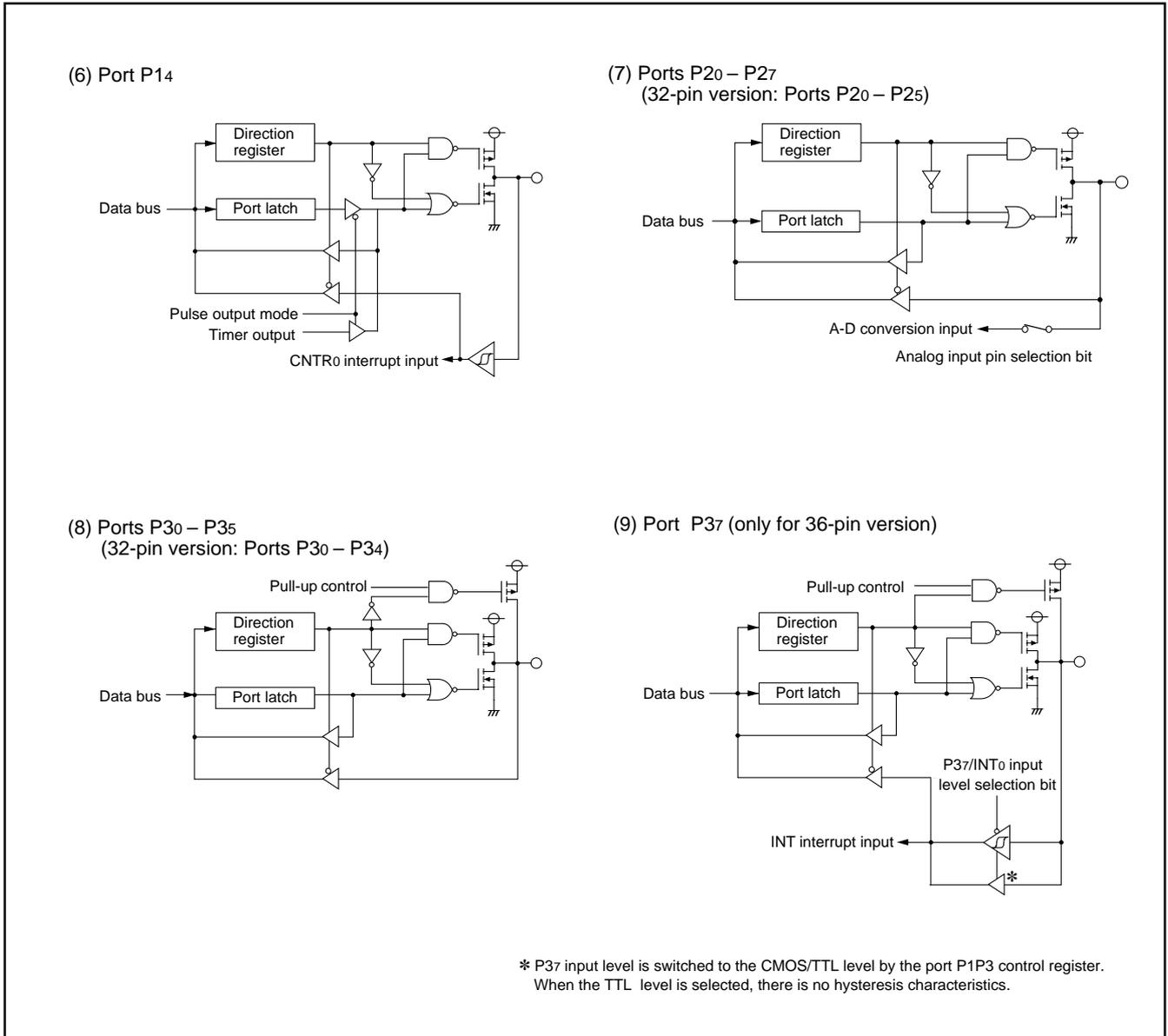


Fig. 14 Block diagram of ports (2)

Interrupts

Interrupts occur by 13 different sources : 3 external sources, 9 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to "1" and the interrupt disable flag is set to "0", an interrupt is accepted.

The interrupt request bit can be cleared by program but not be set.

The interrupt enable bit can be set and cleared by program.

It becomes usable by switching CNTR₀ and AD interrupt sources with bit 7 of the interrupt edge selection register, timer 2 and serial I/O2 interrupt sources with bit 6, and timer X and key-on wake-up interrupt sources with bit 5.

The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

Notes on use

When the active edge of an external interrupt (INT₀, CNTR₀) is set, the interrupt request bit may be set.

Therefore, please take following sequence:

1. Disable the external interrupt which is selected.
2. Change the active edge in interrupt edge selection register. (in case of CNTR₀: Timer X mode register)
3. Clear the set interrupt request bit to "0".
4. Enable the external interrupt which is selected.

Table 4 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset input	Non-maskable
UART receive	2	FFFB ₁₆	FFFA ₁₆	At completion of UART data receive	Valid in UART mode
USB IN token				At detection of IN token	Valid in USB mode
UART transmit	3	FFF9 ₁₆	FFF8 ₁₆	At completion of UART transmit shift or when transmit buffer is empty	Valid in UART mode
USB SETUP/OUT token Reset/Suspend/Resume				At detection of SETUP/OUT token or At detection of Reset/ Suspend/ Resume	Valid in USB mode
INT ₀	4	FFF7 ₁₆	FFF6 ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
Timer X	5	FFF5 ₁₆	FFF4 ₁₆	At timer X underflow	External interrupt (valid at falling)
Key-on wake-up				At falling of conjunction of input logical level for port P0 (at input)	
Timer 1	6	FFF3 ₁₆	FFF2 ₁₆	At timer 1 underflow	STP release timer underflow
Timer 2	7	FFF1 ₁₆	FFF0 ₁₆	At timer 2 underflow	
Serial I/O2				At completion of transmit/receive shift	
CNTR ₀	8	FFEF ₁₆	FFEE ₁₆	At detection of either rising or falling edge of CNTR ₀ input	External interrupt (active edge selectable)
A-D conversion				At completion of A-D conversion	
BRK instruction	9	FFED ₁₆	FFEC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

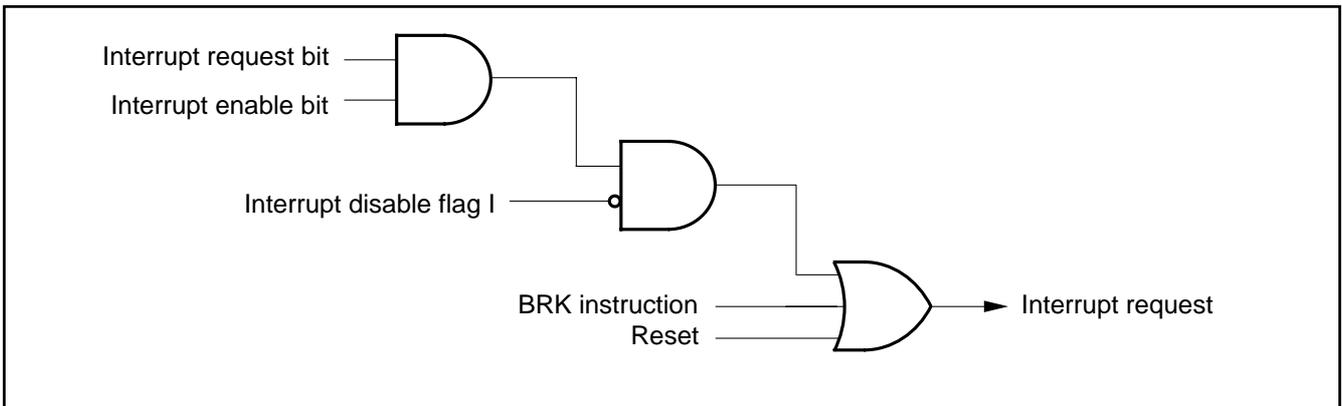


Fig. 15 Interrupt control

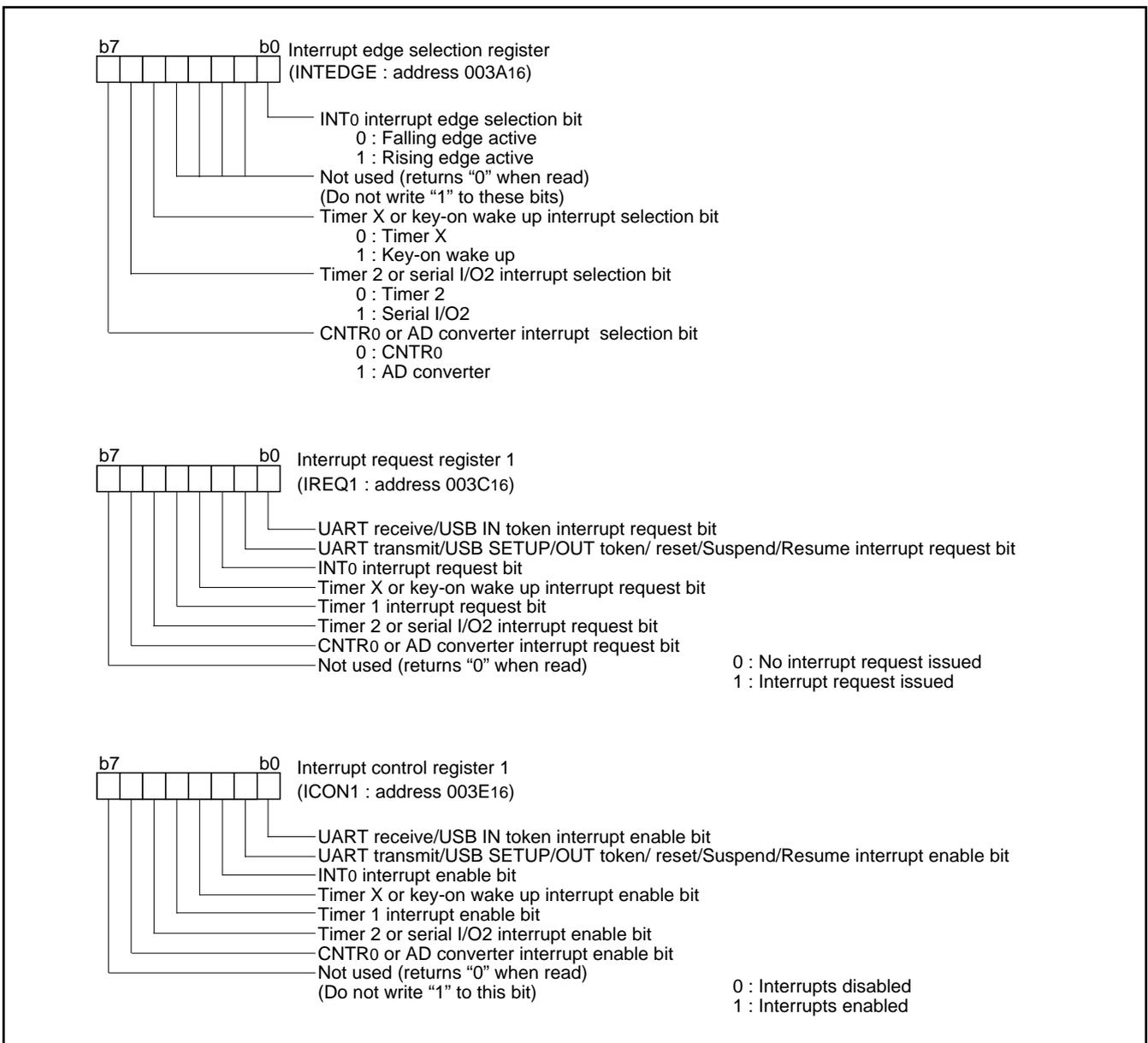


Fig. 16 Structure of Interrupt-related registers

Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying "L" level to any pin of port P0 that has been set to input mode.

In other words, it is generated when the AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 17, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P0 to P03 as input ports.

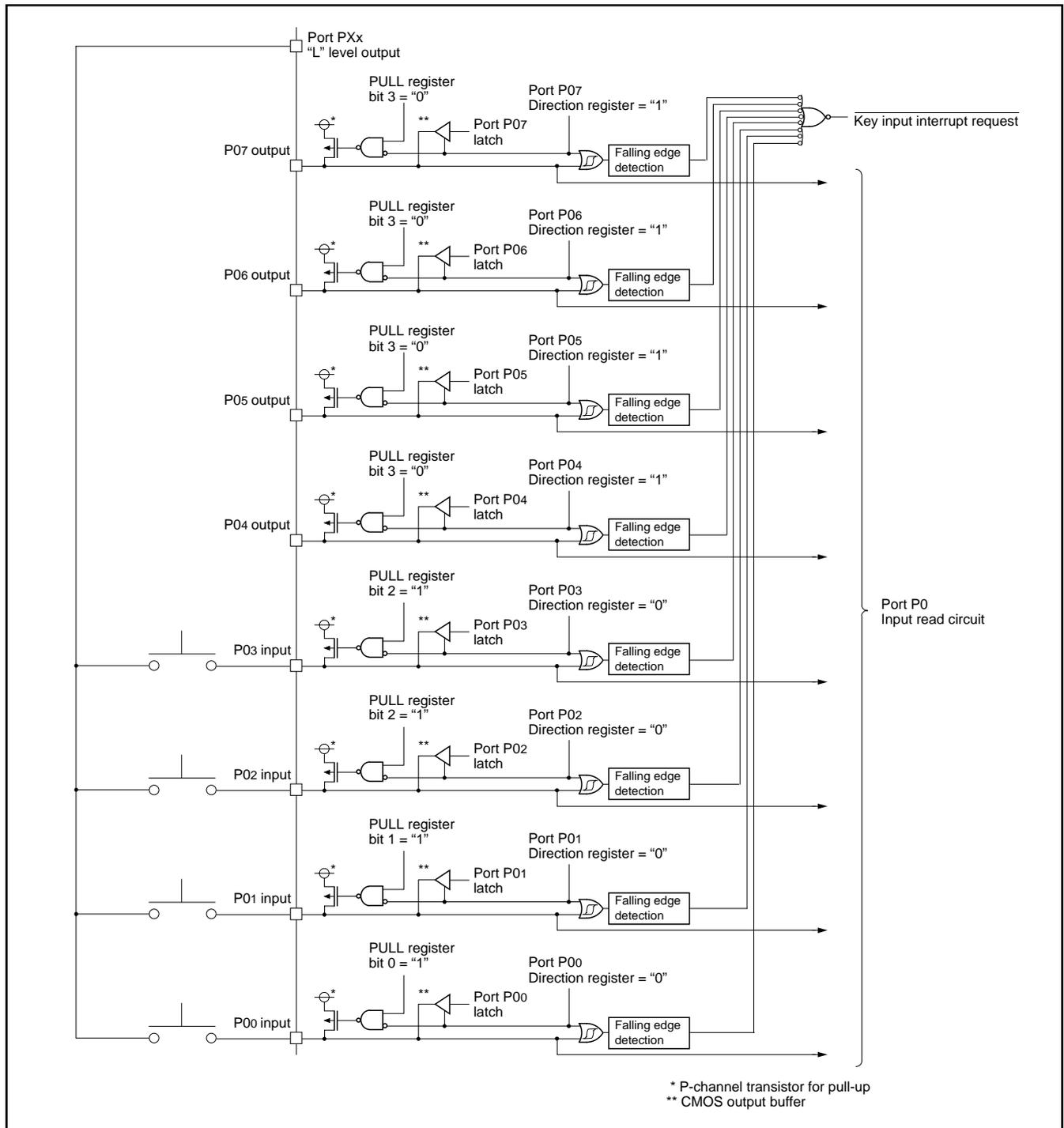


Fig. 17 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7532 Group has 3 timers: timer X, timer 1 and timer 2. The division ratio of every timer and prescaler is $1/(n+1)$ provided that the value of the timer latch or prescaler is n .

All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

●Timer 1, Timer 2

Prescaler 12 always counts $f(X_{IN})/16$. Timer 1 and timer 2 always count the prescaler output and periodically sets the interrupt request bit.

●Timer X

Timer X can be selected in one of 4 operating modes by setting the timer X mode register.

• Timer Mode

The timer counts the signal selected by the timer X count source selection bit.

• Pulse Output Mode

The timer counts the signal selected by the timer X count source selection bit, and outputs a signal whose polarity is inverted each time the timer value reaches "0", from the CNTR₀ pin.

When the CNTR₀ active edge switch bit is "0", the output of the CNTR₀ pin is started with an "H" output.

At "1", this output is started with an "L" output. When using a timer in this mode, set the port P14 direction register to output mode.

• Event Counter Mode

The operation in the event counter mode is the same as that in the timer mode except that the timer counts the input signal from the CNTR₀ pin.

When the CNTR₀ active edge switch bit is "0", the timer counts the rising edge of the CNTR₀ pin. When this bit is "1", the timer counts the falling edge of the CNTR₀ pin.

• Pulse Width Measurement Mode

When the CNTR₀ active edge switch bit is "0", the timer counts the signal selected by the timer X count source selection bit while the CNTR₀ pin is "H". When this bit is "1", the timer counts the signal while the CNTR₀ pin is "L".

In any mode, the timer count can be stopped by setting the timer X count stop bit to "1". Each time the timer overflows, the interrupt request bit is set.

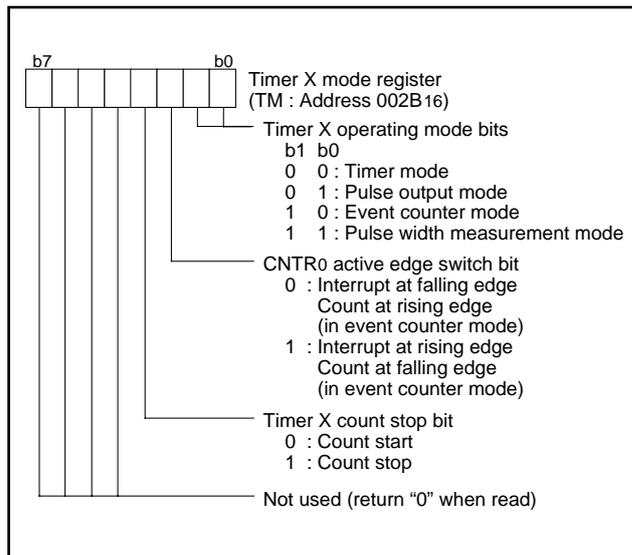


Fig. 18 Structure of timer X mode register

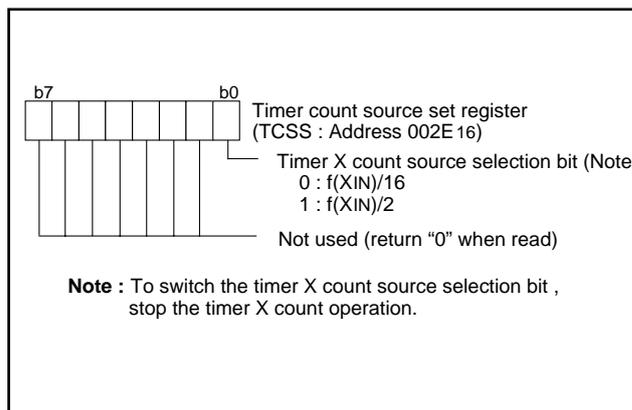


Fig. 19 Timer count source set register

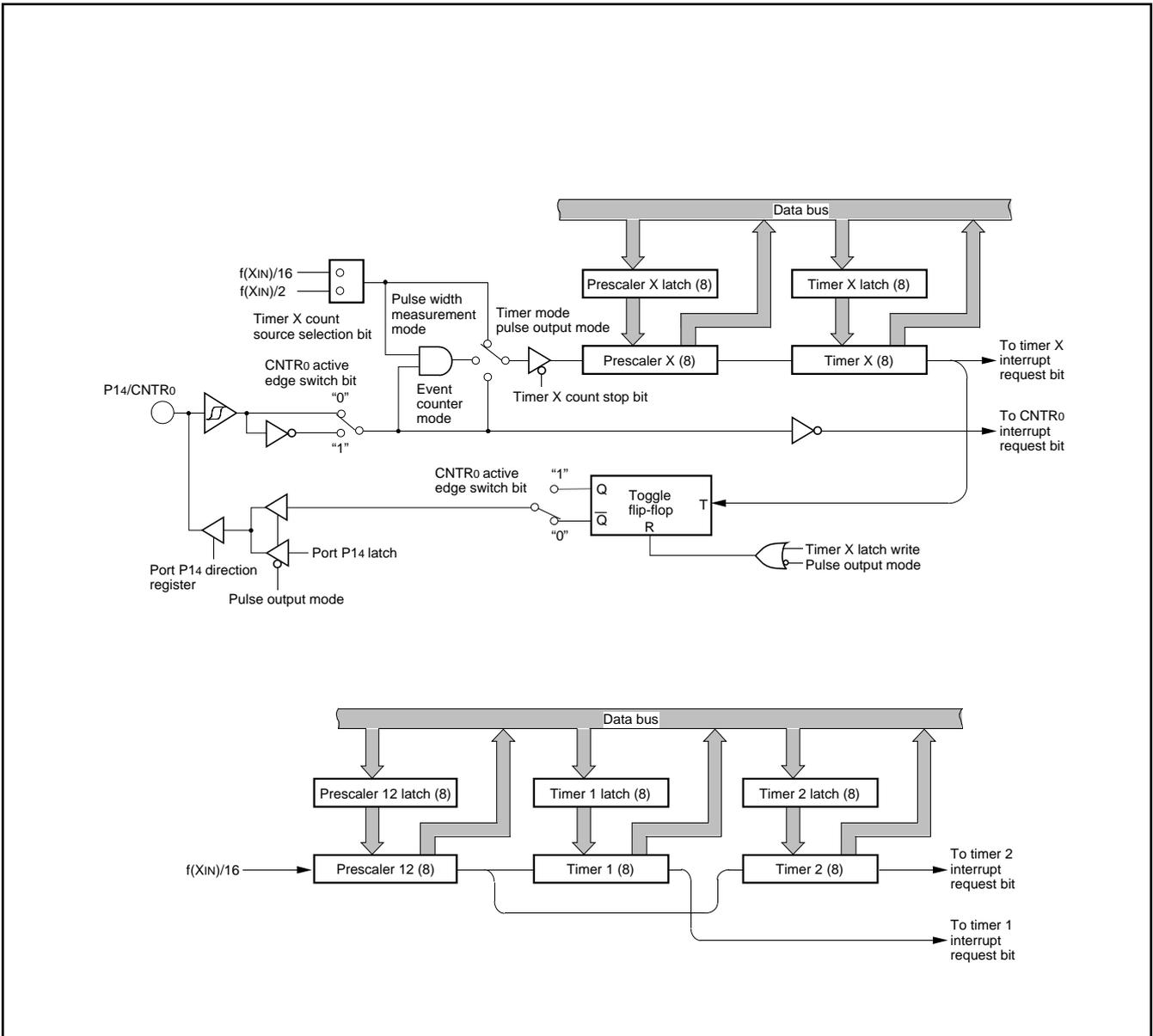


Fig. 20 Block diagram of timer X, timer 1 and timer 2

Serial I/O

●Serial I/O1

• Asynchronous serial I/O (UART) mode

Serial I/O1 can be used as an asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation when serial I/O1 is in operation.

Eight serial data formats can be selected, and the transfer formats to be used by a transmitter and a receiver must be identical.

Each of the transmit and receive shift registers has a buffer register

(the same address on memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the respective buffer registers. These buffer registers can also hold the next data to be transmitted and receive 2-byte receive data in succession.

By selecting "1" for continuous transmit valid bit (bit 2 of SIO1CON), continuous transmission of the same data is made possible. This can be used as a simplified PWM.

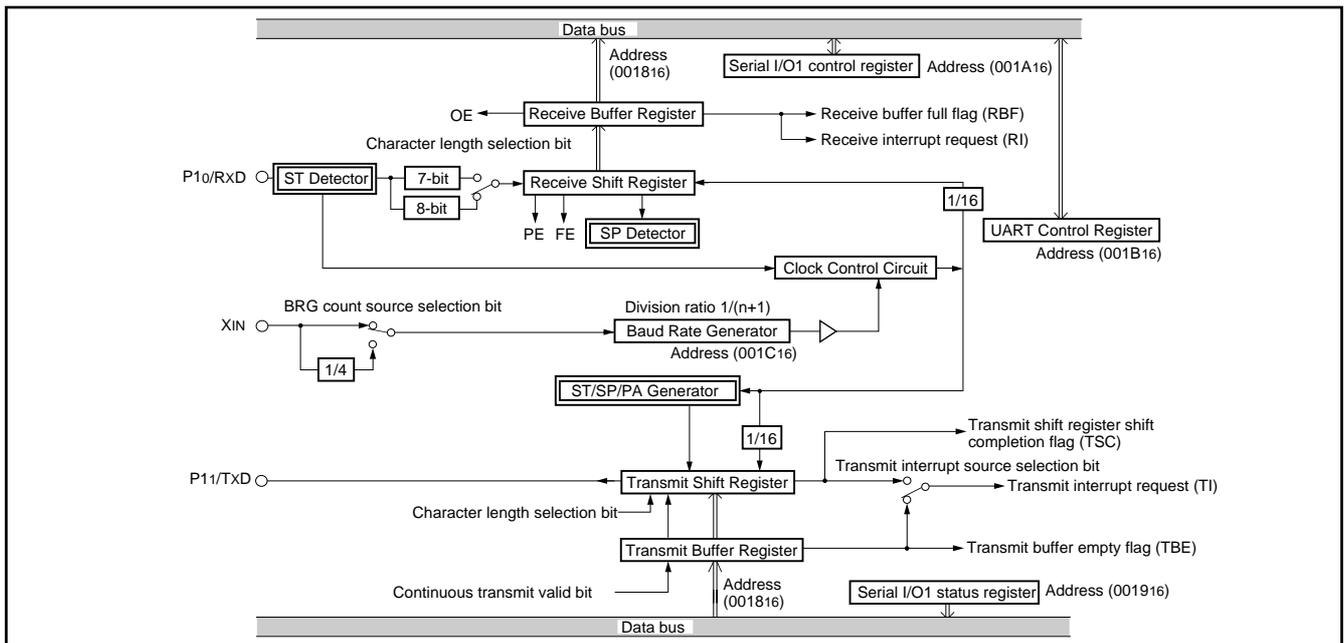


Fig. 21 Block diagram of UART serial I/O

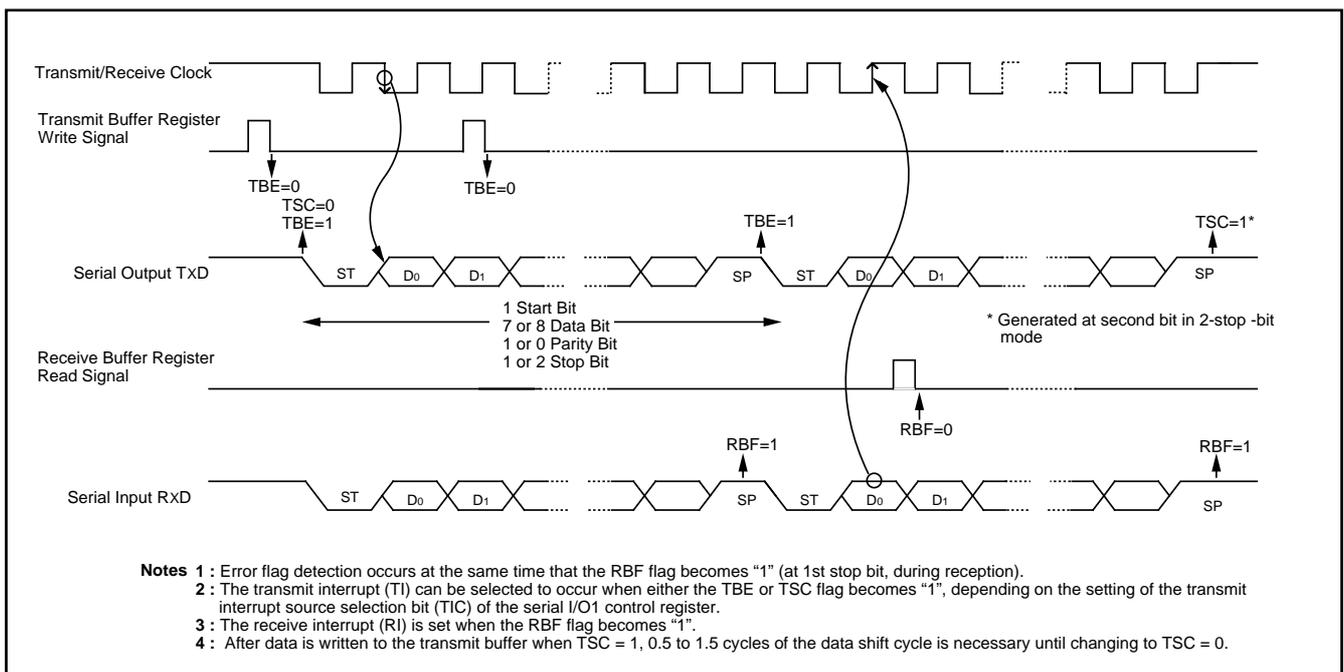


Fig. 22 Operation of UART serial I/O function

[Serial I/O1 control register] SIO1CON

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART control register] UARTCON

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P11/TxD pin.

[UART status register] UARTSTS

The read-only UART status register consists of seven flags (bits 0 to 6) which indicate the operating status of the UART function and various errors. This register functions as the UART status register (UARTSTS) when selecting the UART.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the UART status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 mode selection bits MOD1 and MOD0 (bit 7 and 6 of the Serial I/O1 control register) also clears all the status flags, including the error flags.

All bits of the serial I/O1 status register are initialized to "8116" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the continuous transmit valid bit (bit 2) becomes "1".

[Transmit/Receive buffer register] TB/RB

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7-bit, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator] BRG

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

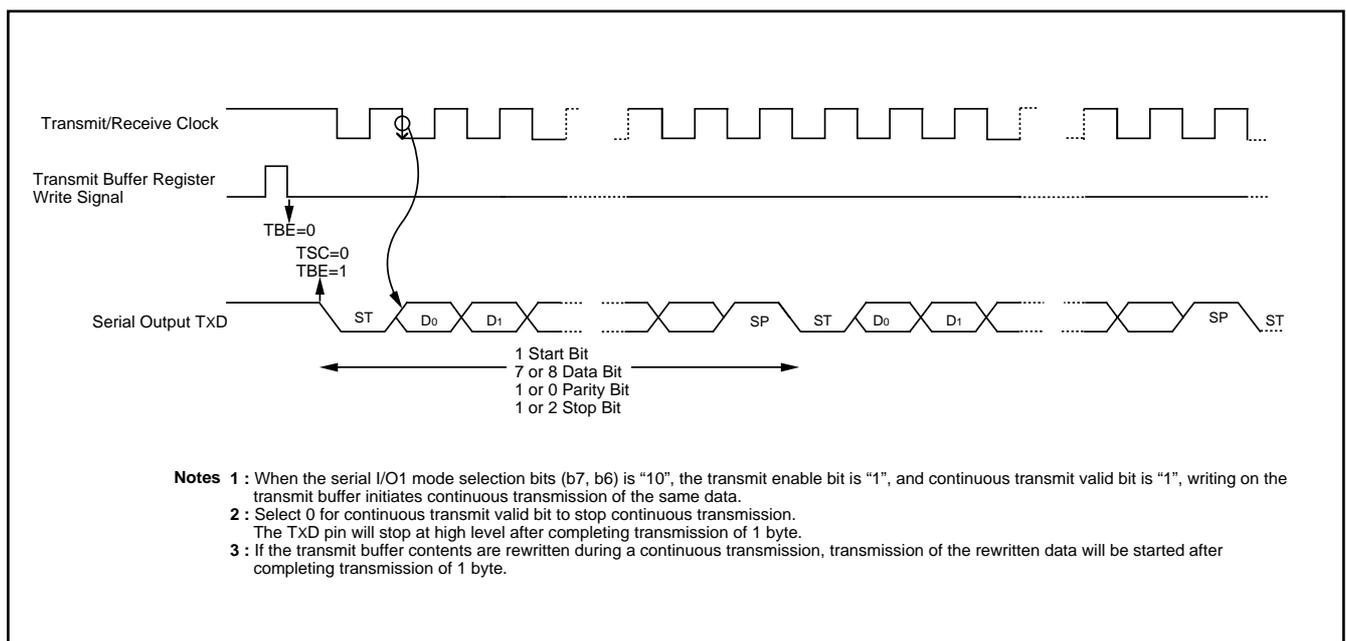


Fig. 23 Continuous transmission operation of UART serial I/O

• Universal serial bus (USB) mode

By setting bits 7 and 6 of the serial I/O1 control register (address 001A16) to "11", the USB mode is selected.

This mode conforms to "Low Speed device" of USB Specification 1.0. In this mode serial I/O1 interrupt have 5 sources; USB in and out token receive, USB reset, suspend, and resume. The USB

status/UART status register functions as the USB status register (USBSTS). There is the USBVREFOUT pin for the USB reference voltage output, and a D-line with 1.5 kΩ external resistor can be pull up. USB mode block and USB transceiver block show in figures 24 and 25.

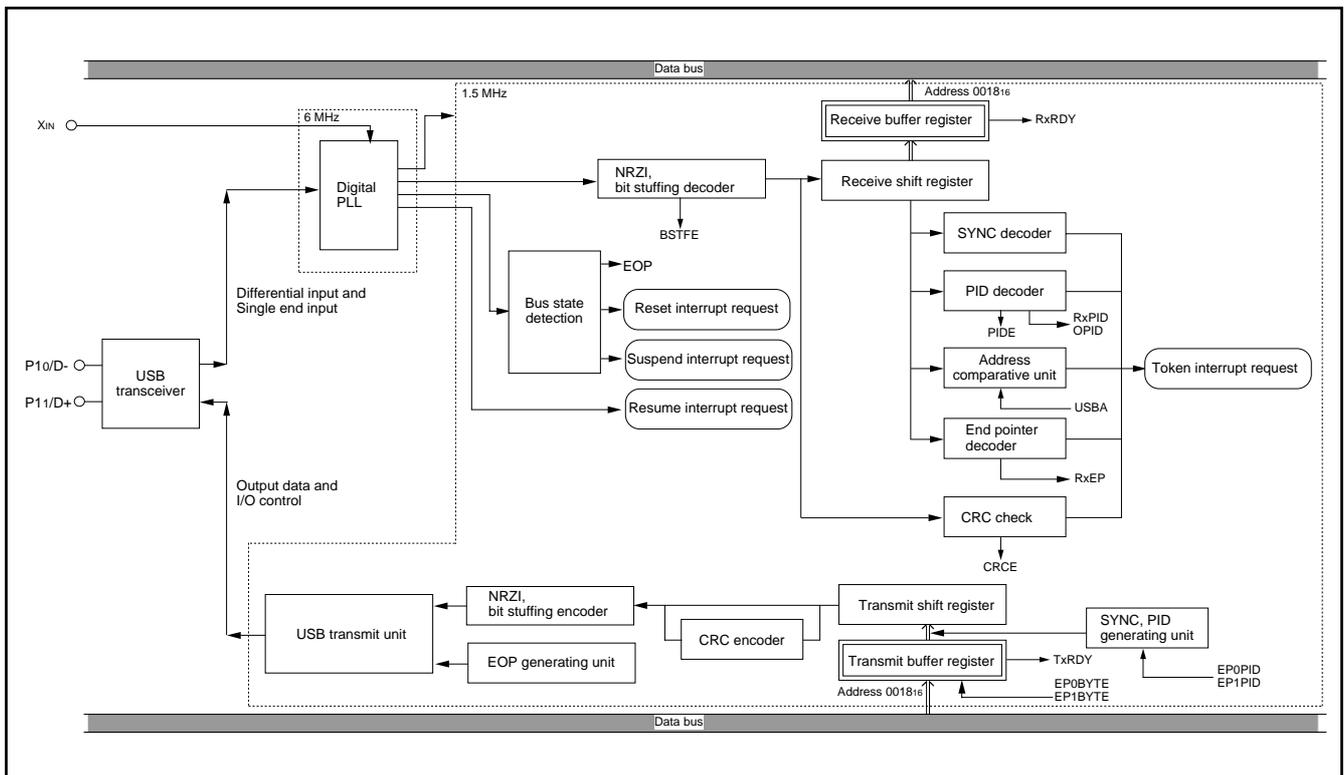


Fig. 24 USB mode block diagram

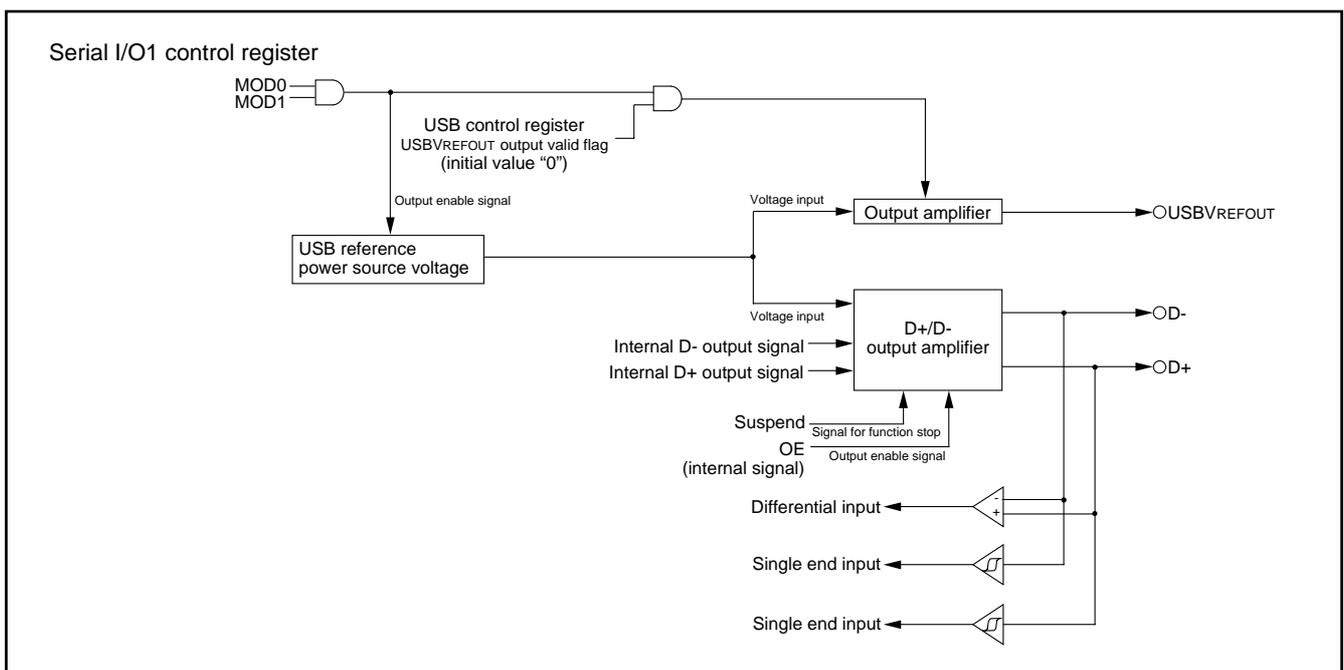


Fig. 25 USB transceiver block diagram

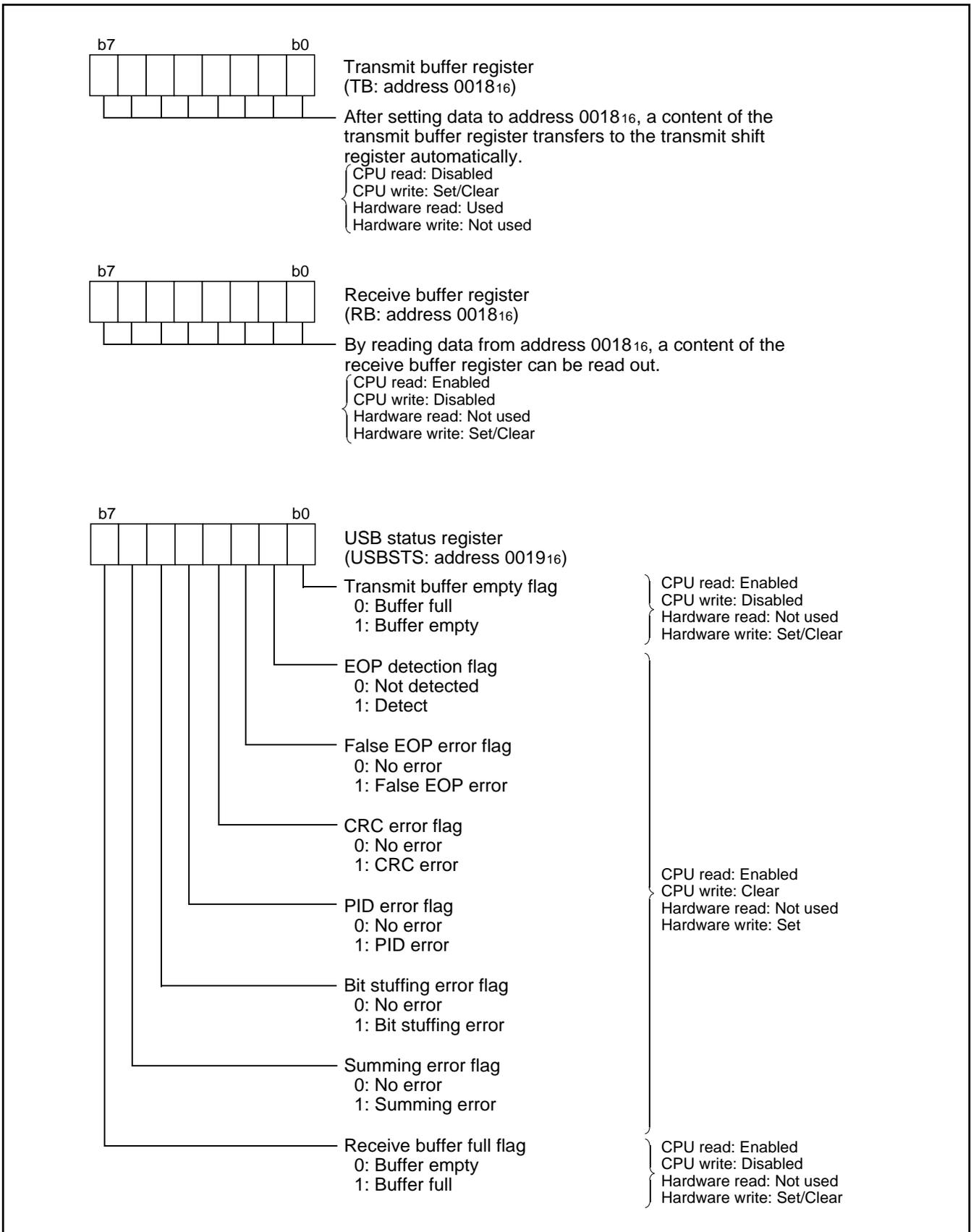


Fig. 26 Structure of serial I/O1-related registers (1)

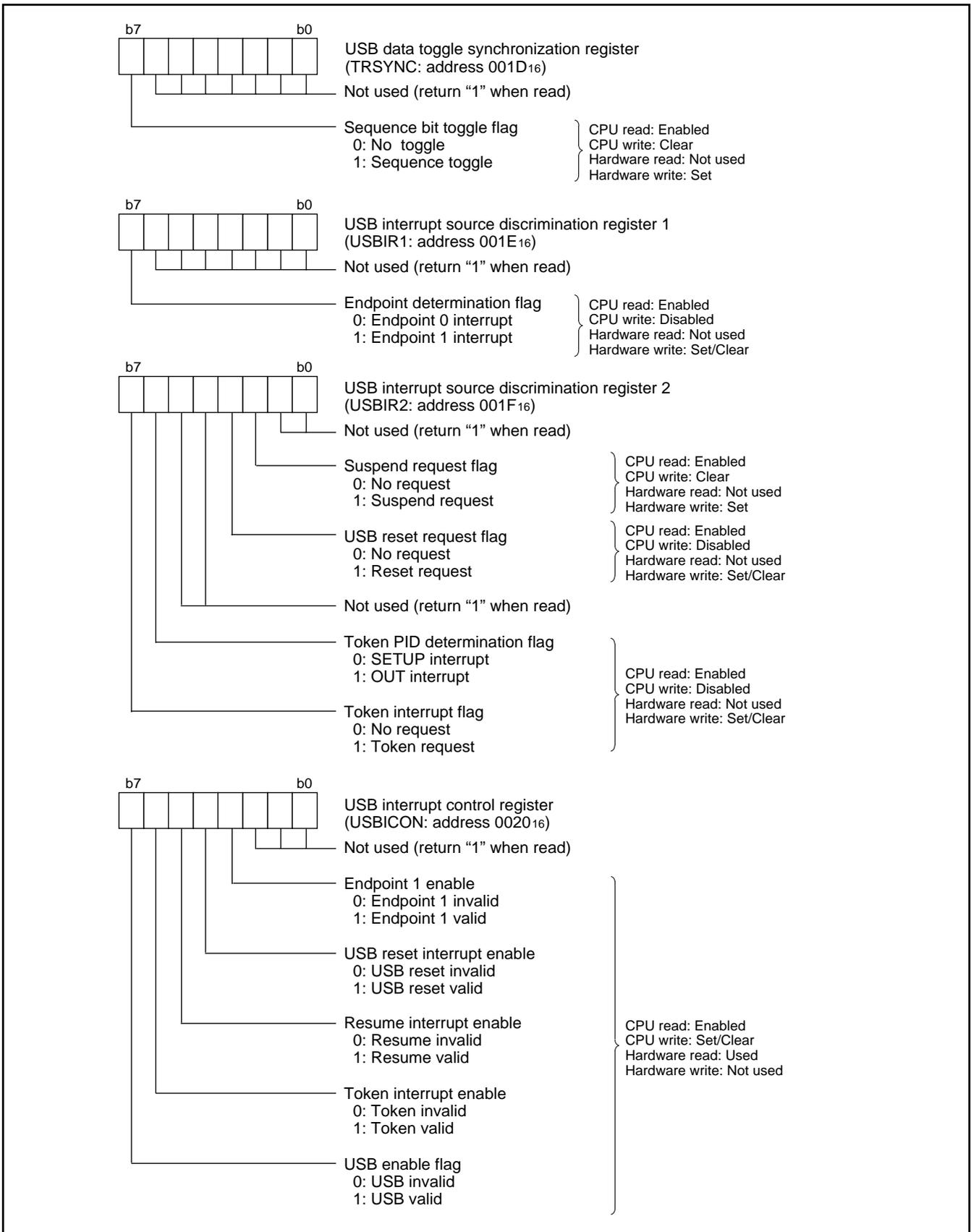


Fig. 27 Structure of serial I/O1-related registers (2)

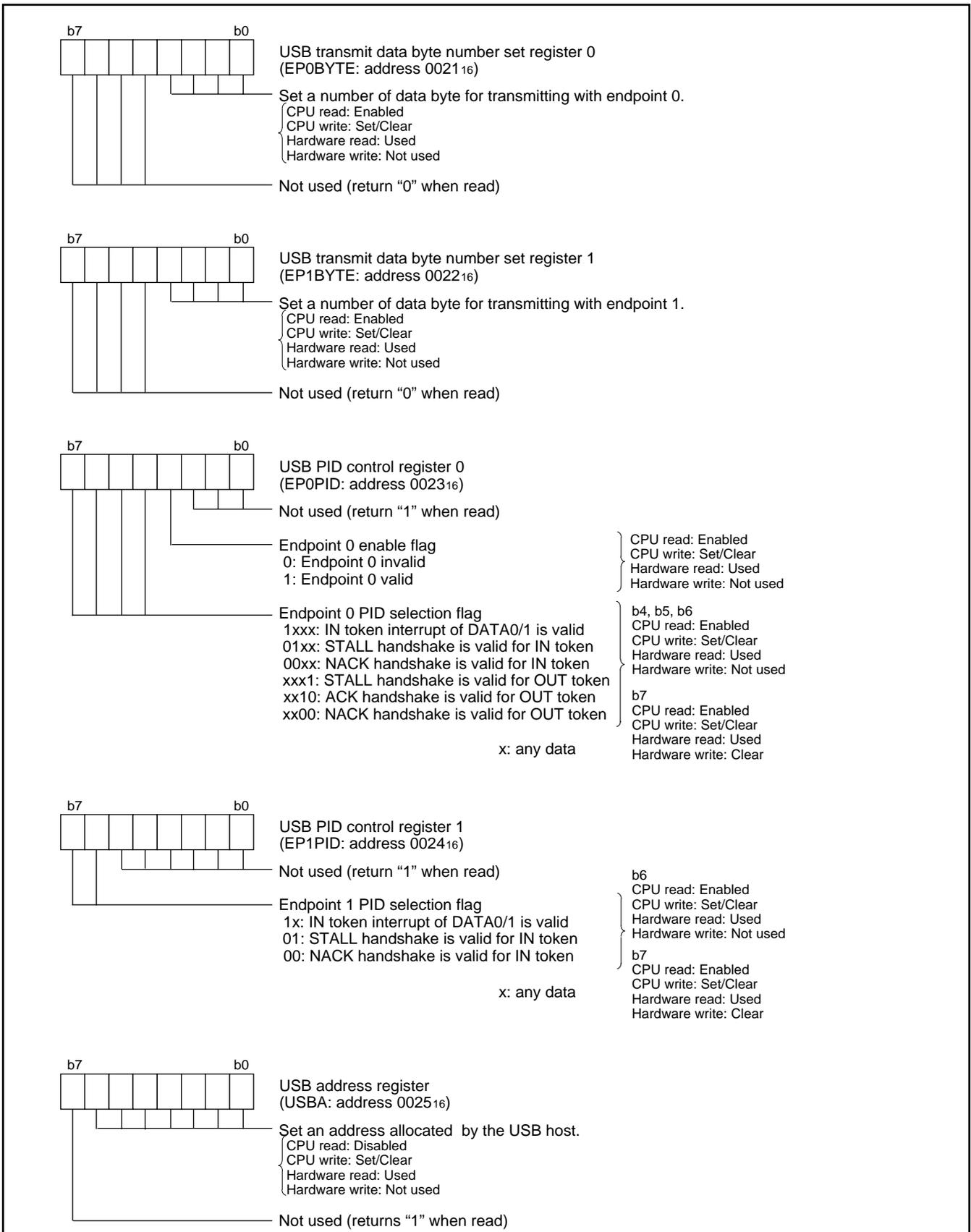


Fig. 28 Structure of serial I/O1-related registers (3)

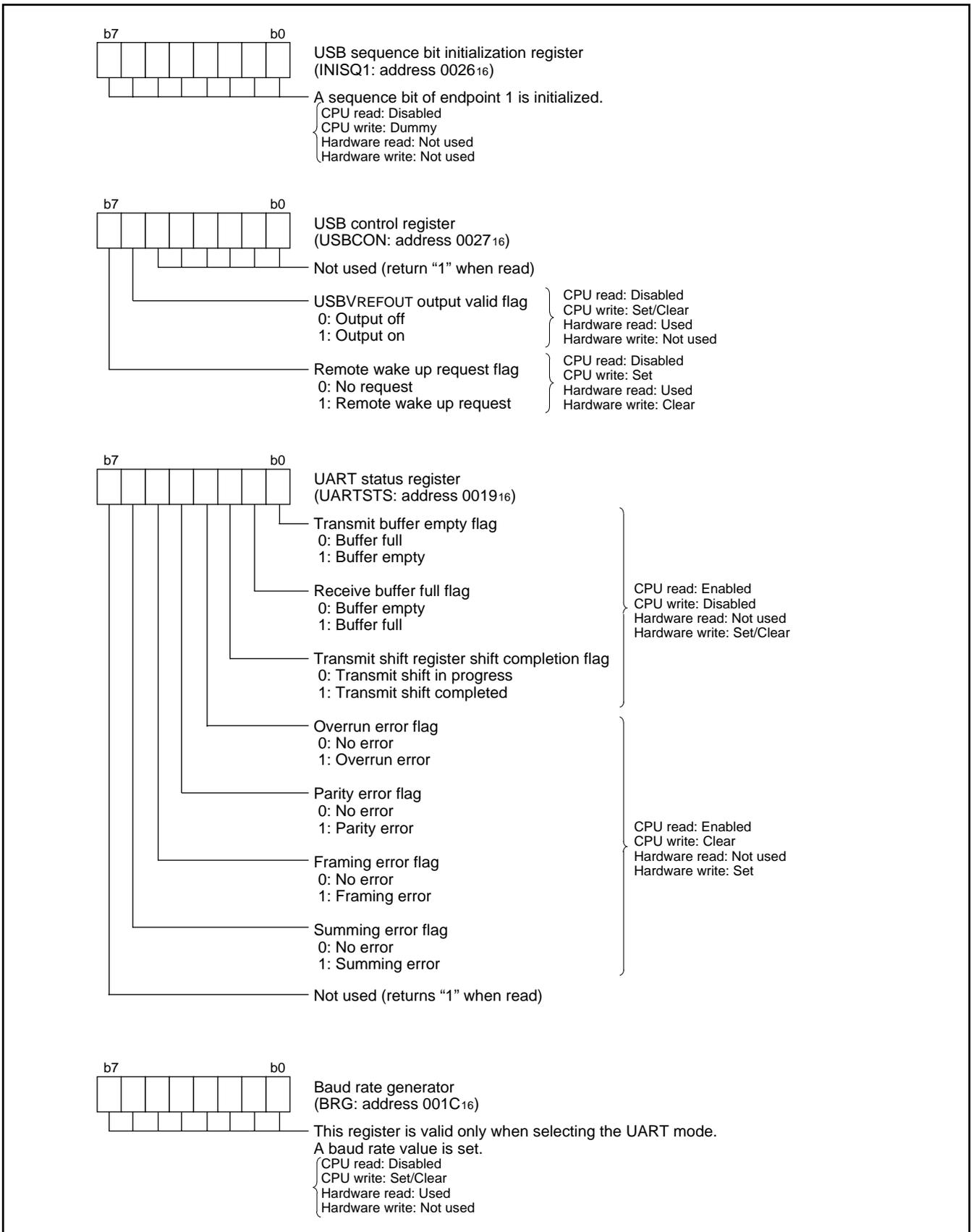


Fig. 29 Structure of serial I/O1-related registers (4)

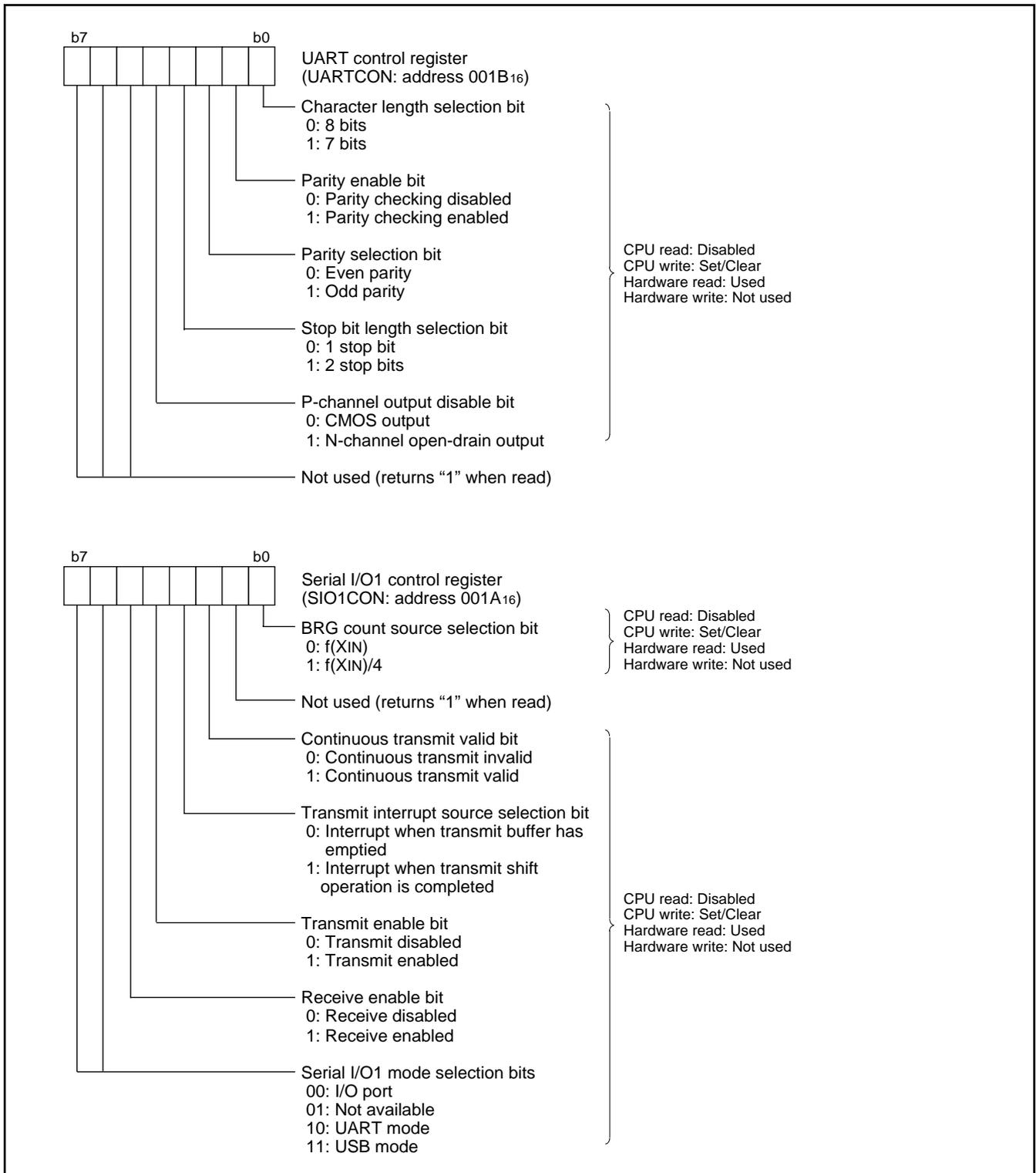


Fig. 30 Structure of serial I/O1-related registers (5)

Note on using USB mode

Handling of SE0 signal in program (at receiving)

7532 group has the border line to detect as USB RESET or EOP (End of Packet) on the width of SE0 (Single Ended 0).

A response apposite to a state of the device is expected.

The name of the following short words which is used in table 5 shows as follow.

- TKNE: Token interrupt enable (bit 6 of address 20₁₆)
- RSME: Resume interrupt enable (bit 5 of address 20₁₆)
- RSTE: USB reset interrupt enable (bit 4 of address 20₁₆)
- Spec: A response of the device requested by USB Specification 1.0
- SIE: Hardware operation in 7532 group
- F/W: Recommendation process in the program
- FEOPE: False EOP error flag (bit 2 of address 19₁₆)
- RxPID: Token interrupt flag (bit 7 of address 1F₁₆)

Table 5 Relation of the width of SE0 and the state of the device

		State of device					
Width of SE0		Idle state TKNE = X RSME = 0 RSTE =1	End of Token in transaction TKNE = 1 RSME = 0 RSTE =1	End of data or handshake in transaction TKNE = 0 RSME = 0 RSTE = 0 or 1	Suspend state TKNE = 0 RSME = 1 RSTE = 0		
	0 μ sec. 0.5 μ sec.	Spec	Ignore	Ignore	Ignore	Spec	Reset or resume
SIE		Keep counting suspend timer	Not detected as EOP(in case of no detection EOP, SIE returns idle state as time out. FEOPE flag is set.)	Not detected as EOP(in case of no detection EOP, SIE returns idle state as timeup. FEOPE flag is set.)			
F/W		Not acknowledge	Not acknowledge	Wait for the next EOP flag			
0.5 μ sec. 2.5 μ sec.	Spec	Keep alive	EOP	EOP	SIE	Reset interrupt request	
	SIE	Initialize suspend timer count value	Token interrupt request	Set EOP flag			
	F/W	Not acknowledge	Token interrupt processing execute	After checking the set of EOP flag, go to the next processing			
2.5 μ sec. 2.67 μ sec.	Spec	Keep alive or Reset	EOP or Reset	EOP or Reset	F/W	Reset interrupt processing Resume interrupt processing	
	SIE	may determine as keep alive and Reset interrupt	may determine as EOP and Reset interrupt	may determine as EOP and Reset interrupt			
	F/W	Keep alive in case of no interrupt request Reset processing in case of interrupt request	RxPID = 1> Token interrupt processing RxPID = 0> Reset interrupt processing	Continue the processing in case of no interrupt request Reset processing in case of interrupt request			
2.67 μ sec.	Spec	Reset	Reset	Reset			
	SIE	Reset interrupt request	Reset interrupt request	Reset interrupt request			
	F/W	Reset processing	Reset processing	Reset processing			

●Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2 the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8 bits which control various serial I/O functions.

- For receiving, set "0" to bit 3.
- When receiving, bit 7 is cleared by writing dummy data to serial I/O2 register after shift is completed.
- Bit 7 is set earlier a half cycle of shift clock than completion of shift operation. Accordingly, when checking shift completion by using this bit, the setting is as follows:
 - (1) check that this bit is set to "1",
 - (2) wait a half cycle of shift clock,
 - (3) read/write to serial I/O2 register.

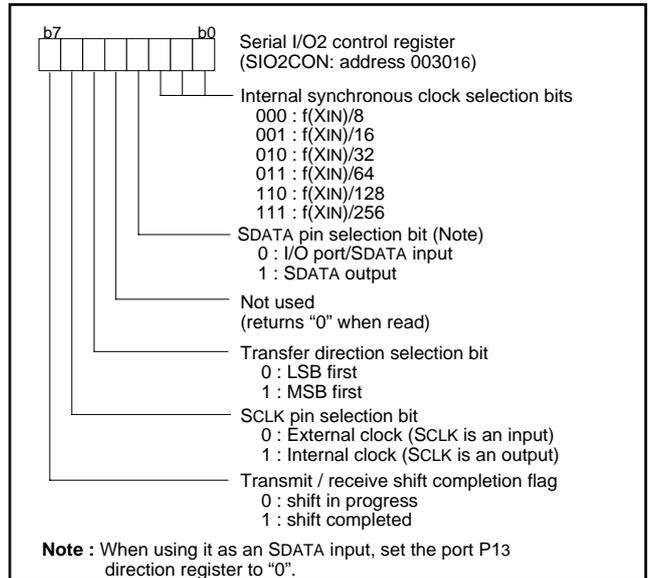


Fig. 31 Structure of serial I/O2 control registers

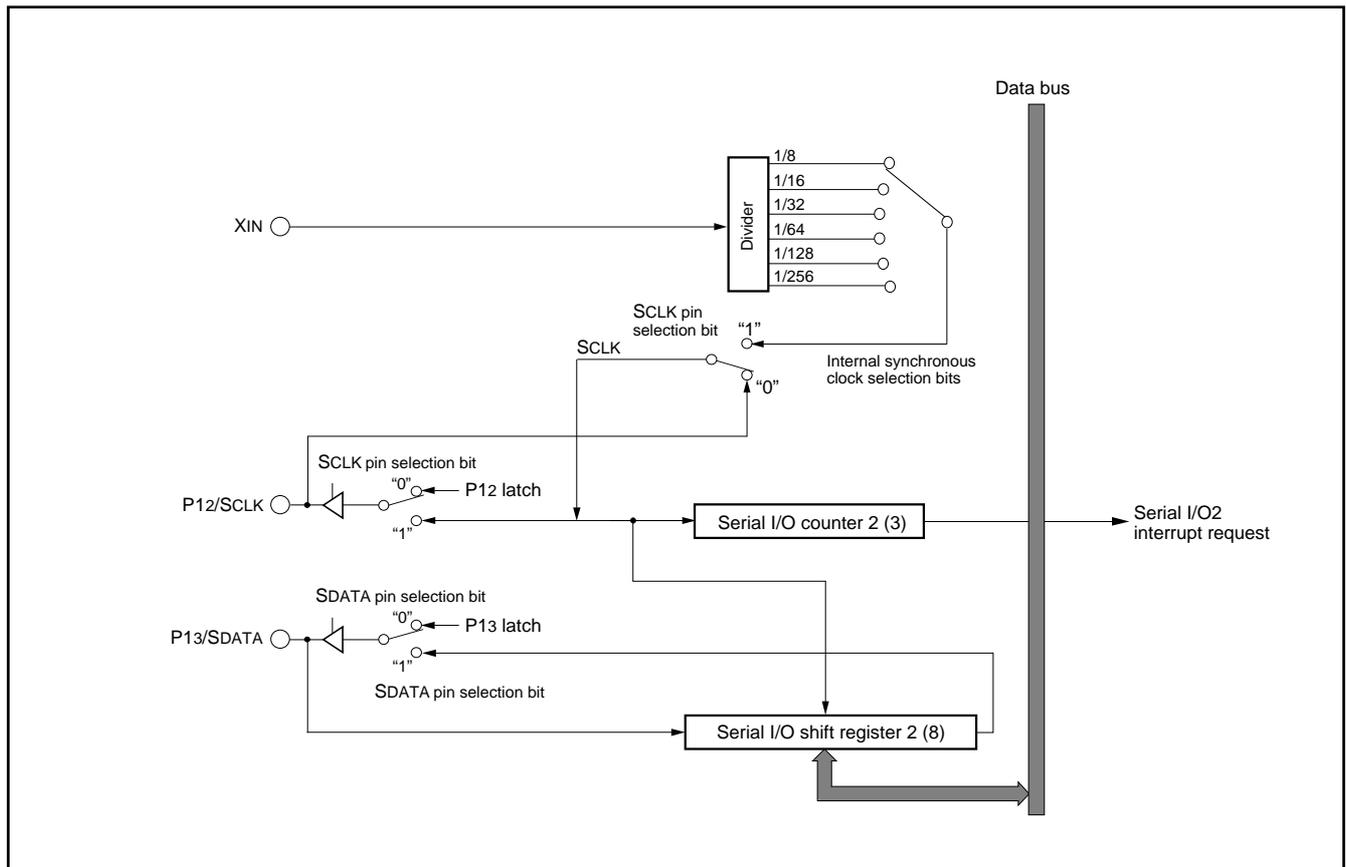


Fig. 32 Block diagram of serial I/O2

Serial I/O2 operation

By writing to the serial I/O2 register(address 0031₁₆) the serial I/O2 counter is set to "7".

After writing, the SDATA pin outputs data every time the transfer clock shifts from a high to a low level. And, as the transfer clock shifts from a low to a high, the SDATA pin reads data, and at the same time the contents of the serial I/O2 register are shifted by 1 bit.

When the internal clock is selected as the transfer clock source, the following operations execute as the transfer clock counts up to 8.

- Serial I/O2 counter is cleared to "0".
- Transfer clock stops at an "H" level.
- Interrupt request bit is set.
- Shift completion flag is set.

Also, the SDATA pin is in a high impedance state after the data transfer is complete (refer to figure 33).

When the external clock is selected as the transfer clock source, the interrupt request bit is set as the transfer clock counts up to 8, but external control of the clock is required since it does not stop. Notice that the SDATA pin is not in a high impedance state on the completion of data transfer.

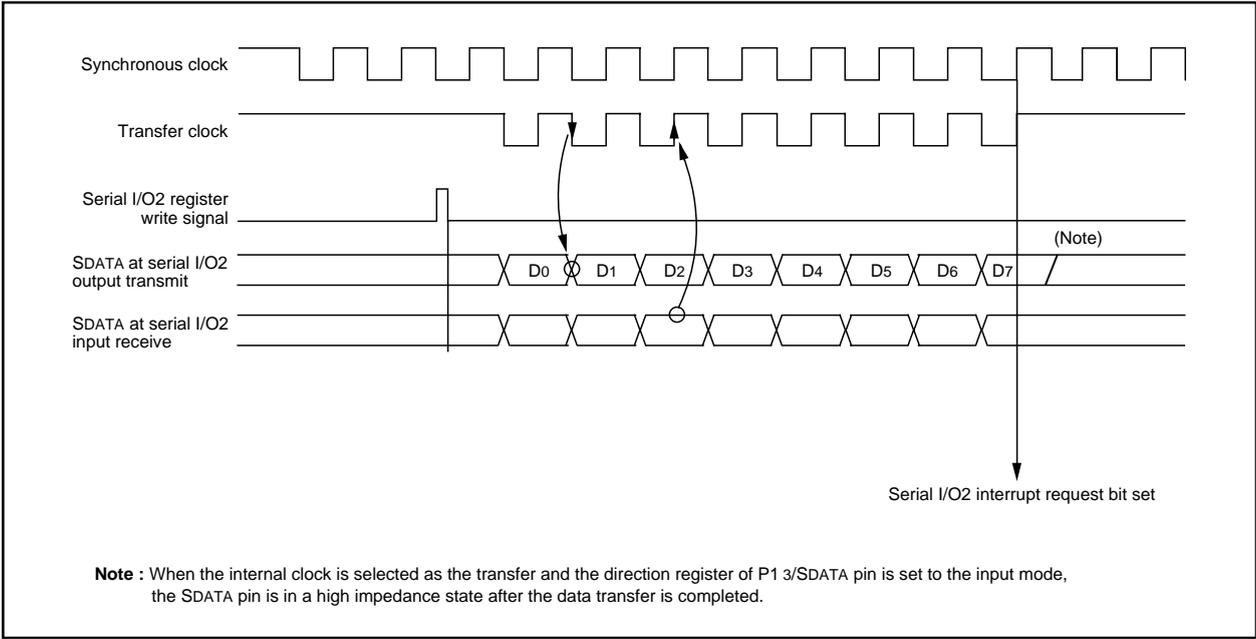


Fig. 33 Serial I/O2 timing (LSB first)

A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

[A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during A-D conversion, and changes to "1" at completion of A-D conversion. A-D conversion is started by setting this bit to "0".

[Comparison voltage generator]

The comparison voltage generator divides the voltage between V_{SS} and V_{REF} by 1024 by a resistor ladder, and outputs the divided voltages. Since the generator is disconnected from V_{REF} pin and V_{SS} pin, current is not flowing into the resistor ladder.

[Channel Selector]

The channel selector selects one of ports P27/AN7 to P20/AN0, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set f(XIN) to 500 kHz or more during A-D conversion.

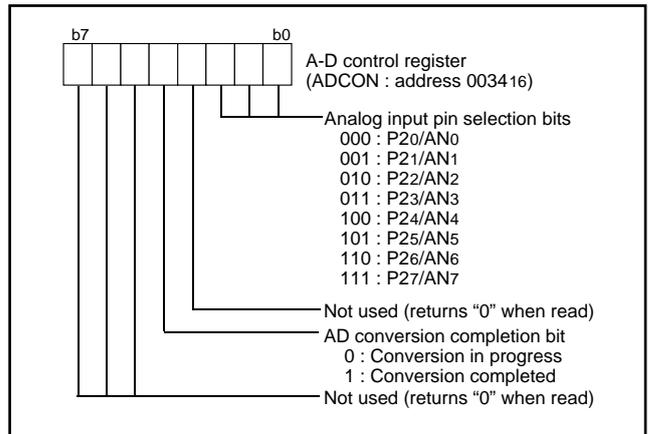


Fig. 34 Structure of A-D control register

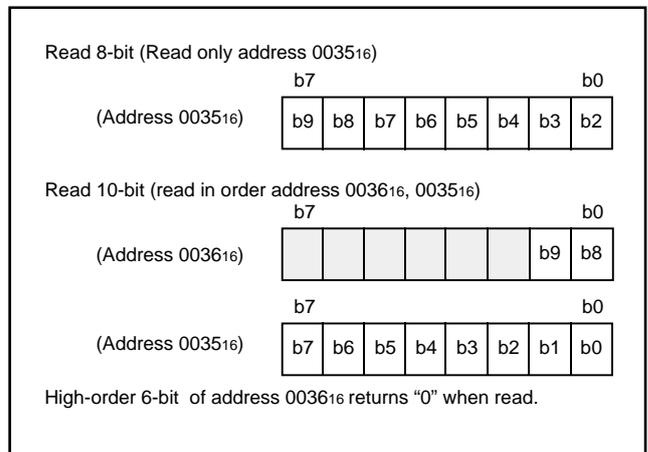


Fig. 35 Structure of A-D conversion register

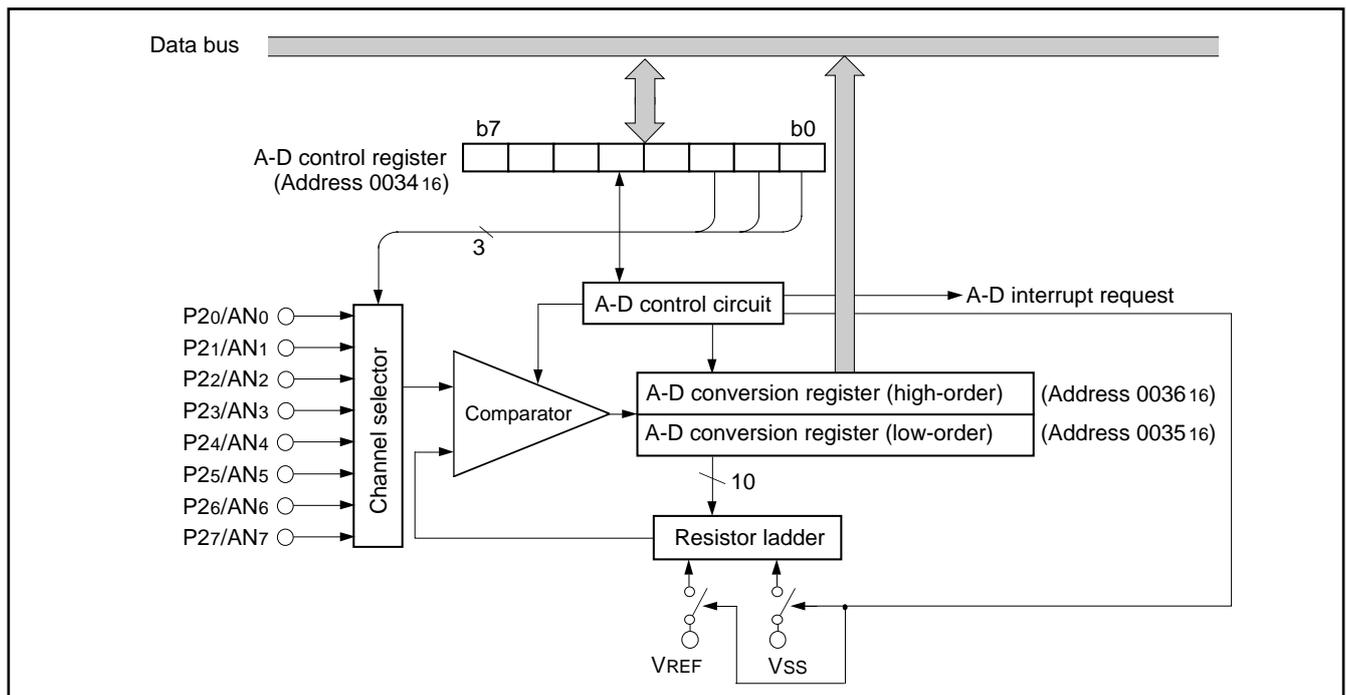


Fig. 36 Block diagram of A-D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039₁₆) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039₁₆) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039₁₆) can be set before an underflow occurs.

When the watchdog timer control register (address 0039₁₆) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039₁₆), the watchdog timer H is set to "FF₁₆" and the watchdog timer L is set to "FF₁₆".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039₁₆). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 174.763 ms at f(XIN)=6 MHz. When this bit is "1", the count source becomes f(XIN)/16. In this case, the detection time is 683 μs at f(XIN)=6 MHz. This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039₁₆). When this bit is "0", the STP instruction is enabled. When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed. Once this bit is set to "1", it cannot be changed to "0" by program. This bit is cleared to "0" after reset.

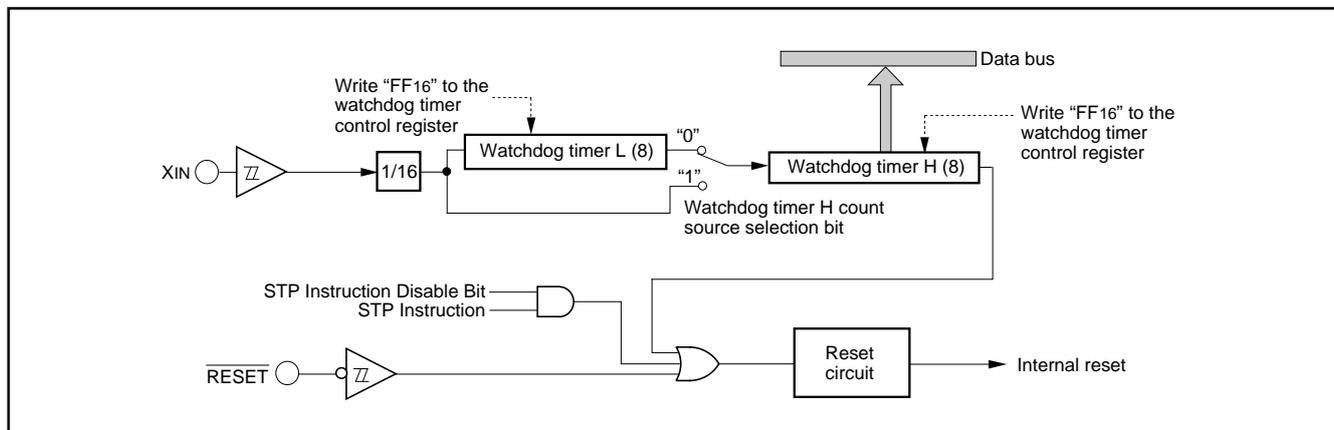


Fig. 37 Block diagram of watchdog timer

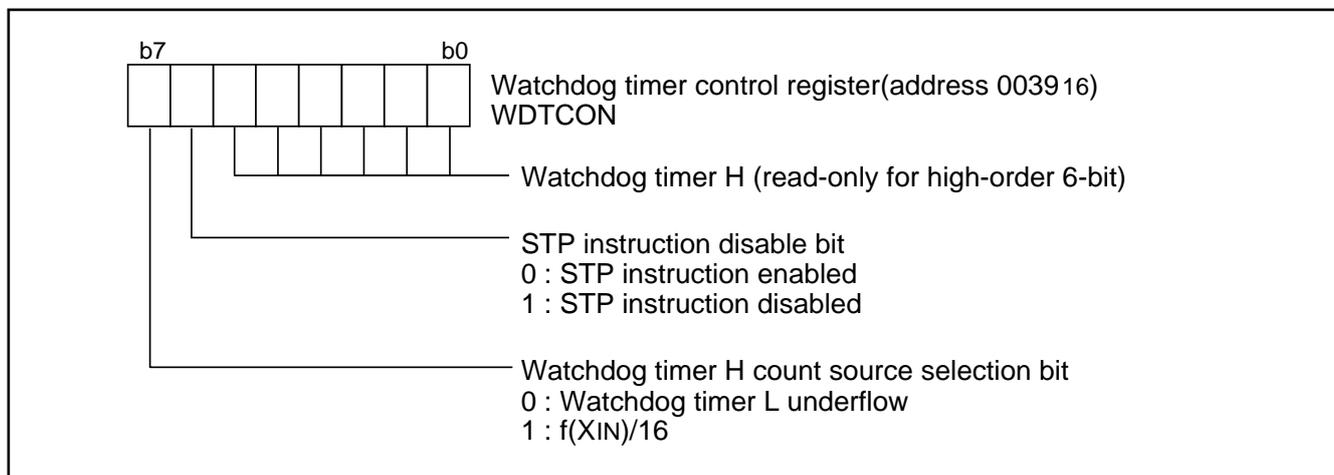


Fig. 38 Structure of watchdog timer control register

Reset Circuit

The microcomputer is put into a reset status by holding the $\overline{\text{RESET}}$ pin at the "L" level for 15 μs or more when the power source voltage is 4.1 to 5.5 V and X_{IN} is in stable oscillation. After that, this reset status is released by returning the $\overline{\text{RESET}}$ pin to the "H" level. The program starts from the address having the contents of address FFFD_{16} as high-order address and the contents of address FFFC_{16} as low-order address. Note that the reset input voltage should be 0.82 V or less when the power source voltage passes 4.1 V.

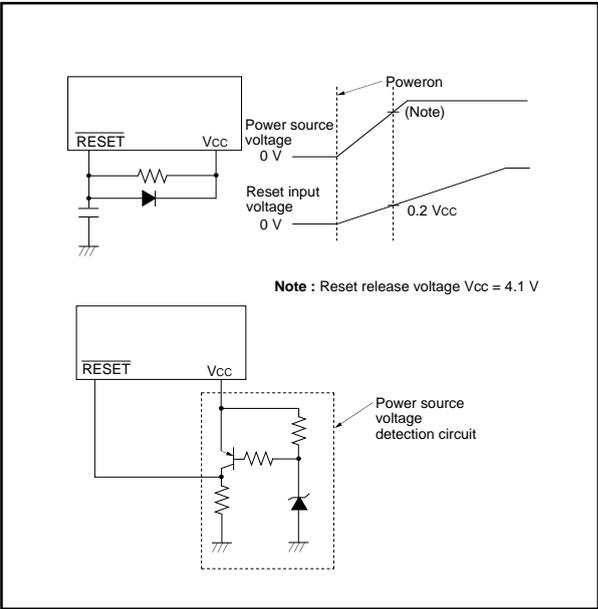


Fig. 39 Example of reset circuit

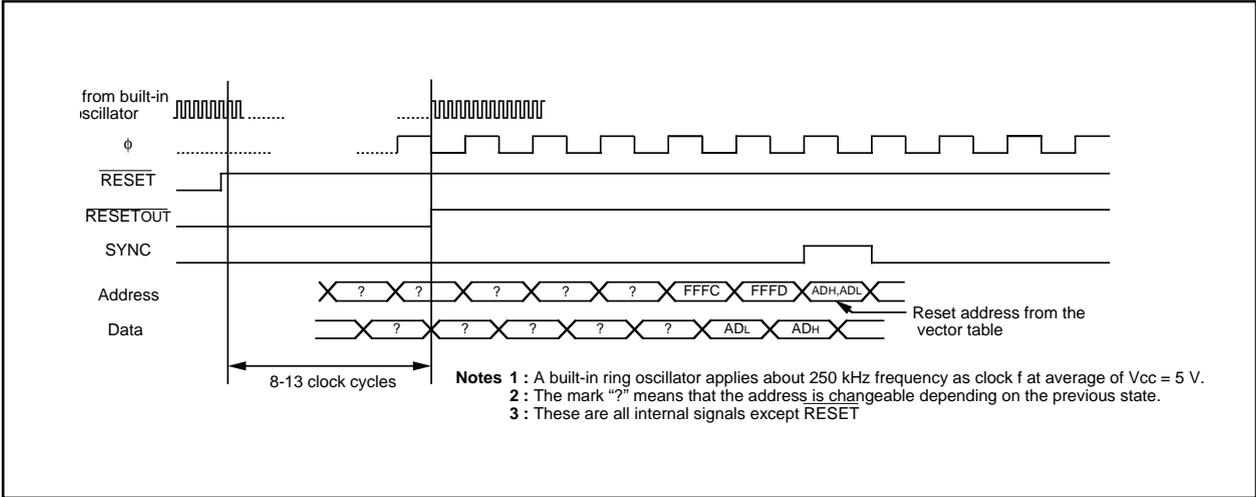


Fig. 40 Timing diagram at reset

	Address	Register contents
(1) Port P0 direction register	0001 ₁₆	00 ₁₆
(2) Port P1 direction register	0003 ₁₆	X X X 0 0 0 0 0
(3) Port P2 direction register	0005 ₁₆	00 ₁₆
(4) Port P3 direction register	0007 ₁₆	00 ₁₆
(5) Pull-up control register	0016 ₁₆	FF ₁₆
(6) Transmit/Receive buffer register	0018 ₁₆	0 0 0 0 0 0 0 0
(7) USB status/UART status register	0019 ₁₆	1 0 0 0 0 0 0 1
(8) Serial I/O1 control register	001A ₁₆	02 ₁₆
(9) UART control register	001B ₁₆	1 1 1 0 0 0 0 0
(10) USB data toggle synchronization register	001D ₁₆	0 1 1 1 1 1 1 1
(11) USB interrupt source discrimination register 1	001E ₁₆	0 1 1 1 1 1 1 1
(12) USB interrupt source discrimination register 2	001F ₁₆	0 1 1 1 0 0 1 1
(13) USB interrupt control register	0020 ₁₆	0 0 0 0 0 1 1 1
(14) USB transmit data byte number set register 0	0021 ₁₆	00 ₁₆
(15) USB transmit data byte number set register 1	0022 ₁₆	00 ₁₆
(16) USBPID control register 0	0023 ₁₆	0 0 0 0 0 1 1 1
(17) USBPID control register 1	0024 ₁₆	0 0 1 1 1 1 1 1
(18) USB address register	0025 ₁₆	1 0 0 0 0 0 0 0
(19) USB sequence bit initialization register	0026 ₁₆	1 1 1 1 1 1 1 1
(20) USB control register	0027 ₁₆	0 0 1 1 1 1 1 1
(21) Prescaler 12	0028 ₁₆	FF ₁₆
(22) Timer 1	0029 ₁₆	01 ₁₆
(23) Timer 2	002A ₁₆	00 ₁₆
(24) Timer X mode register	002B ₁₆	00 ₁₆
(25) Prescaler X	002C ₁₆	FF ₁₆
(26) Timer X	002D ₁₆	FF ₁₆
(27) Timer count source set register	002E ₁₆	00 ₁₆
(28) Serial I/O2 control register	0030 ₁₆	00 ₁₆
(29) A-D control register	0034 ₁₆	10 ₁₆
(30) MISRG	0038 ₁₆	00 ₁₆
(31) Watchdog timer control register	0039 ₁₆	0 0 1 1 1 1 1 1
(32) Interrupt edge selection register	003A ₁₆	00 ₁₆
(33) CPU mode register	003B ₁₆	1 0 0 0 0 0 0 0
(34) Interrupt request register 1	003C ₁₆	00 ₁₆
(35) Interrupt control register 1	003E ₁₆	00 ₁₆
(36) Processor status register	(PS)	X X X X X 1 X X
(37) Program counter	(PC+)	Contents of address FFFD ₁₆
	(PC-)	Contents of address FFFC ₁₆

Note X : Undefined

Fig. 41 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT}.

Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feed-back resistor exists on-chip.

●Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock ϕ stops at an "H" level and the X_{IN} oscillator stops. At this time, timer 1 is set to "0116" and prescaler 12 is set to "FF16" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 12 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used.

$f(X_{IN})/16$ is forcibly connected to the input of prescaler 12.

When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation.

In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the RESET pin while oscillation becomes stable.

• Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received.

Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting clock which is X_{IN} divided by 16, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

Note

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.

• Clock mode

Operation is started by a built-in ring oscillator after releasing reset. A division ratio (1/1,1/2,1/8) is selected by setting bits 7 and 6 of the CPU mode register after releasing it.

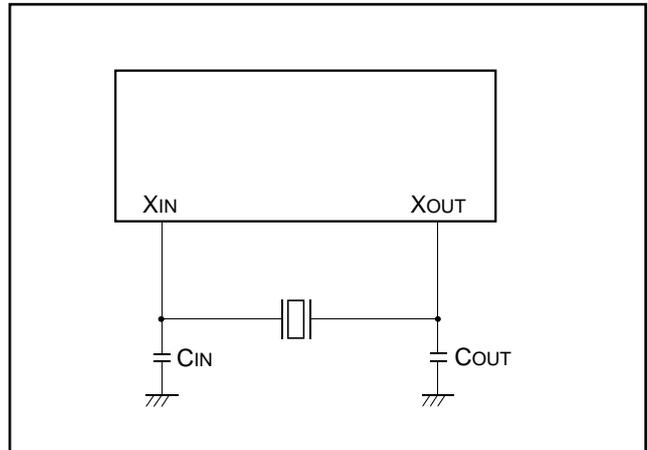


Fig. 42 External circuit of ceramic resonator

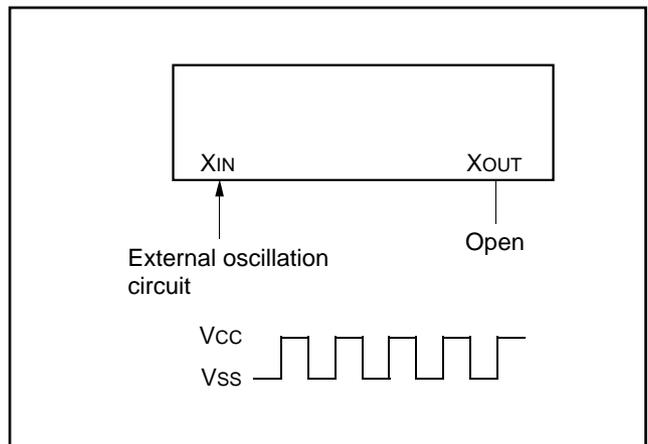


Fig. 43 External clock input circuit

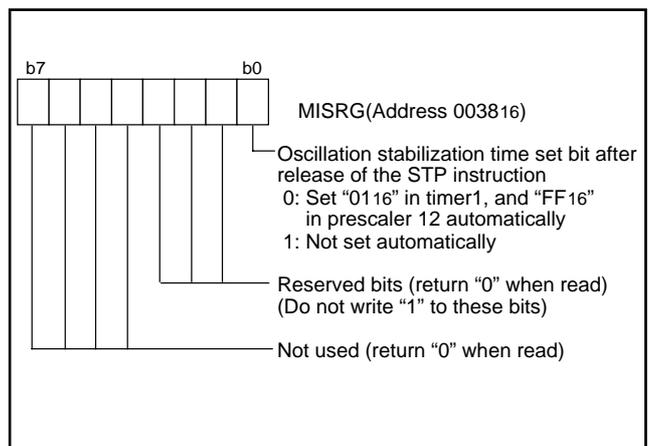


Fig. 44 Structure of MISRG

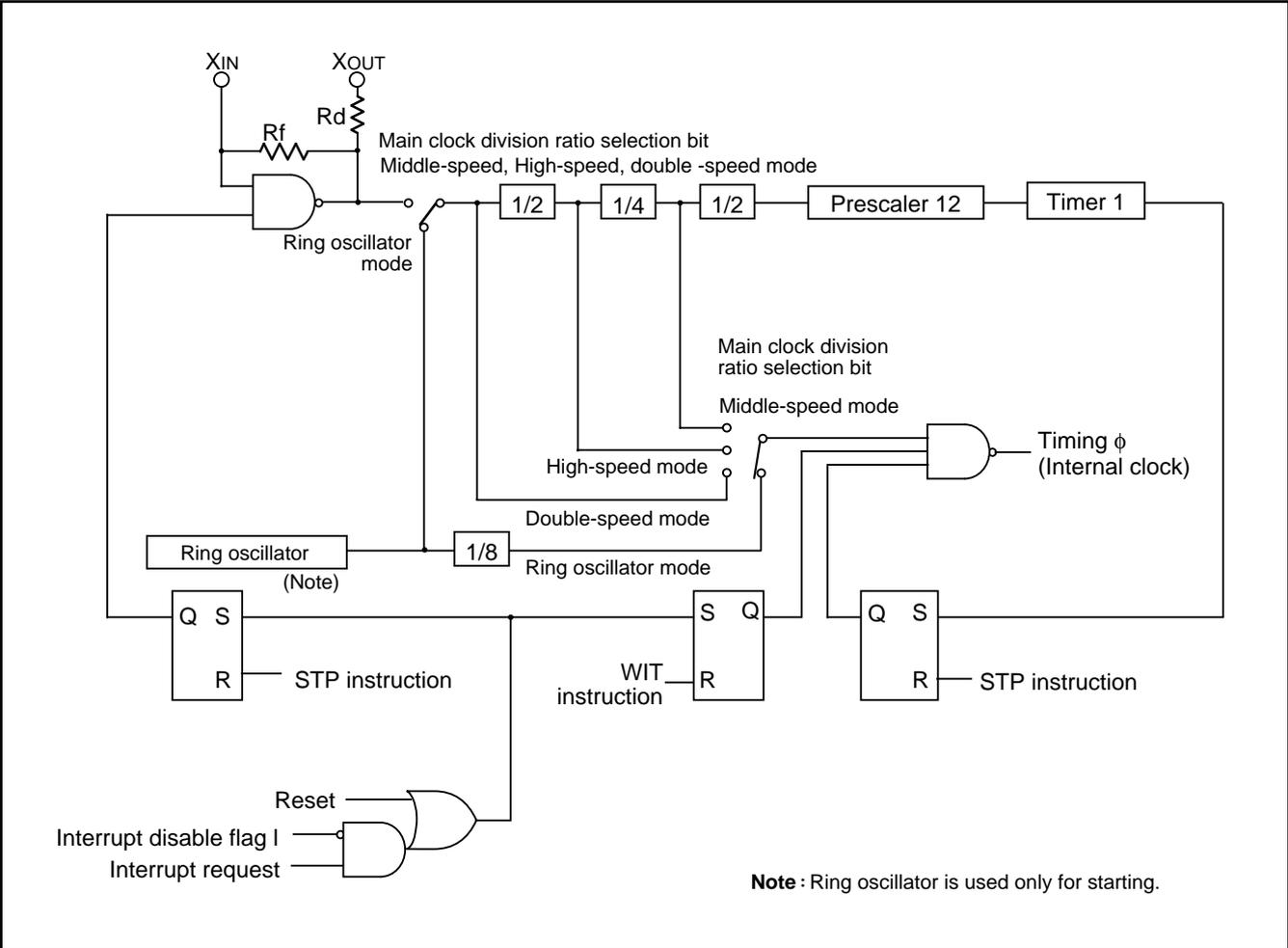


Fig. 45 Block diagram of system clock generating circuit (for ceramic resonator)

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.
- When a count source of timer X is switched, stop a count of timer X.

Ports

- The values of the port direction registers cannot be read.
That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
For setting direction registers, use the LDM instruction, STA instruction, etc.
- Set "1" to each bit 6 of the port P3 direction register and the port P3 register.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(X_{IN})$ is 500kHz or more during A-D conversion.

Do not execute the STP instruction during A-D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.

The frequency of the internal clock ϕ is the same as that of the X_{IN} in double-speed mode, twice the X_{IN} cycle in high-speed mode and 8 times the X_{IN} cycle in middle-speed mode.

NOTES ON USE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF to 0.1 μF is recommended.

Handling of USBVREFOUT Pin

In order to prevent the instability of the USBVREFOUT output due to external noise, connect a capacitor as bypass capacitor between USBVREFOUT pin and GND pin (V_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor, a ceramic or electrolytic capacitor of 0.1 μF is recommended.

One Time PROM Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.

To improve the noise reduction, connect a track between CNVss pin and V_{SS} pin with 1 to 10 k Ω resistance.

The mask ROM version track of CNVss pin has no operational interference even if it is connected via a resistor.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mask Specification Form
- (3) Data to be written to ROM, in EPROM form (three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 6 Special programming adapter

Package	Name of Programming Adapter
36P2R-A	PCA7535FP

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 46 is recommended to verify programming.

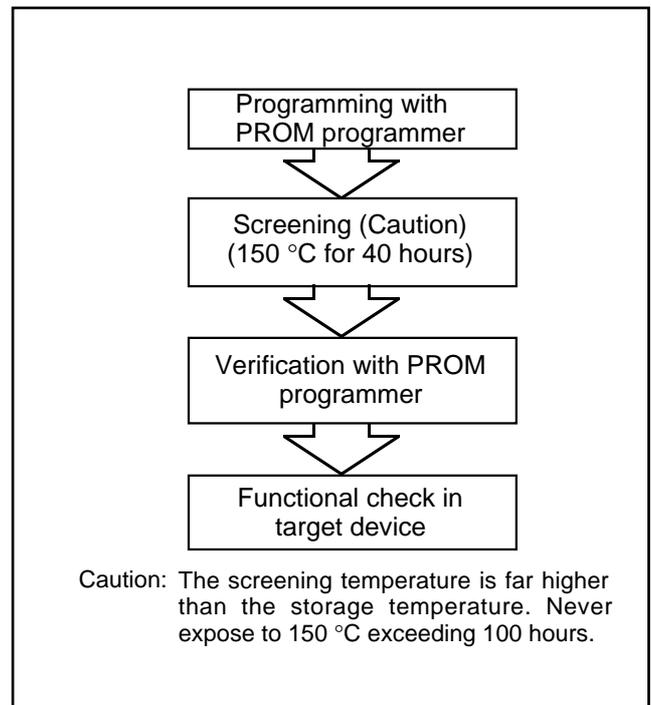


Fig. 46 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 7 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage	All voltages are based on VSS. Output transistors are cut off.	-0.3 to 7.0	V
Vi	Input voltage P00-P07, P10-P14, P20-P27, P30-P35, P37, VREF		-0.3 to VCC + 0.3	V
Vi	Input voltage RESET, XIN		-0.3 to VCC + 0.3	V
Vi	Input voltage CNVSS (Note 1)		-0.3 to 13	V
Vo	Output voltage P00-P07, P10-P14, P20-P27, P30-P35, P37, XOUT, USBVREFOUT		-0.3 to VCC + 0.3	V
Pd	Power dissipation	Ta = 25°C	300 (Note 2)	mW
Topr	Operating temperature		-20 to 85	°C
Tstg	Storage temperature		-40 to 125	°C

Notes 1: It is a rating only for the One Time PROM version. Connect to VSS for the Mask ROM version.

2: 200 mW for 32-pin version.

Recommended Operating Conditions

Table 8 Recommended operating conditions (V_{CC} = 4.1 to 5.5 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Power source voltage	f(XIN) = 6 MHz	4.1	5.0	5.5	V
V _{SS}	Power source voltage			0		V
V _{REF}	Analog reference voltage		2.0		V _{CC}	V
V _{IH}	"H" input voltage	P00–P07, P10–P14, P20–P27, P30–P35, P37	0.8 V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage (TTL input level selected)	P10, P12, P13, P37	2.0		V _{CC}	V
V _{IH}	"H" input voltage	RESET, XIN	0.8 V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	D+, D-	2.0		3.6	V
V _{IL}	"L" input voltage	P00–P07, P10–P14, P20–P27, P30–P35, P37	0		0.3 V _{CC}	V
V _{IL}	"L" input voltage (TTL input level selected)	P10, P12, P13, P37	0		0.8	V
V _{IL}	"L" input voltage	RESET, CNV _{SS}	0		0.2 V _{CC}	V
V _{IL}	"L" input voltage	D+, D-	0		0.8	V
V _{IL}	"L" input voltage	XIN	0		0.16V _{CC}	V
ΣIOH(peak)	"H" total peak output current (Note 1)	P00–P07, P10–P14, P20–P27, P30–P35, P37			-80	mA
ΣIOL(peak)	"L" total peak output current (Note 1)	P00–P07, P10–P14, P20–P27, P37			80	mA
ΣIOL(peak)	"L" total peak output current (Note 1)	P30–P35			60	mA
ΣIOH(avg)	"H" total average output current (Note 1)	P00–P07, P10–P14, P20–P27, P30–P35, P37			-40	mA
ΣIOL(avg)	"L" total average output current (Note 1)	P00–P07, P10–P14, P20–P27, P37			40	mA
ΣIOL(avg)	"L" total average output current (Note 1)	P30–P35			30	mA
IOH(peak)	"H" peak output current (Note 2)	P00–P07, P10–P14, P20–P27, P30–P35, P37			-10	mA
IOL(peak)	"L" peak output current (Note 2)	P00–P07, P10–P14, P20–P27, P37			10	mA
IOL(peak)	"L" peak output current (Note 2)	P30–P35			30	mA
IOH(avg)	"H" average output current (Note 3)	P00–P07, P10–P14, P20–P27, P30–P35, P37			-5	mA
IOL(avg)	"L" average output current (Note 3)	P00–P07, P10–P14, P20–P27, P37			5	mA
IOL(avg)	"L" average output current (Note 3)	P30–P35			15	mA
f(XIN)	Internal clock oscillation frequency (Note 4) at ceramic oscillation or external clock input	V _{CC} = 4.1 to 5.5 V Double-speed mode			6	MHz

Note 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current IOL (avg), IOH (avg) in an average value measured over 100 ms.

4: When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics

Table 9 Electrical characteristics (1) (VCC = 4.1 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P14, P20-P27, P30-P35, P37 (Note 1)	IOH = -5 mA VCC = 4.1 to 5.5 V	VCC-1.5			V
		IOH = -1.0 mA VCC = 4.1 to 5.5 V	VCC-1.0			V
VOH	"H" output voltage D+, D-	VCC = 4.40 to 5.25 V Pull-down through 15kΩ ±5% for D+, D- Pull-up through 1.5kΩ ±5% by USBVREFOUT for D- (Ta = 0 to 70 °C)	2.8		3.6	V
VOL	"L" output voltage P00-P07, P10-P14, P20-P27, P37	IOI = 5 mA VCC = 4.1 to 5.5 V			1.5	V
		IOI = 1.5 mA VCC = 4.1 to 5.5 V			0.3	V
VOL	"L" output voltage D+, D-	VCC = 4.40 to 5.25 V Pull-down through 15kΩ ±5% for D+, D- Pull-up through 1.5kΩ ±5% by USBVREFOUT for D- (Ta = 0 to 70 °C)			0.3	V
VOL	"L" output voltage P30-P35	IOI = 15 mA VCC = 4.1 to 5.5 V			2.0	V
		IOI = 1.5 mA VCC = 4.1 to 5.5 V			0.3	V
VT+–VT–	Hysteresis D+, D–			0.15		V
VT+–VT–	Hysteresis CNTR0, INT0 (Note 2), P00–P07 (Note 3)			0.4		V
VT+–VT–	Hysteresis RXD, SCLK, SDATA (Note 2)			0.5		V
VT+–VT–	Hysteresis RESE \bar{T}			0.5		V
I _{IH}	"H" input current P00–P07, P10–P14, P20–P27, P30–P35, P37	VI = VCC (Pin floating. Pull up transistors "off")			5.0	μA
I _{IH}	"H" input current RESE \bar{T}	VI = VCC			5.0	μA
I _{IH}	"H" input current XIN	VI = VCC		4		μA
I _{IL}	"L" input current P00–P07, P10–P14, P20–P27, P30–P35, P37	VI = VSS (Pin floating. Pull up transistors "off")			-5.0	μA
I _{IL}	"L" input current RESE \bar{T} , CNVSS	VI = VSS			-5.0	μA
I _{IL}	"L" input current XIN	VI = VSS		-4		μA
I _{IL}	"L" input current P00–P07, P30–P35, P37	VI = VSS (Pull up transistors "on")		-0.2	-0.5	mA
VRAM	RAM hold voltage	When clock stopped	2.0		5.5	V

Note 1: P11 is measured when the P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".
2: RXD, SCLK, SDATA, and INT0 have hysteresises only when bits 0 and 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake-up.

Table 10 Electrical characteristics (2) (VCC = 4.1 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
I _{CC}	Power source current	Double-speed mode, f(X _{IN}) = 6 MHz Output transistors "off"		6	10	mA	
		f(X _{IN}) = 6 MHz (in WIT state) Output transistors "off"		1.6	3.2	mA	
		Increment when A-D conversion is executed f(X _{IN}) = 6 MHz, VCC = 5 V		0.8		mA	
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	μA
			Ta = 85 °C			10	μA
VCC = 4.40 to 5.25 V Oscillation stopped in USB mode USB (SUSPEND), (pull-up resistor output not included) (Fig. 47)	Ta = 0 to 70 °C			300	μA		

A-D Converter Characteristics

Table 11 A-D Converter characteristics (1) (VCC = 4.1 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	VCC = 4.1 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	VCC = 4.1 to 5.5 V Ta = 25 °C			±0.9	LSB
VOT	Zero transition voltage	VCC = VREF = 5.12 V	0	5	20	mV
VFST	Full scale transition voltage	VCC = VREF = 5.12 V	5105	5115	5125	mV
tCONV	Conversion time				122	tc(X _{IN})
RLADDER	Ladder resistor			55		kΩ
I _{VREF}	Reference power source input current	VREF = 5.0 V	50	150	200	μA
		VREF = 3.0 V	30	70	120	
I _{I(AD)}	A-D port input current				5.0	μA

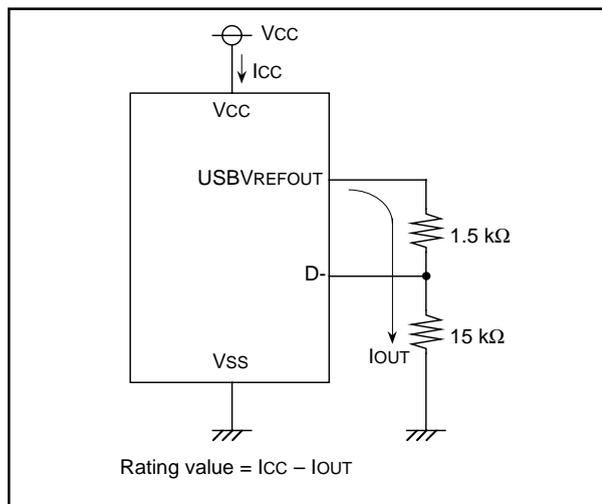


Fig. 47 Power source current measurement circuit in USB mode at oscillation stop

Timing Requirements

Table 12 Timing requirements (Vcc = 4.1 to 5.5 V, Vss = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	15			μs
tc(XIN)	External clock input cycle time	166			ns
tWH(XIN)	External clock input "H" pulse width	70			ns
tWL(XIN)	External clock input "L" pulse width	70			ns
tc(CNTR)	CNTR0 input cycle time	200			ns
tWH(CNTR)	CNTR0, INT0 input "H" pulse width	80			ns
tWL(CNTR)	CNTR0, INT0 input "L" pulse width	80			ns
tc(SCLK)	Serial I/O2 clock input cycle time	1000			ns
tWH(SCLK)	Serial I/O2 clock input "H" pulse width	400			ns
tWL(SCLK)	Serial I/O2 clock input "L" pulse width	400			ns
tsu(SCLK-SDATA)	Serial I/O2 input set up time	200			ns
th(SCLK-SDATA)	Serial I/O2 input hold time	200			ns

Switching Characteristics

Table 13 Switching characteristics (Vcc = 4.1 to 5.5 V, Vss = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWH(SCLK)	Serial I/O2 clock output "H" pulse width	tc(SCLK)/2-30			ns
tWL(SCLK)	Serial I/O2 clock output "L" pulse width	tc(SCLK)/2-30			ns
td(SCLK-SDATA)	Serial I/O2 output delay time			140	ns
tv(SCLK-SDATA)	Serial I/O2 output valid time	0			ns
tr(SCLK)	Serial I/O2 clock output rising time			30	ns
tf(SCLK)	Serial I/O2 clock output falling time			30	ns
tr(CMOS)	CMOS output rising time (Note)		10	30	ns
tf(CMOS)	CMOS output falling time (Note)		10	30	ns
tr(D+), tr(D-)	USB output rising time, CL = 350 pF, Ta = 0 to 70 °C	100	200	300	ns
tf(D+), tf(D-)	USB output falling time, CL = 350 pF, Ta = 0 to 70 °C	100	200	300	ns

Notes: XOUT pin is excluded.

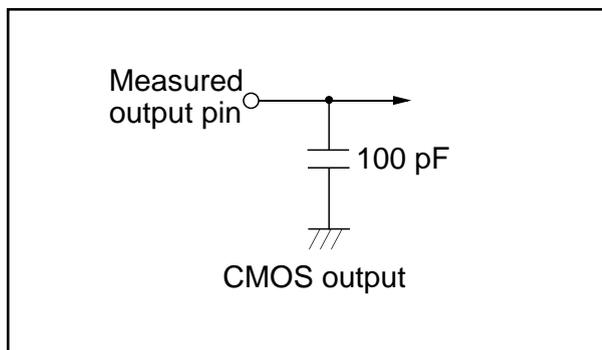


Fig. 48 Output switching characteristics measurement circuit

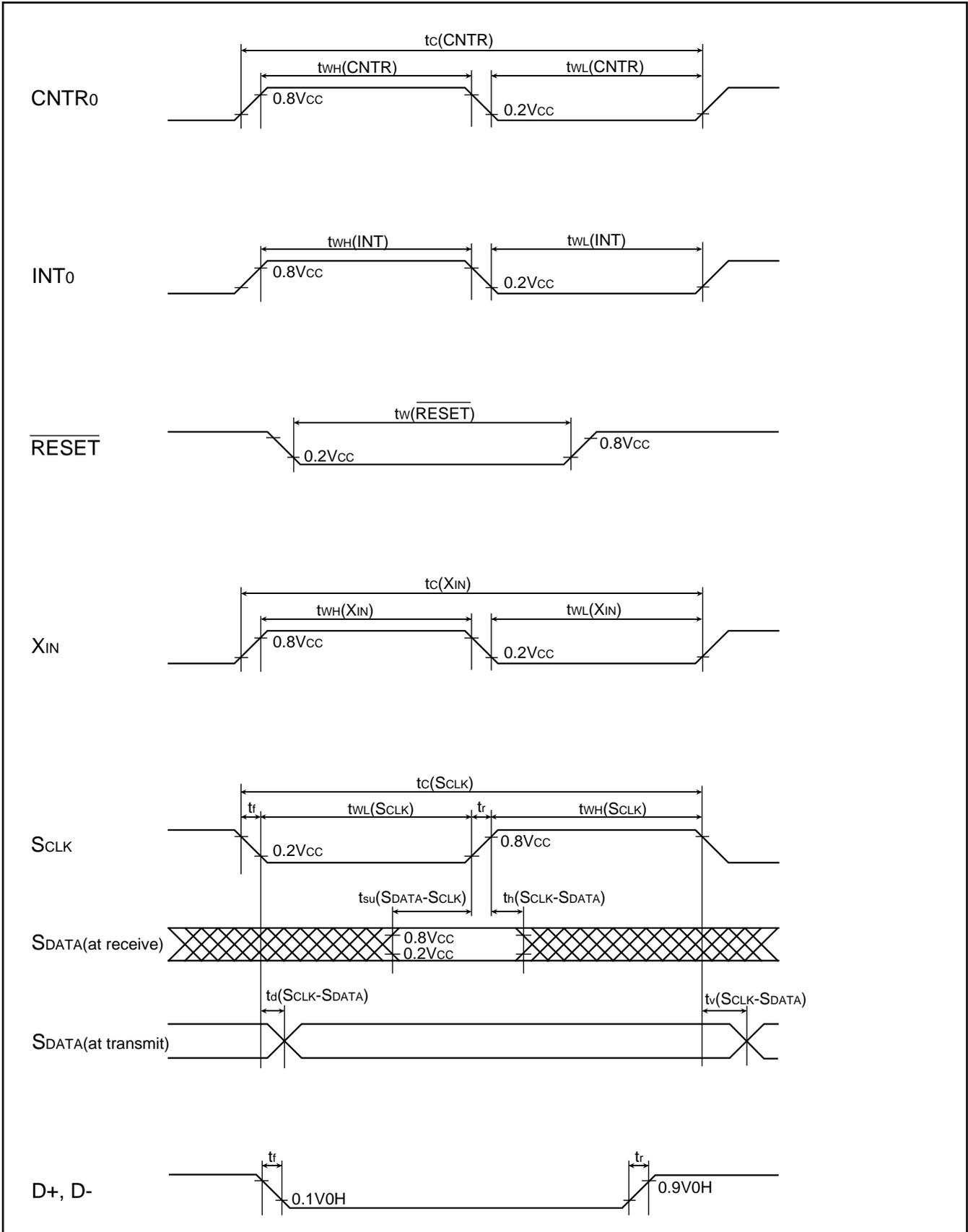


Fig. 49 Timing chart

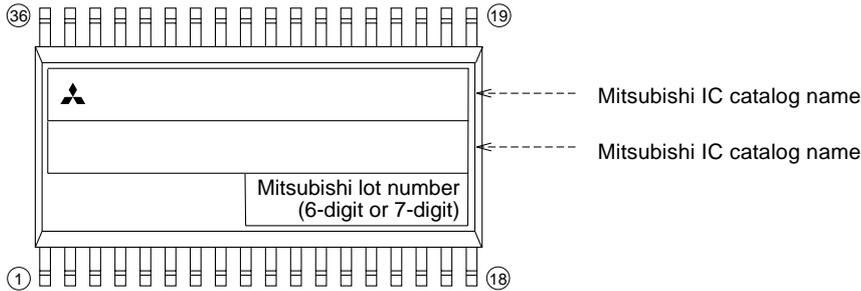
MARK SPECIFICATION FORM

36P2R-A (36-PIN SHRINK SOP) MARK SPECIFICATION FORM

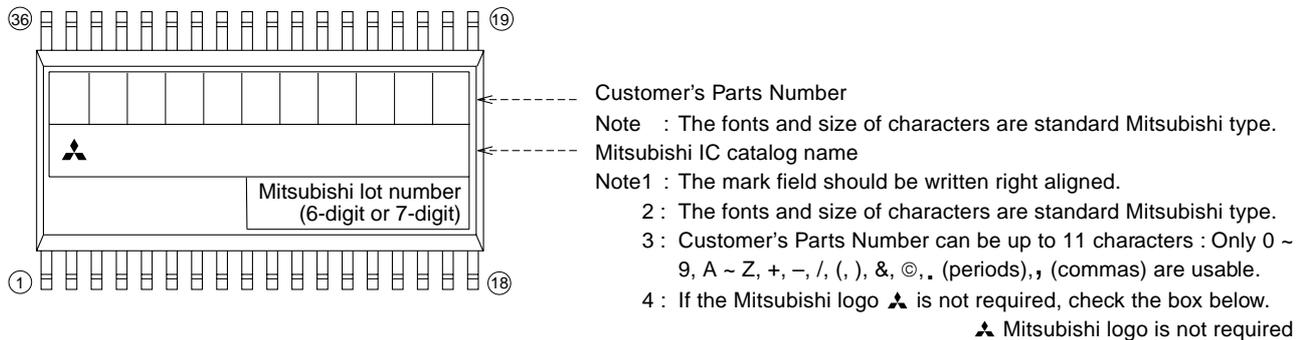
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

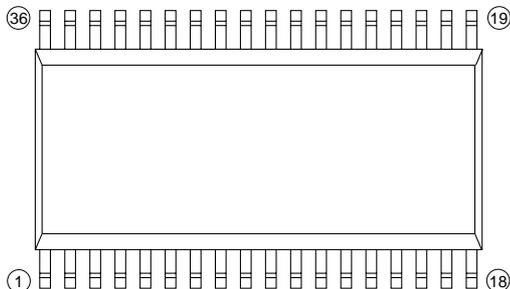


B. Customer's Parts Number + Mitsubishi catalog name



Mitsubishi logo is not required

C. Special Mark Required



Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.

Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.

Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

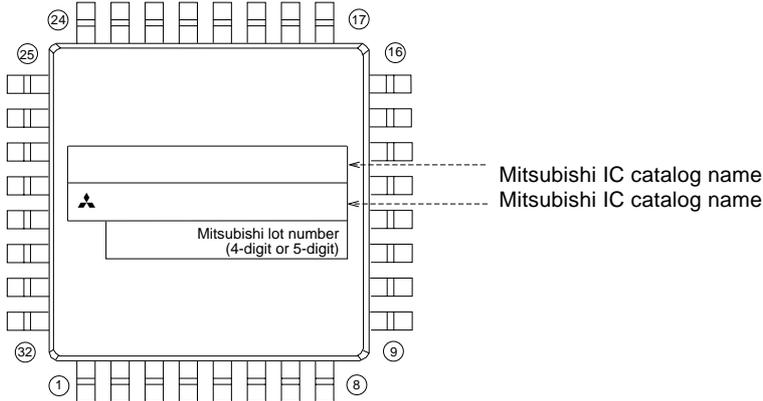
3 : The standard Mitsubishi font is used for all characters except for a logo.

32P6B-A (32-PIN LQFP) MARK SPECIFICATION FORM

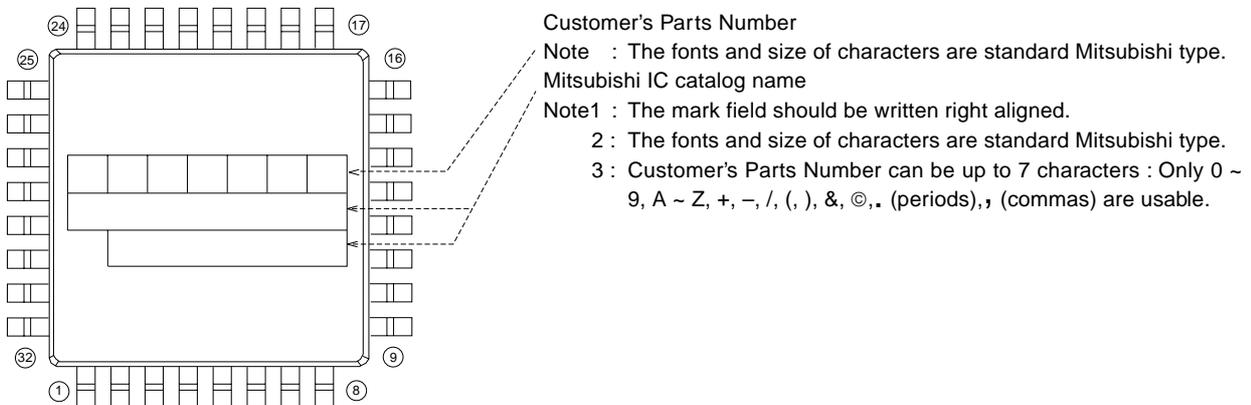
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi catalog name

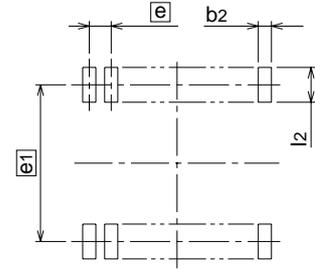
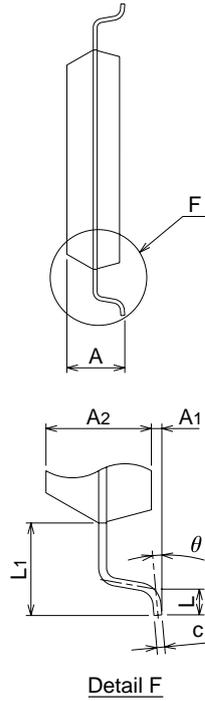
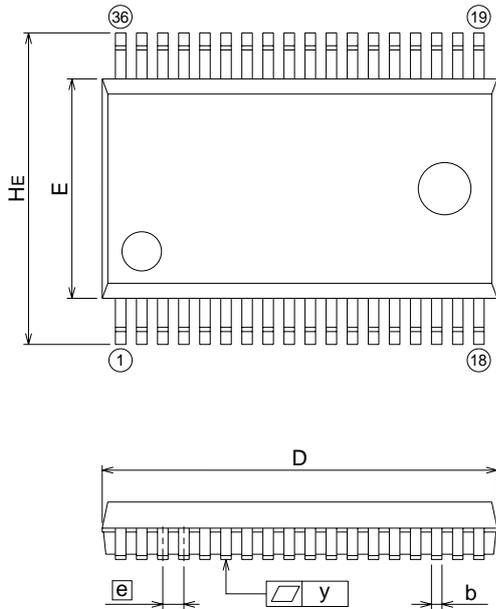


PACKAGE OUTLINE

36P2R-A

Plastic 36pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	-	0.53	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	2.4
A1	0.05	-	-
A2	-	2.0	-
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	-	0.8	-
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	-	1.765	-
y	-	-	0.15
theta	0°	-	10°
b2	-	0.5	-
e1	-	11.43	-
l2	1.27	-	-

REVISION DESCRIPTION LIST

7532 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	970822
1.1	<p>All pages; "PRELIMINARY Notice: This is not a final specification. Some parametric limits are subject to change." eliminated.</p> <p>Page 4; Fig. 3; "Under development" eliminated.</p> <p>Page 5; Central Processing Unit (CPU); The name of manual, 740 Family Software Manual, is revised. Fig. 4; The bit name is revised. Bits 6 and 7 explanations of CPU mode register are revised. Fig. 5; Explanation is added.</p> <p>Page 6; Special page; Some words are corrected.</p> <p>Page 7 Fig. 7 ; Some register names are revised.</p> <p>Page 8 [Direction register] PiD; The sentence is revised. →Pins set to output are floating. Fig. 9; The Figure title is revised.</p> <p>Page 12; Interrupts; Explanation is revised. The period is added. Interrupt operation; The order of operation is revised. Table 4: Remarks is revised. Some words are corrected.</p> <p>Page 17; Serial I/O; Some words and the pin name position are revised.</p> <p>Page 18; The register name is revised. → [UART status register] UARTSTS Fig. 20; Some words are corrected.</p> <p>Page 21 to Page 24; Some words are corrected.</p> <p>Page 26; Serial I/O2; Some words are corrected. Fig. 29; Explanation is revised.</p> <p>Page 28; [A-D conversion register]AD; The sentence is revised.→Do not read out during an A-D conversion.</p> <p>Page 29; Fig. 35; The sentence is revised.→read-only for high-order 6-bit</p> <p>Page 30; Fig. 37; The period is added.</p> <p>Page 32; • Wait mode; The sentence is revised. →When the STP status is released, prescaler 12 and timer 1 will start counting clock which is XIN divided by 16,.....</p> <p>Page 34; One Time PROM Version; The sentences are revised. →To improve the noise reduction, connect a track between CNMss pin and Vss pin... →The mask ROM version track of CNVSS pin has no operational interference...</p> <p>Page 36; Absolute Maximum Ratings; Parameter of input voltage is revised. Note is revised.</p> <p>Page 37; Recommended operating conditions; Limits of "H" input voltage is revised.</p>	981218

REVISION DESCRIPTION LIST

7532 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
1.1	<p>Page 38; Electrical characteristics; Test conditions of V_{OH} and V_{OL} are revised. Some of V_{OL} are eliminated partly. Hysteresis is added.</p> <p>Page 39; Electrical characteristics; Test condition is added. A-D Converter Characteristics; Some of V_{OT} and V_{FST} are eliminated partly.</p> <p>Page 40; Switching characteristics; Title and Table title are revised. Limits of t_c(X_{IN}), t_{WH}(X_{IN}), t_{WL}(X_{IN}). Figure is added.</p>	981218
2.0	Most of the contents (Functional Description, Electrical characteristics, and so on) are updated.	990723
2.1	<p>Page 2; Fig. 2 Pin configuration of M37532M4-XXXGP; Pin functions revised. Pin 26: P10/RxD/D- (correct) Pin 27: P11/TxD/D+ (correct)</p>	991015
2.2	<p>Updated as follows:</p> <ul style="list-style-type: none"> •Page 1; Power dissipation to 30 mW •Page 9; Fig. 9; Start address of Interrupt vector area to FFEC16 •Page 42, Table 11; Parameter to Linearity error from former Absolute accuracy 	991110
2.3	<p>Page 30; Fig.33 Note revised</p> <p>Page 33; Description revised; $\overline{\text{RESET}}$ "L" pulse width 2 μs → 15 μs</p> <p>Page 42, Table 11 Linearity error; "excluding quantization error" deleted</p> <p>Page 43; Table 12 t_w($\overline{\text{RESET}}$) revised; 2 → 15</p>	000614
2.4	Page 33: Character fonts errors revised	000905