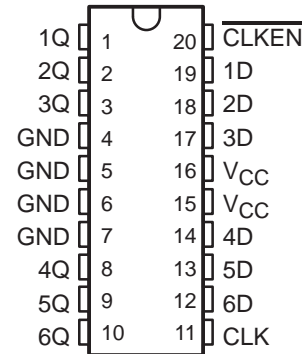


# 74ACT11378 HEX D-TYPE FLIP-FLOP WITH CLOCK ENABLE

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- Inputs Are TTL-Voltage Compatible
- Contains Six D-Type Flip-Flops
- Clock Enable Latched to Avoid False Clocking
- Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, and Standard Plastic 300-mil DIPs

DW OR N PACKAGE  
(TOP VIEW)



## description

These circuits are positive-edge-triggered D-type flip-flops with a clock-enable input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the clock-enable input (CLKEN) is low.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock inputs are at either the high or low level, the data (D) input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the clock-enable (CLKEN) input.

The 74ACT11378 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT Q
CLKEN	CLK	D	
H	X	X	$Q_O$
L	↑	H	H
L	↑	L	L
X	L	X	$Q_O$

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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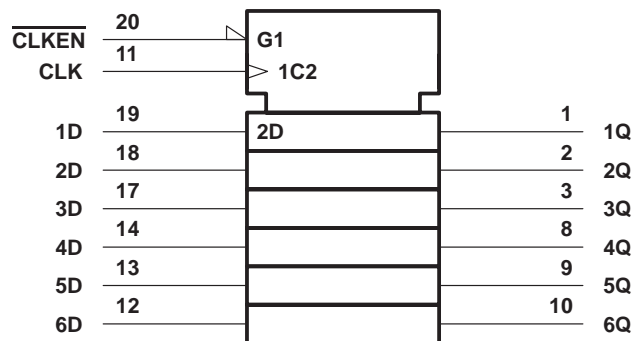
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# 74ACT11378

## HEX D-TYPE FLIP-FLOP WITH CLOCK ENABLE

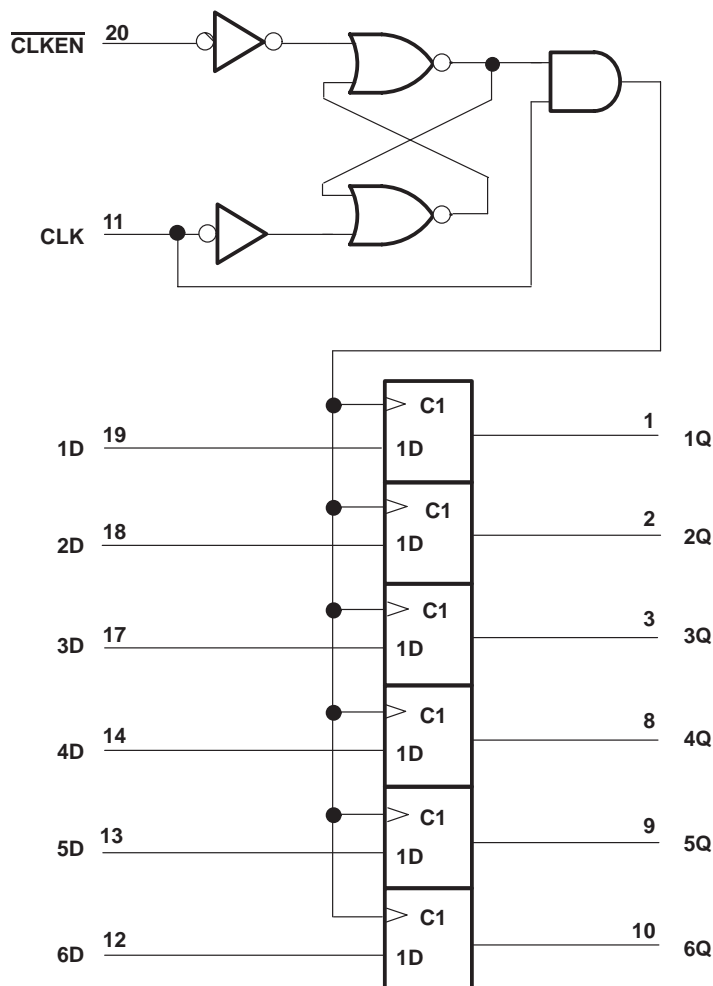
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND pins	±150 mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**recommended operating conditions (see Note 2)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$V_I$ Input voltage	0	$V_{CC}$		V
$V_O$ Output voltage	0	$V_{CC}$		V
$I_{OH}$ High-level output current			–24	mA
$I_{OL}$ Low-level output current			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	ns/V
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	$I_{OH} = -24\ \text{mA}$	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	$I_{OH} = -75\ \text{mA}^\ddagger$	5.5 V				3.85		
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	$I_{OL} = 24\ \text{mA}$	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	$I_{OL} = 75\ \text{mA}^\ddagger$	5.5 V					1.65	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	μA
$\Delta I_{CC}^\S$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			0.9		1	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4.5				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

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**HEX D-TYPE FLIP-FLOP**  
**WITH CLOCK ENABLE**

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
$f_{\text{clock}}$	Clock frequency		0	100	0	100	MHz
$t_w$	Pulse duration	CLK high or low	5		5		ns
$t_{\text{su}}$	Setup time, before CLK $\uparrow$	Data	5		5		ns
		CLKEN high or low	4.5		4.5		
$t_h$	Hold time, after CLK $\uparrow$	Data	0.5		0.5		ns
		CLKEN high or low	1		1		

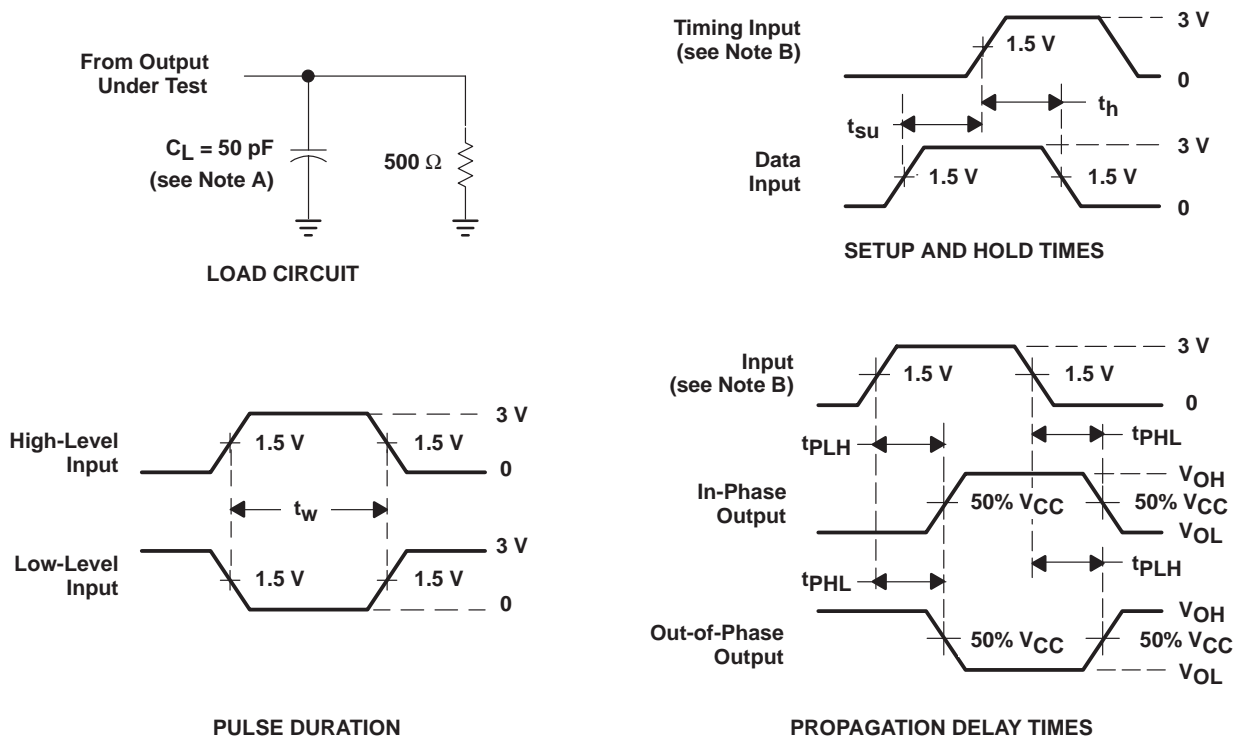
**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			100	130		100		MHz
$t_{\text{PLH}}$	CLK	Any Q	2.8	5.9	6.8	2.8	9	ns
$t_{\text{PHL}}$			3.7	7.3	9.2	3.7	10.7	

**operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 1\text{ MHz}$	31	pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . For testing  $f_{max}$  and pulse duration:  $t_r = 1 \text{ to } 3 \text{ ns}$ ,  $t_f = 1 \text{ to } 3 \text{ ns}$ .

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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