# 74ACT11873
DUAL 4-BIT D-TYPE LATCH
WITH 3–STATE OUTPUTS

SCAS096 – FEBRUARY 1990 – REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Flow-Through Architecture to Optimize PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **EPIC ™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)

1C	1	28	1$\overline{OC}$
1Q1	2	27	1$\overline{CLR}$
1Q2	3	26	1D1
1Q3	4	25	1D2
1Q4	5	24	1D3
GND	6	23	1D4
GND	7	22	V_{CC}
GND	8	21	V_{CC}
GND	9	20	2D1
2Q1	10	19	2D2
2Q2	11	18	2D3
2Q3	12	17	2D4
2Q4	13	16	2$\overline{CLR}$
2C	14	15	2$\overline{OC}$
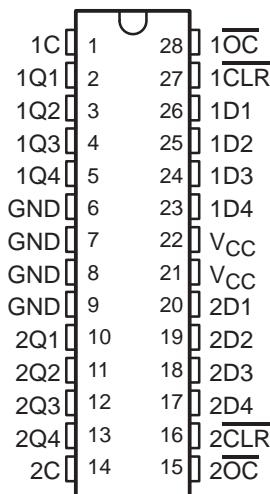
description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latch is transparent D-type. When the latch enable input (1C or 2C) is high, the (Q) outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When $\overline{CLR}$ goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when $\overline{OC}$ (output control) is at a high logic level.

The 74ACT11873 is characterized for operation from − 40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OC}$	$\overline{CLR}$	C	D	Q
L	L	X	X	L
L	H	H	H	H
L	H	H	L	L
L	H	L	X	Q_O
H	X	X	X	Z

EPIC is a trademark of Texas Instruments Incorporated.

Copyright © 1993, Texas Instruments Incorporated

TEXAS INSTRUMENTS

74ACT11873
DUAL 4-BIT D-TYPE LATCH
WITH 3–STATE OUTPUTS
SCAS096 – FEBRUARY 1990 – REVISED APRIL 1993

logic symbol†

logic diagram (positive logic)
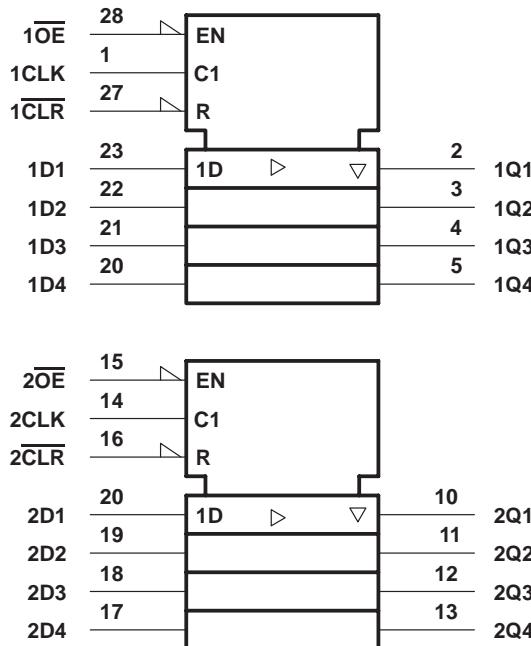
each quad latch

† This symbol is in accordance with ANSI/IEEE Std 91-1984
and IEC Publication 617-12.
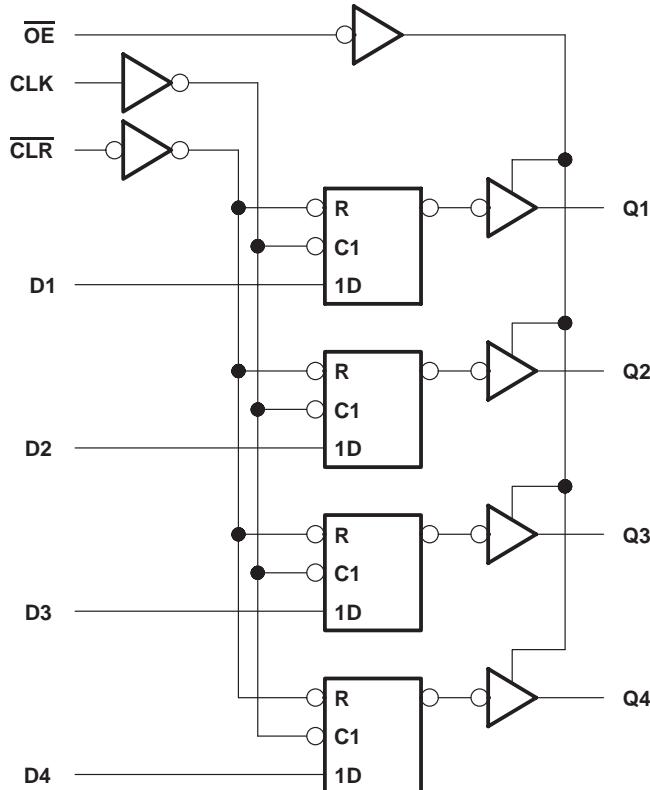
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ± 50 mA
Continuous current through V_{CC} or GND . . . . ± 200 mA
Storage temperature range . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\ \mu A$	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	$I_{OH} = -24\ mA$	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	$I_{OH} = -75\ mA^\dagger$	5.5 V				3.85		
V_{OL}	$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	$I_{OL} = 24\ mA$	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	$I_{OL} = 75\ mA^\dagger$	5.5 V					1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5				pF
C_O	$V_O = V_{CC}$ or GND	5 V		13.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|			$T_A = 25°C$		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	$\overline{CLR}$ low	5		5		ns
		C high	5		5		
t_{su}	Setup time before C ↓	Data high	6		6		ns
		Data low	3		3		
t_h	Hold time after C ↓	Data high	0		0		ns
		Data low	0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	4.4	7.2	8.8	4.4	10	ns
t_{PHL}			3	6.6	9.1	3	10.2	
t_{PLH}	C	Q	4.7	8.1	10	4.7	11.3	ns
t_{PHL}			5.2	8.9	10.9	5.2	12.3	
t_{PHL}	$\overline{CLR}$	Q	2.9	6.5	9	2.9	10	ns
t_{PZH}	$\overline{OC}$	Q	1.9	4.9	7.1	1.9	8	ns
t_{PZL}			2.7	6.4	9.1	2.7	10.3	
t_{PHZ}	$\overline{OC}$	Q	5.7	8	9.5	5.7	10.2	ns
t_{PLZ}			5.2	7.8	9.1	5.2	9.8	

operating characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per latch	Outputs enabled	$C_L = 50$ pF, f = 1 MHz	40	pF
	Outputs disabled		7	

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND
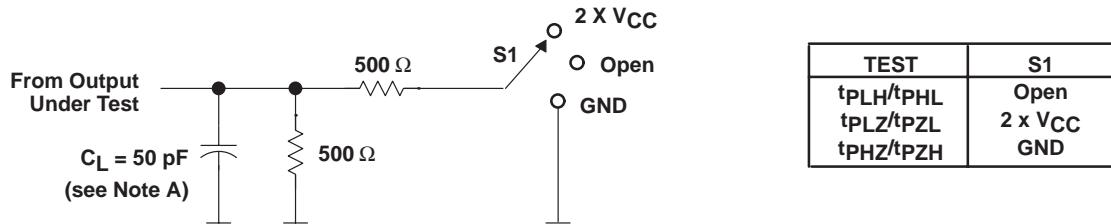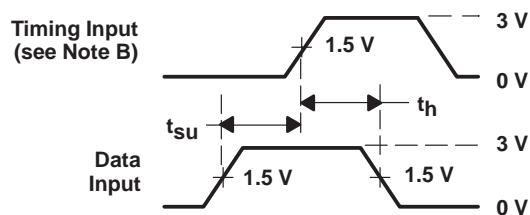
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
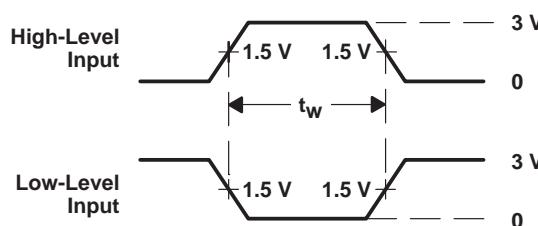
VOLTAGE WAVEFORMS
PULSE DURATION
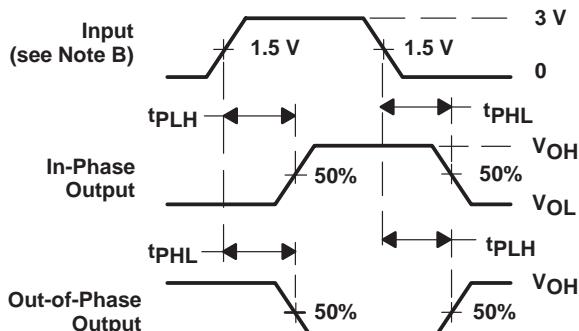
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
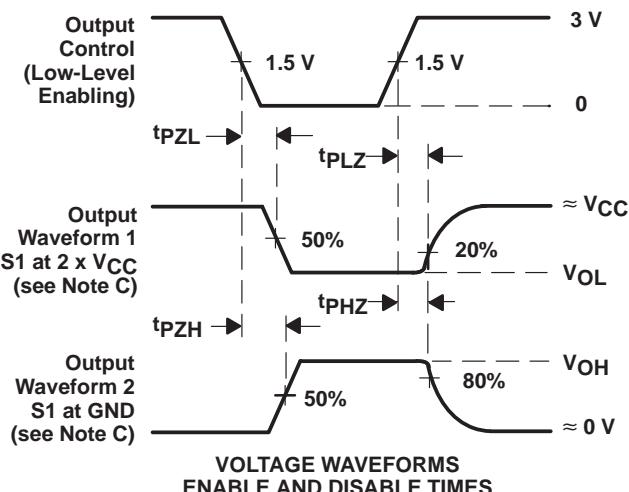
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
   B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.