

August 1993 Revised March 1999

### 74VHC125

# **Quad Buffer with 3-STATE Outputs**

#### **General Description**

The VHC125 contains four independent non-inverting buffers with 3-STATE outputs. It is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology and achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This cir-

cuit prevents device destruction due to mismatched supply and input voltages.

#### **Features**

- High Speed:  $t_{PD} = 3.8$  ns (typ) at  $V_{CC} = 5V$
- Lower power dissipation:  $I_{CC} = 4 \mu A \text{ (max)}$  at  $T_A = 25 ^{\circ} C$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Power down protection is provided on all inputs
- Low noise:  $V_{OLP} = 0.8V$  (max)

#### **Ordering Code:**

Order Number	Package Number	Package Description					
74VHC125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow					
74VHC125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide					
74VHC125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide					
74VHC125N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide					

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

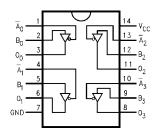
#### **Logic Symbol**

# | IEEE/IEC | $B_0$ | $A_0$ |

#### **Pin Descriptions**

Pin Names	Description					
$\overline{A}_n$ , $B_n$	Inputs					
O <sub>n</sub>	Outputs					

# **Connection Diagram**



#### **Function Table**

Inp	Output			
Ā <sub>n</sub>	$\overline{A}_n$ $B_n$			
L	L	L		
L	Н	Н		
Н	X	Z		

H = HIGH Voltage Level

L = LOW Voltage Level Z = HIGH Impedance

X = Immateria

## Absolute Maximum Ratings(Note 1)

# Recommended Operating Conditions (Note 2)

DC V $_{\rm CC}$ /GND Current (I $_{\rm CC}$ )  $\pm 50$  mA Storage Temperature (T $_{\rm STG}$ )  $-65^{\circ}{\rm C}$  to  $+150^{\circ}{\rm C}$ 

Lead Temperature (T<sub>L</sub>)

(Soldering, 10 seconds)

Input Rise and Fall Time  $(t_{\rm r},\,t_{\rm f})$ 

$$\begin{split} \text{V}_{\text{CC}} = 3.3 \text{V} \pm 0.3 \text{V} & 0 \sim 100 \text{ ns/V} \\ \text{V}_{\text{CC}} = 5.0 \text{V} \pm 0.5 \text{V} & 0 \sim 20 \text{ ns/V} \end{split}$$

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

#### **DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 25°C			$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	
		(V)	Min	Тур	Max	Min	Max	Units	Conditions	
V <sub>IH</sub>	HIGH Level Input	2.0	1.50			1.50		V		
	Voltage	3.0 - 5.5	0.7 V <sub>CC</sub>			0.7 V <sub>CC</sub>		v		
V <sub>IL</sub>	LOW Level Input	2.0			0.50		0.50	V		
	Voltage	3.0 - 5.5			$0.3\mathrm{V}_{\mathrm{CC}}$		$0.3  V_{\rm CC}$	V		
V <sub>OH</sub>	HIGH Level Output	2.0	1.9	2.0		1.9			$V_{IN} = V_{IH} I_{OH} = -50 \mu A$	A
	Voltage	3.0	2.9	3.0		2.9		V	or V <sub>IL</sub>	
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V	$I_{OH} = -4 \text{ mA}$	<u> </u>
		4.5	3.94			3.80		v	$I_{OH} = -8 \text{ mA}$	١.
V <sub>OL</sub>	LOW Level Output	2.0		0.0	0.1		0.1		$V_{IN} = V_{IH}$ $I_{OL} = 50 \mu A$	
	Voltage	3.0		0.0	0.1		0.1	V	or V <sub>IL</sub>	
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V	$I_{OL} = 4 \text{ mA}$	
		4.5			0.36		0.44	v	$I_{OL} = 8 \text{ mA}$	
loz	3-STATE Output	5.5			±0.25		±2.5	μΑ	$V_{IN} = V_{IH}$ or $V_{IL}$	
	Off-State Current								$V_{OUT} = V_{CC}$ or GND	
I <sub>IN</sub>	Input Leakage	0 – 5.5			±0.1		±1.0	μΑ	V <sub>IN</sub> = 5.5V or GND	
	Current									
I <sub>CC</sub>	Quiescent Supply	5.5			4.0		40.0	μΑ	$V_{IN} = V_{CC}$ or GND	
	Current									

260°C

#### **Noise Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> =	: 25°C	Units	Conditions	
			Тур	Limits		00.141.101.10	
V <sub>OLP</sub>	Quiet Output Maximum	5.0	0.5	0.8	V	C <sub>L</sub> = 50 pF	
(Note 3)	Dynamic V <sub>OL</sub>						
V <sub>OLV</sub>	Quiet Output Minimum	5.0	-0.5	-0.8	V	C <sub>L</sub> = 50 pF	
(Note 3)	Dynamic V <sub>OL</sub>						
V <sub>IHD</sub>	Minimum HIGH Level	5.0		3.5	V	C <sub>L</sub> = 50 pF	
(Note 3)	Dynamic Input Voltage						
V <sub>ILD</sub>	Maximum HIGH Level	5.0		1.5	V	C <sub>L</sub> = 50 pF	
(Note 3)	Dynamic Input Voltage						

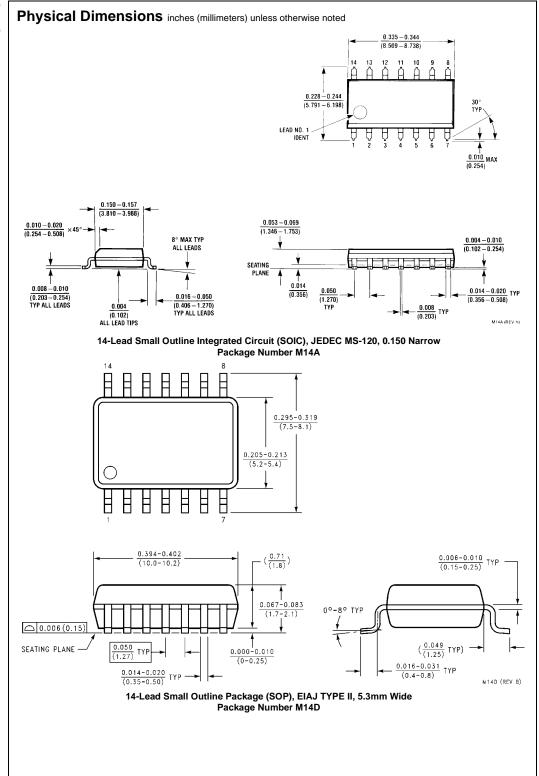
Note 3: Parameter guaranteed by design.

# **AC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	$T_A = 25^{\circ}C$			T <sub>A</sub> = -40°	C to +85°C	Units	Conditions	
		(V)	Min	Тур	Max	Min	Max	Units	J	
t <sub>PLH</sub>	Propagation Delay	$3.3 \pm 0.3$		5.6	8.0	1.0	9.5	ns		$C_{L} = 15 \text{ pF}$
t <sub>PHL</sub>	Time			8.1	11.5	1.0	13.0	115		$C_L = 50 pF$
		$5.0 \pm 0.5$		3.8	5.5	1.0	6.5	ns		C <sub>L</sub> = 15 pF
				5.3	7.5	1.0	8.5	115		$C_L = 50 pF$
t <sub>PZL</sub>	3-STATE Output	$3.3\pm0.3$		5.4	8.0	1.0	9.5	ns	$R_L = 1 k\Omega$	$C_{L} = 15 \text{ pF}$
$t_{PZH}$	Enable Time			7.9	11.5	1.0	13.0	ns		$C_L = 50 \text{ pF}$
		$5.0 \pm 0.5$		3.6	5.1	1.0	6.0	ns		$C_{L} = 15 \text{ pF}$
				5.1	7.1	1.0	8.0	115		$C_L = 50 pF$
t <sub>PLZ</sub>	3-STATE Output	$3.3\pm0.3$		9.5	13.2	1.0	15.0	ns	$R_L = 1 k\Omega$	$C_L = 50 pF$
$t_{PHZ}$	Disable Time	$5.0 \pm 0.5$		6.1	8.8	1.0	10.0	115		$C_{L} = 50 \text{ pF}$
t <sub>OSLH</sub>	Output to Output Skew	$3.3\pm0.3$			1.5		1.5	ns	(Note 4)	$C_L = 50 pF$
toshl		$5.0 \pm 0.5$			1.0		1.0	115		$C_L = 50 pF$
C <sub>IN</sub>	Input Capacitance			4	10		10	pF	V <sub>CC</sub> = Open	
C <sub>OUT</sub>	Output Capacitance			6				pF	V <sub>CC</sub> = 5.0V	
C <sub>PD</sub>	Power Dissipation			14				pF	(Note 5)	
	Capacitance									

 $\textbf{Note 4:} \ \ \text{Parameter guaranteed by design.} \ \ t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|; \ t_{OSHL} = |t_{PHLmax} - t_{PHLmin}|.$ 

Note 5:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC}$  (OPR.) =  $C_{PD}$  \*  $V_{CC}$  \*  $f_{IN}$  +  $I_{CC}$ /4 (per bit).



# Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 5.0±0.1 0.43 TYP 7.72 4.16 6.4 4.4±0.1 -B-3.2 0.65 LAND PATTERN RECOMMENDATION PIN #1 IDENT. SEE DETAIL A ALL LEAD TIPS 1.2 MAX -0.90<sup>+0.15</sup> 0.09-0.20 -C-0.10±0.05 0.65 , -12.00°T□P & B□TT□M R0.16 R0.31 GAGE PLANE NOTES 0.25 A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ABJREF NOTE 6, DATED 7/93 0°-8° B. DIMENSIONS ARE IN MILLIMETERS C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS SEATING PLANE -1.00 DETAIL A 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.630 - 8.128}{(7.620 - 8.128)}$ 0.060 (1.524) 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 $0.075 \pm 0.015$ $\overline{(3.175 - 3.810)}$ $(1.905 \pm 0.381)$ (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$ 0.325 <sup>+0.040</sup> -0.015 8.255 + 1.016

#### 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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N14A (REV F)