9Mb Pipelined QDR™ SRAM Burst of 2

Advance Information

IDT71T62805

Features

- **9Mb Density (512Kx18)**
- **Separate Independent Read and Write Data Ports**
  - *Supports concurrent transactions*
- **333MHz Data Rate for High Bandwidth Applications**
- **Fast Clock-to ValidDR access times**
  - *2.5ns for 166MHz version*
- **Double Data Rate (DDR) interfaces on both Read and Write ports (data transfered at 333MHz)**
- **Two Input clocks (K and $\overline{K}$), using rising edges only, for precise timing**
- **Two output register clocks (C and $\overline{C}$) compensate for clock skew and flight time mismatches**
  - *Clock and data delivered together to receiving device*
- **Single multiplexed address input bus latches address inputs for both READ and WRITE ports**
- **Data forwarding feature provides most current data**
- **Separate Port Selects for depth expansion**
- **Internal synchronous self-timed three-state control**
- **Synchronous internally self-timed writes**
- **2.5V core power supply with HSTL Inputs and Outputs**
- **165-ball,1.0mm pitch 13mm x 15mm fBGA Package**
- **Variable drive HSTL output buffers**
- **JTAG Interface**
- **Variable Impedance HSTL.**

Description

The IDT71T62805 is a 2.5V Synchronous pipelined SRAM equipped with QDR™ architecture. QDR architecture consists of two separate ports to access the memory array. The Read port has dedicated Data Outputs to support Read operations, and the Write Port has dedicated Data inputs to support Write operations. Access to each port is accomplished through a common address bus. The Read address is latched on the rising edge of the K clock and the Write address is latched on the rising edge of $\overline{K}$ clock. QDR architecture has separate data inputs and data outputs to completely eliminate the need to "turn-around" the data bus required with common I/O devices. Accesses to the IDT71T62805 Read and Write ports are completely independent of one another. All accesses are initiated synchronously on the rising edge of the positive input clock (K). In order to maximize data throughout, both Read and Write ports are equipped with Double Data Rate (DDR) interfaces. Therefore, data can be transferred into the device on every rising edge of both input clocks (K and $\overline{K}$) and out of the device on every rising edge of the output clock (C and $\overline{C}$) thereby maximizing performance while simplifying system design.

Depth expansion is accomplished with a Port Select input for each port. Each Port Select allow each port to operate independently.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the C or $\overline{C}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Pin Description Summary

A_0 - A_{17}	Address Inputs	Input	Synchronous
$\overline{RPE}$	Read Port Enable	Input	Synchronous
$\overline{WPE}$	Write Port Enable	Input	Synchronous
$\overline{BW_0}$, $\overline{BW_1}$	Individual Byte Write Selects	Input	Synchronous
K, $\overline{K}$	Clock signals for Data, Address and Control Inputs	Input	N/A
C, $\overline{C}$	Data Output Clocks	Input	N/A
D_0 - D_{17}	Data Input	Input	Synchronous
Q_0 - Q_{17}	Data Output	Output	Synchronous
ZQ	Output Impedance Matching Input	Input	Static
TMS, TDI, TCK	JTAG Inputs	Input	N/A
TDO	JTAG Output	Input	N/A
V_{REF}	Reference Voltage Input	Input	Static
V_{DD}, V_{DDQ}	Core and Output Power	Supply	Static
V_{SS}	Ground	Supply	Static

5285 tbl 01

QDR SRAMs and Quad Data Rate comprise a new family of products developed by Cypress Semiconductor, IDT, Inc. and Micron Technology.

AUGUST 2000

Pin Definitions

Symbol	Pin Function	I/O	Active	Description
A_0 - A_{17}	Address Inputs	Input	N/A	Address inputs. Sampled on the rising edge of the K clock during active read and on the rising edge of the $\overline{K}$ clock during active write operations. These address inputs are multiplexed for both Read and Write operations. Internally, the device is organized 256Kx36 and delivered externally in two 18-bit words. Therefore, only 18 address inputs are needed to access the entire memory array. These inputs are ignored when appropriate port is deselected. Therefore, on the rising edge of the postive input clock (K), these inputs are ignored if the Read port is deselected. These inputs are ignored on the rising edge of the negative input clock ($\overline{K}$) when the Write port is deslected.
$\overline{RPE}$	Read port Enable	Input	Low	Read Port Enable. Sampled on the rising edge of positive input clock (K). When active, a Read operation is initiated. Deasserting will cause the Read port to be deselected. When deselected, the pending access is allowed to complete and the output drivers are automatically three-stated following the next rising edge of the C clock. The IDT71T62805 organized internally as 256Kx36. Each read access consists of a burst of two sequential 18-bit transfers over one clock cycle. The entire burst of two data words should be allowed to complete. Initiating Read accesses on two consecutive K clock rises is a valid operation resulting in two consecutive Read operations.
$\overline{WPE}$	Write Port Enable	Input	Low	Write Port Enable. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting will deselect the Write port. When deselected, the pending access is allowed to complete. The IDT71T62805 is organized internally as 256Kx18. Each write access consists of a burst of two sequential 18-bit transfers over one clock cycle. The entire burst of two data words should be allowed to complete. Initiating Write accesses on two consecutive K clock rises is a valid operation resulting in two consecutive Read Operations.
$\overline{BW_0}$, $\overline{BW_1}$	Individual Byte Write Enables	Input	Low	Byte Write Enables 0 and 1. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. $\overline{BW_0}$ controls $D_{[8:0]}$ while $\overline{BW_1}$ controls $D_{[17:9]}$. $\overline{BW_0}$ and $\overline{BW_1}$ are sampled on same edge as D[17:0]. Deselecting a Byte Write Enable will cause the corresponding byte of data to be ignored and not written into the device.
K	Master Clock	Input	N/A	Positive Input Clock Input. The rising edge of K is used to capture synchronous inputs (data, address and control) to the device and drive out data through Q[17:0} when in single clock mode.
$\overline{K}$	Master Clock	Input	N/A	Negative Input Clock Input. $\overline{K}$ is used to capture synchronous inputs (data, address and control) being presented to the device and drive out data through Q[17:0] when in single clock mode. All accesses are initiated on the rising edge of K.
C	Output Data Clock	Input	N/A	Positive Output Clock Input. C is used in conjuction with $\overline{C}$ clock out the Read data from the device. C and $\overline{C}$ can travel with the data to the receiving device. When used in this way C and $\overline{C}$ can be used to de-skew the flight times of various devices on the board (see application example).
$\overline{C}$	Output Data Clock	Input	N/A	Negative Output Clock Input. $\overline{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\overline{C}$ can travel with the data to the receiving device. When used in this way C and $\overline{C}$ can be used to de-skew the flight times of various devices on the board (see application example).
D_0 - D_{17}	Data Input	Input	N/A	Data Input signals, sampled on the rising edge of K and $\overline{K}$ clocks during the data portion of a valid write operation.
Q_0 - Q_{17}	Data Output	Output	N/A	Data Output signals. These pins drive out the requested data during a Read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during Read operations (or K and $\overline{K}$ when in single clock mode). When the read is deselected, Q[17:0} are automatically tri-stated.
ZQ	Programmable Impedance Matching	Input	N/A	Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. $Q_{[17:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternately, this pin can be connected to directly to V_{DD}, which enables the minimum impedance mode. This pin cannot be connected directly to Vss or left unconnected.

5285 tbl 02a

Pin Descriptions continued on Page 3.

Pin Definitions continued

Symbol	Pin Function	I/O	Active	Description
TMS	Test Mode Select	Input	N/A	Gives input command for TAP controller; sampled rising edge of TCK.
TDI	Test Data Input	Input	N/A	Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK.
TCK	Test Clock	Input	N/A	Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from falling edge of TCK.
TDO	Test Data Output	Output	N/A	Serial output of registers placed between TDI and TDO. This output is active dpending on state of TAP controller.
V_{REF}	Input Reference Voltage	Input	N/A	Reference Voltage Input. Static input used to set the reference level for HSTL inputs, nominally adjusted to improve system noise margin.
V_{DD}	Core Power Supply	N/A	N/A	Power supply inputs to the core of the device. Should be connected to 2.5V power supply.
V_{DDQ}	I/O Power Supply	N/A	N/A	Power supply inputs for the outputs of the device. Should be connected to 1.5V power supply.
V_{SS}	Core Ground	N/A	N/A	Ground for the core of the device. Should be connected to ground of the system.

5285 tbl 02b

Introduction

Functional Overview

The IDT71T62805 is a synchronous pipelined Burst SRAM equipped with both a Read Port and a Write Port. The Read port is dedicated to Read operations and the Write Port is dedicated to Write operations. Data flows into the SRAM through the Write port and out through the Read Port. The IDT71T62805 multiplexes the address inputs in order to minimize the number of address pins required. The IDT71T62805 latches the Read address on the rising edge of the positive input clock (K) and latches the Write address on the rising edge of the negative input clock ($\overline{K}$). By having separate Read and Write ports, the IDT71T62805 completely eliminates the need to "turn-around" the data bus and avoids any possible data contention, thereby simplifying system design.

Accesses for both ports are initiated by the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and $\overline{K}$) and all output timing is referenced to the output clocks, C and $\overline{C}$ (or K and $\overline{K}$ when in single clock mode.)

All synchronous data inputs ($D_{[17:0]}$) inputs pass through input registers controlled by the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[17:0]}$) outputs pass through output registers controlled by the rising edge of the output clocks (C and $\overline{C}$).

All synchronous control ($\overline{RPE}$, $\overline{WPE}$, $\overline{BW}_0$, $\overline{BW}_1$) inputs pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

Read Operations

Read operations are initiated by asserting $\overline{RPE}$ active at the rising edge of the positive input clock (K). The address presented to $A_{[17:0]}$ is stored in the Read address register. Because the IDT71T62805 is a 36-bit memory, it will access two 18-bit data words with each read operation. Following the next K clock rise the data is available to be latched out of the device, triggered by the C clock. On the following C clock rise the corresponding lower order word of data is driven onto the $Q_{[17:0]}$. On the subsequent rising edge of $\overline{C}$ the higher order data word is driven onto the $Q_{[17:0]}$. The requested data will be valid 2.5ns from the rising edge of the output clock (C or $\overline{C}$, 166MHz device). With the separate Input and Output ports and the internal logic determining when the device should drive the data bus, the QDR architecture has eliminated the need for an output enable input to control the state of the output drivers.

Read accesses can be initiated on every rising edge of the positive input clock (K). Doing so will pipeline the data flow such that data is transferred out of the device on every rising edge of the output clocks (C and $\overline{C}$). The IDT71T62805 will deliver the most recent data for the address location being accessed. This includes forwarding data when a Read and Write transactions to the same address location are initiated on the same clock rise.

When the read port is deselected, the IDT71T62805 will first complete the pending read tansactions. Synchronous internal circuitry will automatically three-state the outputs following the next rising edge of the positive output clock (C). This will allow for a seamless transition between devices without the insertion of wait states.

The IDT71T62805 is equipped with internal logic that synchronously controls the state of the output drivers. The logic inside the device determines when the output drivers need to be active or inactive. This advanced logic eliminates the need for an asynchronous output enable ($\overline{OE}$) since the device will automatically enable/disable the output drivers during the proper cycles. The IDT71T62805 will automatically power-up in a deselcted state with the outputs in a three state condition.

Write Operations

Write operations are initiated by asserting $\overline{WPE}$ active at the rising edge of the positive input clock (K). On the same clock rise (K) the data presented to $D_{[17:0]}$ is stored into the lower 18-bit Write Data register provided $\overline{BW}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$), the information presented to $A_{[17:0]}$

Introduction continued on Page 4.

Introduction *continued*

is latched and stored in the Write Address Register and the information presented to $D_{[17:0]}$ is also stored into the upper 18-bit Write Data Register provided $\overline{BW}_{[1:0]}$ are both asserted active. The 36 bits of data are then written into the memory array at the specified location.

Write accesses can be initiated on every rising edge of the positive clock. Doing so will pipeline the data flow such that 18-bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

Byte Write operations are supported by the IDT71T62805. A write operation is initiated by enabling the write port using $\overline{WPE}$. The bytes that are written are determined by $\overline{BW}_0$ and $\overline{BW}_1$ which are sampled with each set of 18-bit data word. Asserting the appropriate Byte Write Enable input during the data portion of a write will allow the data being presented to be latched and written into the device. De-asserting the Byte Write Enable input during the data portion of a write will allow the data stored in the device for that byte to remain unaltered. This feature can be used to simplify READ/MODIFY/WRITE operations to a Byte Write operation.

When deselected, the write port will ignore all inputs.

Single Clock Mode

The IDT71T62805 can be used with a single clock mode. In this mode the device will recognize only the pair of input clocks (K and $\overline{K}$) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/$\overline{K}$ and C/$\overline{C}$ clocks. All timing parameters remain the same in this mode. To use this mode of operation, the user must tie C and $\overline{C}$ to V_{DD}. During power-up, the device will sense the single clock input and operating in either single clock or double clock mode. The clock mode should not be changed during device operation.

Concurrent Transactions

The Read and Write ports on the IDT71T62805 operate completely independently of one another. Since each port latches the address inputs on different clock edges, the user can Read or Write to any location, regardless of the transaction on the other port. Should the Read and Write ports access the same location on the rising edge of the positive input clock, the information presented to the $D_{[17:0]}$ will be forwarded to the $Q_{[17:0]}$ such that no latency is required to access valid data. Coherency is conducted on cycle boundaries. Once the second word of data is latched into the device, the write operation is considered completed. At this point, any access to that address location will receive that data until altered by a subsequent Write operation. Coherency is not maintained for Write operations initiated in the cycle after a Read.

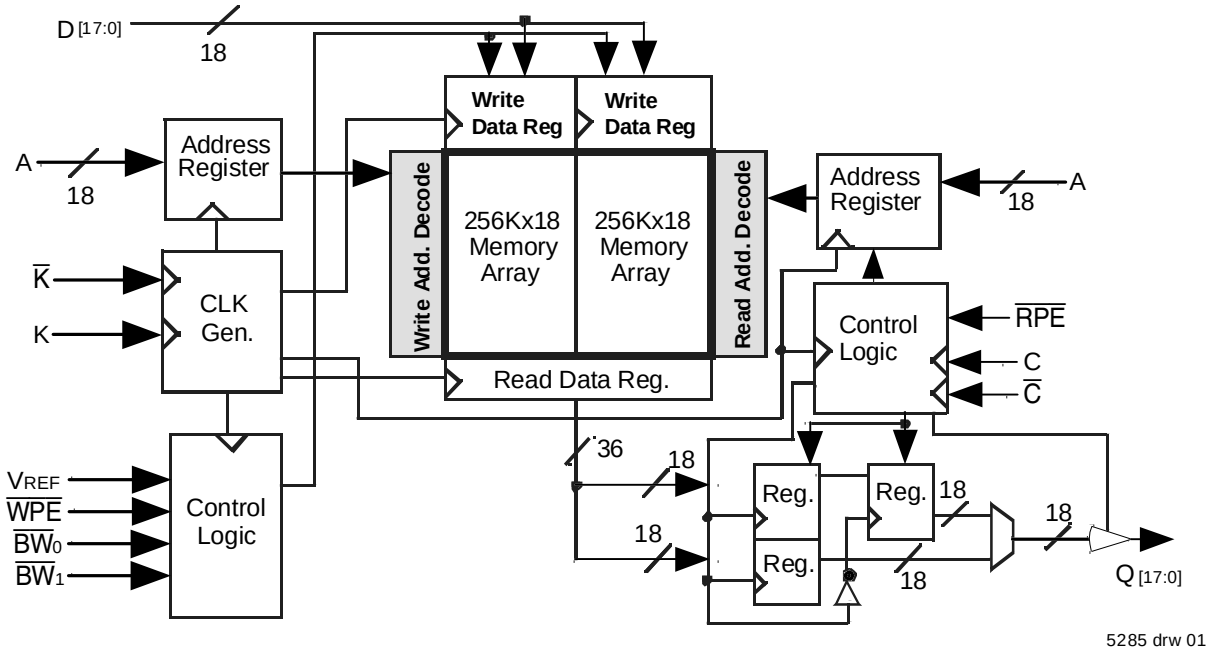
Depth Expansion

The IDT71T62805 has a Port Enable input for each port. This allows for easy depth expansion. Both Port Enables are sampled on the rising edge of the positive input clock only (K). Each port enable input can disable the specified port. Disabling a port will not affect the other port. All pending transactions (Read and Write) will be completed prior to the device being disabled.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM, The allowable range of RQ to guarantee impedance matching with a tolerance of +/-10% is between 175Ω and 350Ω, with V_{DDQ}=1.5V. The output impedance is adjusted every 1024 cycles to adjust for drifts in supply voltage and temperature.

Functional Block Diagram



Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature(1)	VSS, VSSQ	VDD	VDDQ
Commercial	0°C to +70°C	OV	2.5 ± 100mV	1.4V to 1.9V

5285 tbl 03

NOTE:
1. TA is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Power Supply Voltage	2.4	2.5	2.6	V
VDDQ	I/O Supply Voltage	1.4	1.5	1.9	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	VREF+0.1	–	VDDQ+0.3	V
VIL	Input Low Voltage	–0.3(1)	–	VREF–0.1	V

5285 tbl 04

NOTE:
1. -2.0V for pulse duration less than 20ns.

Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11
A	DNU	V_{SS}(2)	NC(1)	$\overline{WPE}$	$\overline{BW_1}$	$\overline{K}$	NC	$\overline{RPE}$	NC(1)	V_{SS}(2)	DNU
B	NC	Q_9	D_9	A_{16}	NC	K	$\overline{BW_0}$	A_{17}	NC	NC	Q_8
C	NC	NC	D_{10}	V_{SS}	A_2	A_0	A_1	V_{SS}	NC	Q_7	D_8
D	NC	D_{11}	Q_{10}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D_7
E	NC	NC	Q_{11}	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D_6	Q_6
F	NC	Q_{12}	D_{12}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q_5
G	NC	D_{13}	Q_{13}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D_5
H	NC	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D_{14}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q_4	D_4
K	NC	NC	Q_{14}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D_3	Q_3
L	NC	Q_{15}	D_{15}	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q_2
M	NC	NC	D_{16}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q_1	D_2
N	NC	D_{17}	Q_{16}	V_{SS}	A_3	A_4	A_5	V_{SS}	NC	NC	D_1
P	NC	NC	Q_{17}	A_6	A_7	C	A_8	A_9	NC	D_0	Q_0
R	TDO	TCK	A_{10}	A_{11}	A_{12}	$\overline{C}$	A_{13}	A_{14}	A_{15}	TMS	TDI

5285 tbl 12

165-ball FBGA Pinout
TOP VIEW

NOTE:
1. 9A and 3A are reserved for future 18M and 36M respectively.
2. 10A and 2A are reserved for future 72M and 144M respectively. This should be connected to Vss on the IDT71T62805.

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Supply Voltage on VDD with Respect to GND	–0.5 to +3.6	V
V_{TERM}(3)	DC Input Voltage(5)	–0.5 to V_{DDQ}+0.5	V
V_{TERM}(4)	DC Voltage Applied to Outputs in High-Z State(5)	–0.5 to V_{DDQ}+0.5	V
T_A(6)	Operating Temperature	0°C to 70°C	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Current into Outputs (Low)	20	mA

5285 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. Input terminals.
4. Output terminals.
5. Minimum voltage equals –2.0V for pulse duration less than 20ns.
6. T_A is the "instant on" case temperature.

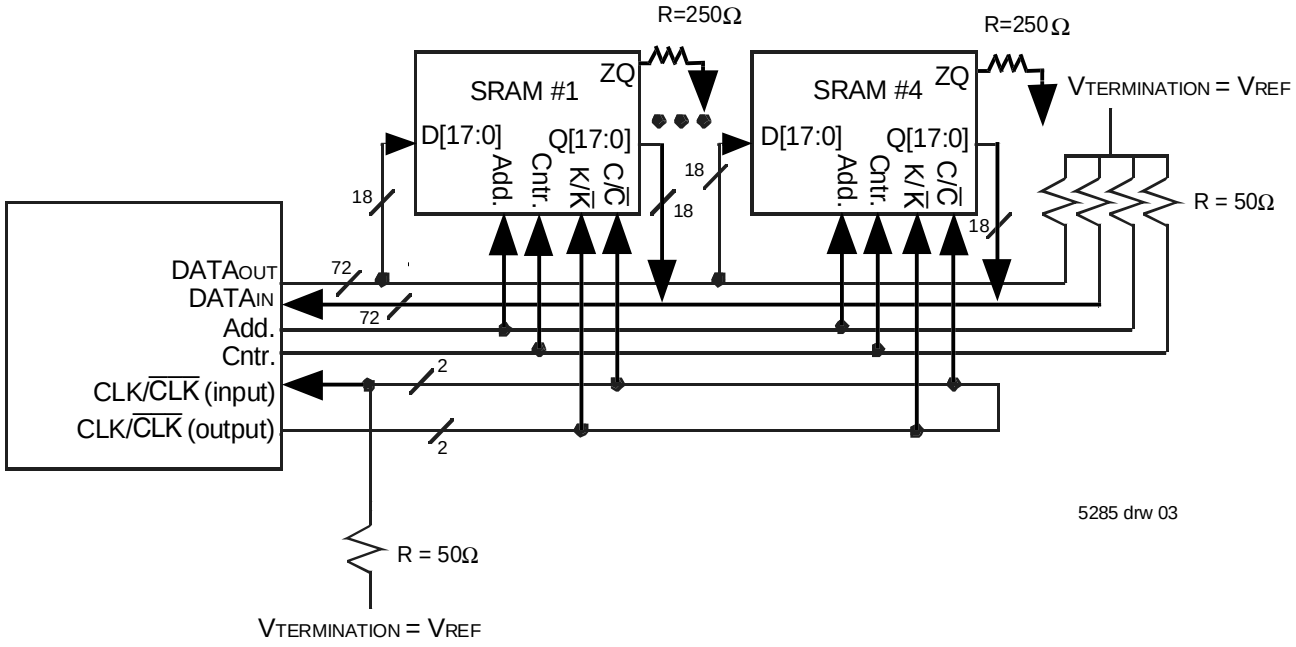
Capacitance (T_A = +25°C, f = 1.0MHz)(1)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{DD} = 2.5V, V_{DDQ} = 1.5V	5	pF
C_{CLK}	Clock Input Capacitance		6	pF
C_O	Output Capacitance		7	pF

5285 tbl 06

NOTE:
1. Tested initially and after any design or process change that may affect these parameters.

Application Example



Read Port Cycle Description Truth Table[1,2]

Operation	Address Used	$\overline{RPE}$	K	Comments
Deselected	—	H	L–H	Read port is deselected. Outputs three-state following next rising edge of negative input clock ($\overline{K}$) if in single clock mode, or $\overline{C}$ if using C and $\overline{C}$ as output clocks.
Begin Read	External	L	L–H	Read operation initiated. Addresses are stored in the Read Address Register. Following the next K clock rise the first (lower order) 18-bit word will be available to be driven out onto $Q_{[17:0]}$ gated by the rising edge of the output clock C. On the subsequent rising edge of the negative output clock ($\overline{C}$) the second (higher order) 18-bit word is driven out onto $Q_{[17:0]}$.

5285 tbl 07

Write Port Cycle Description Truth Table[1,2,3,4,5]

Operation	Address Used	$\overline{WPE}$	K	Comments
Deselected	—	H	L–H	$\overline{WPE}$ deselects Write Port. All Write Port inputs are ignored during this clock rise and the subsequent rising edge of the negative input clock ($\overline{K}$).
Begin Read	External on next rising edge of $\overline{K}$	L	L–H	Write operation initiated. The information presented to $D_{[17:0]}$ is stored in the Write Data Register. On the subsequent rising edge of the negative input clock ($\overline{K}$) the device will latch the addresses presented to $A_{[17:0]}$ and the data presented to $D_{[17:0]}$. The entire 36 bits of information will then be written into the memory array. See Write Description table for byte write information.

5285 tbl 08

NOTES:
1. X = Don't Care, H = Logic High, L = Logic Low.
2. Device will power-up deselected and the outputs in a three-state condition.
3. $\overline{BW}_0$ and $\overline{BW}_1$ asserted active LOW during all cycles. For byte write operations, see Write Description table.
4. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on C and $\overline{C}$ rising edges, except when in single clock mode.
5. It is recommended that K = $\overline{K}$# and C = $\overline{C}$# when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

Write Descriptions[1]

Operation	$\overline{BW}_0$	$\overline{BW}_1$	K	$\overline{K}$	Comments
Write Initiated	L	L	L–H	—	Both bytes ($D_{[17:0]}$) are written into the low order 18-bit write buffer device during this portion of a write operation.
Write Completed — Write initiated on previous K clock rise	L	L	—	L–H	Both bytes ($D_{[17:0]}$) are written into the higher order 18-bit write buffer device during this portion of a write operation. The contents of the entire 36-bits write buffer are written into the memory array.
Write Initiated	L	H	L–H	—	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
Write Completed — Write initiated on previous K clock rise	L	H	—	L–H	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
Write Initiated	H	L	L–H	—	During the Data portion of a Write sequence, only the upper byte ($D_{17:9]}$) is written into the device. $D_{[8:0]}$ will remain unaltered.
Write Completed — Write initiated on previous K clock rise	H	L	—	L–H	During the Data portion of a Write sequence, only the upper byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ will remain unaltered.
Write — NO-OP	H	H	L–H	—	No data is written into the device during this portion of a write operation.
Write — NO-OP	H	H	—	L–H	No data is written into the device during this portion of a write operation.

5285 tbl 09

NOTE:
1. Assumes a Write cycle was initiated per the Write Port Cycle Description Truth Table. $\overline{BW}_0$ and $\overline{BW}_1$ can be altered on different portions of a write cycle, as long as the set-up and hold requirements are achieved.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 2.5 ± 100mV, V_{DDQ} = 1.4V to 1.9V)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	GND ≤ V_I ≤ V_{DD}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled	—	5	µA
$V_{OL\ (Low)}$	Output Low Voltage(3)	I_{OL} ≤ 0.1mA	Vss	0.2	V
V_{OL}		Note 1	V_{DDQ}/2 - 0.08	V_{DDQ}/2 + 0.08	V
$V_{OH\ (Low)}$	Output High Voltage(3)	$\|I_{OH}\|$ ≤ 0.1mA	V_{DDQ} - 0.2	V_{DDQ}	V
V_{OH}		Note 2	V_{DDQ}/2 - 0.08	V_{DDQ}/2 + 0.08	V
V_{REF}	Input Reference Voltage	Typical Value = 0.75V	0.68	0.9	V

NOTES:
5285 tbl 10a

1. Output Impedance is programmmable I_{OL}=(V_{DDQ}/2)/(R_{ZQ}/5) for values 175ohm ≤ R_{ZQ} ≤ 350ohms.
2. Output Impedance is programmmable I_{OH}=(V_{DDQ}/2)/(R_{ZQ}/5) for values 175ohm ≤ R_{ZQ} ≤ 350ohms.
3. HSTL outputs meet JEDEC HSTL Class I and Class II standards.

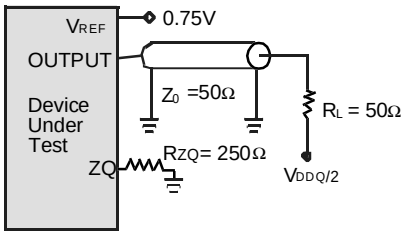
DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 2.5 ± 100mV, V_{DDQ} = 1.4V to 1.9V)

Symbol	Parameter	Test Conditions	S166	S133	S100	Unit
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0mA, f = f_{MAX}(2) = 1/t_{CYC}	550	450	330	mA
I_{SB1}	Automatic Power-Down Current	Max. V_{DD}, Both Ports Deselected, Inputs Static, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}(3) = 1/t_{CYC}	100	80	60	mA

NOTES:
5285 tbl 10b

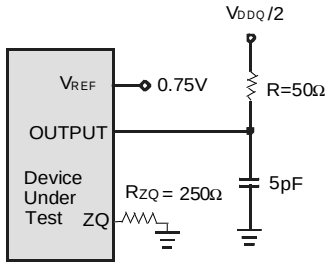
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC}; f=0 means no input lines are changing.
3. Clock Inputs.

AC Test Loads



5285 drw 04

(a)



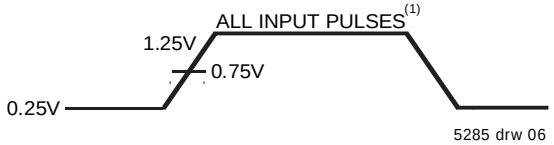
5285 drw 05

(b)

AC Test Conditions

Input Pulse Levels	0.25V to 1.25V
Input Rise/Fall Times	2V/ns
Input Timing Reference Levels	0.75V
Output Timing Reference Levels	0.75V
AC Test Load	See Figures a and b

5285tbl 11a



5285 drw 06

NOTE:
1. Unless otherwise noted, test conditions assume signal transition time of 2V/ns, timing reference levels of 0.75V, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance showing in (a) of AC Test Loads.

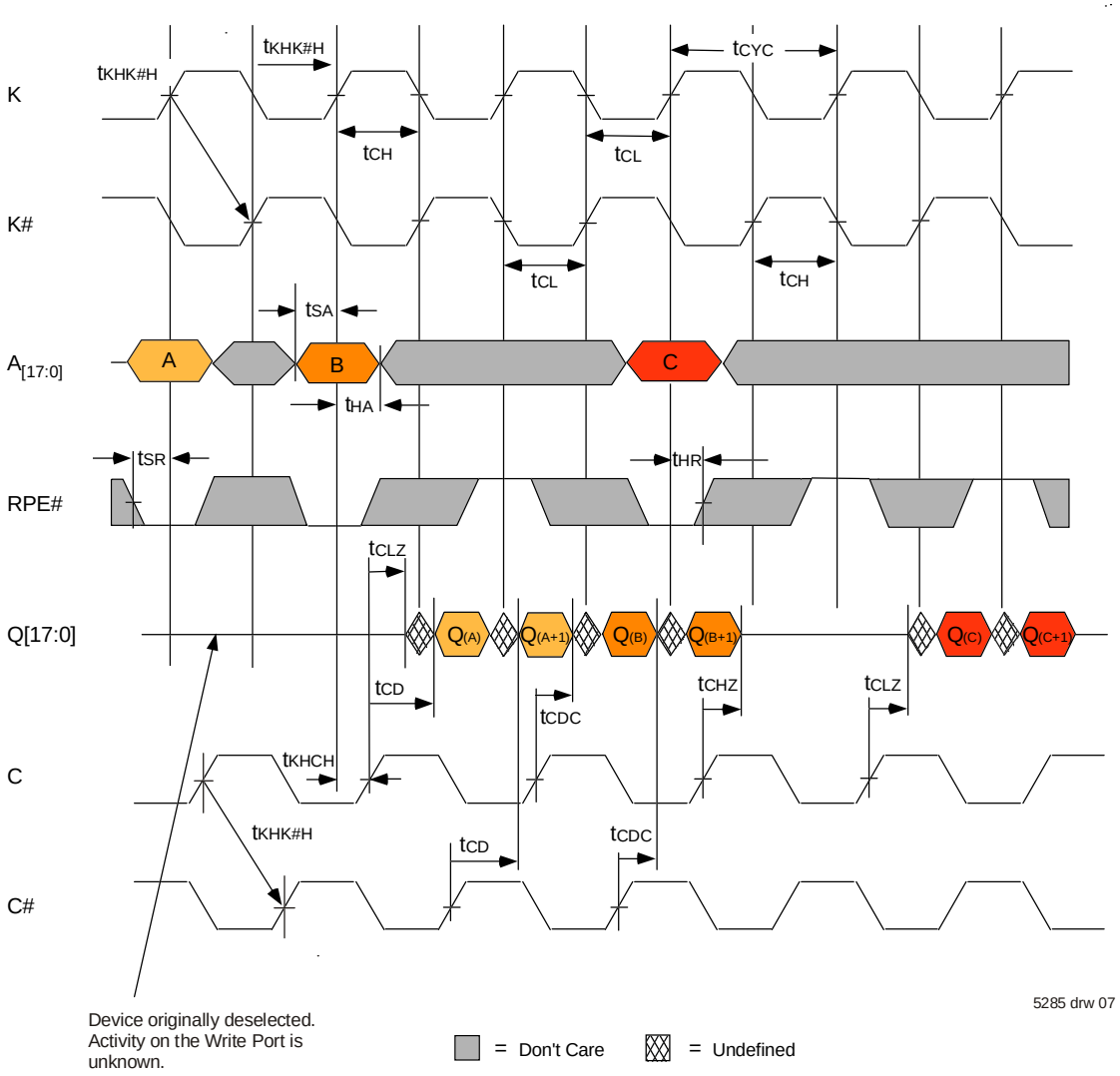
AC Electrical Characteristics (V_{DD} = 2.5 ± 100mV, V_{DDQ} = 1.4V to 1.9V)[3]

Symbol	Parameter	IDT71T62805S166		IDT71T62805S133		IDT71T62805S100		Unit
		Min.	Max	Min.	Max	Min.	Max	
Clock Parameters								
t_{CYC}	K Clock and C Clock Cycle Time	6.0	—	7.5	—	10.0	—	ns
t_{CH}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) High Pulse Width	2.4	—	3.2	—	3.5	—	ns
t_{CL}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) Low Pulse Width	2.4	—	3.2	—	3.5	—	ns
$t_{KHK\#H}$	K Clock Rise to $\overline{K}$ Clock Rise and C to $\overline{C}$ Rise (Rising Edge to Rising Edge)	2.7	3.3	3.4	4.1	4.4	5.4	ns
t_{KHCH}	K Clock Rise to C Clock Rise and $\overline{K}$ and $\overline{C}$ Rise(Rising Edge to Rising Edge)	0.0	2.0	0.0	2.5	0.0	3.0	ns
Output Parameters								
t_{CD}	C/$\overline{C}$ Clock Rise (or K/$\overline{K}$ in Single Clock Mode) to Data Valid	—	2.5	—	3.0	—	3.0	ns
t_{CDC}	Data Output Hold After Output C/$\overline{C}$ Clock Rise (Active to Active)	1.2	—	1.2	—	1.2	—	ns
t_{CLZ}[1,2,4]	Clock (C and $\overline{C}$) Rise to Low-Z	1.2	—	1.2	—	1.2	—	ns
t_{CHZ}[1,2,4]	Clock (C and $\overline{C}$) Rise to High-Z (Active to High-Z)	—	2.5	—	3.0	—	3.0	ns
Set-Up Times								
t_{SA}	Address Set-Up to Clock (K and $\overline{K}$) Rise	0.7	—	0.8	—	1.0	—	ns
t_{SD}	$D_{[17:0]}$ Set-Up to Clock (K and $\overline{K}$) Rise	0.7	—	0.8	—	1.0	—	ns
t_{SR}	$\overline{RPE}$ Set-Up to Clock K Rise	0.7	—	0.8	—	1.0	—	ns
t_{SW}	$\overline{WPE}$ Set-Up to Clock K Rise	0.7	—	0.8	—	1.0	—	ns
t_{SB}	$\overline{BW_0}$, $\overline{BW_1}$ Set-Up to Clock K and $\overline{K}$ Rise	0.7	—	0.8	—	1.0	—	ns
Hold Times								
t_{HA}	Address Hold After Clock (K and $\overline{K}$) Rise	0.7	—	0.8	—	1.0	—	ns
t_{HD}	$D_{[17:0]}$ Hold After Clock (K and $\overline{K}$) Rise	0.7	—	0.8	—	1.0	—	ns
t_{HR}	$\overline{RPE}$ Hold After Clock K Rise	0.7	—	0.8	—	1.0	—	ns
t_{HW}	$\overline{WPE}$ Hold After Clock K Rise	0.7	—	0.8	—	1.0	—	ns
t_{HB}	$\overline{BW_0}$, $\overline{BW_1}$ Hold After Clock K and $\overline{K}$ Rise	0.7	—	0.8	—	1.0	—	ns

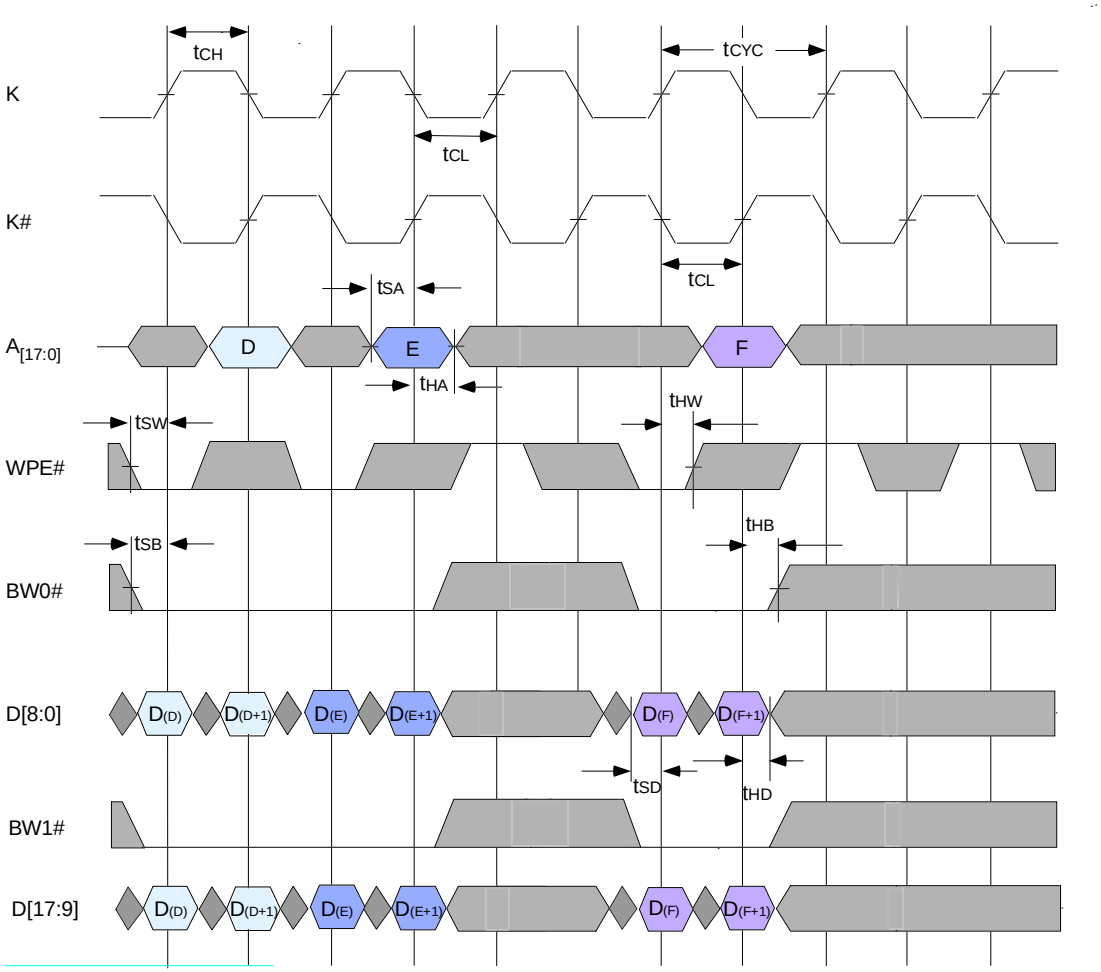
5285 tbl 11

NOTES:
1. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5pF as shown in (b) of AC Test Loads. Transition is measured ±100 mV from steady-state voltage.
2. At any given voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CD}.
3. Unless otherwise noted, test conditions assume signal transition time of 2V/ns, timing reference levels of 0.75V, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance showing in (a) of AC Test Loads.
4. These parameters are guaranteed with the AC load (b) by device characterization. They are not tested in production.

Timing Waveform of Read/Deselect Cycle



Timing Waveform of Write/Deselect Cycle

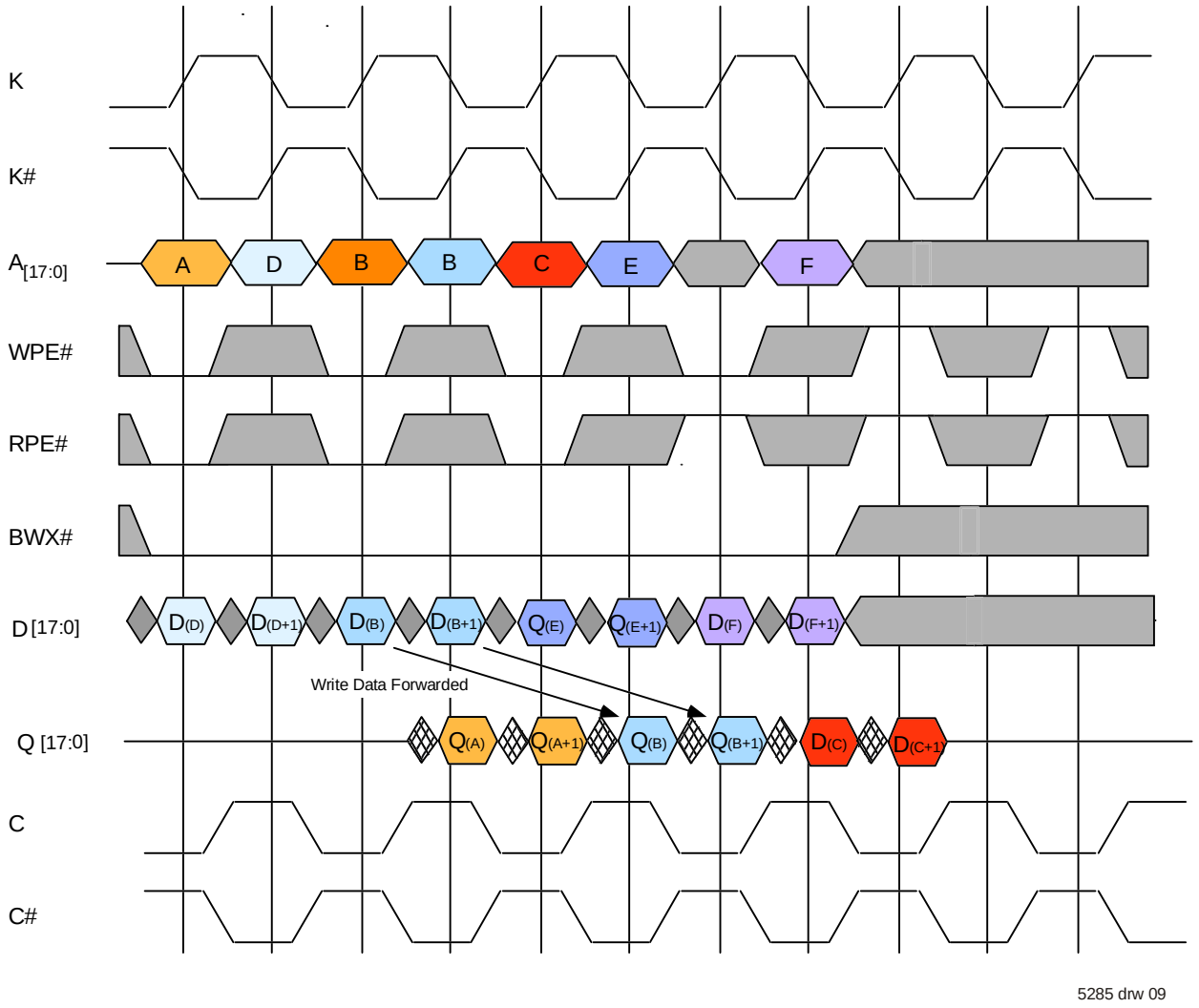


$\overline{BW}x$ is both $\overline{BW}_0$ and $\overline{BW}_1$.

5285 drw 08

= Don't Care = Undefined

Timing Waveform of Combined Read and Write Cycles

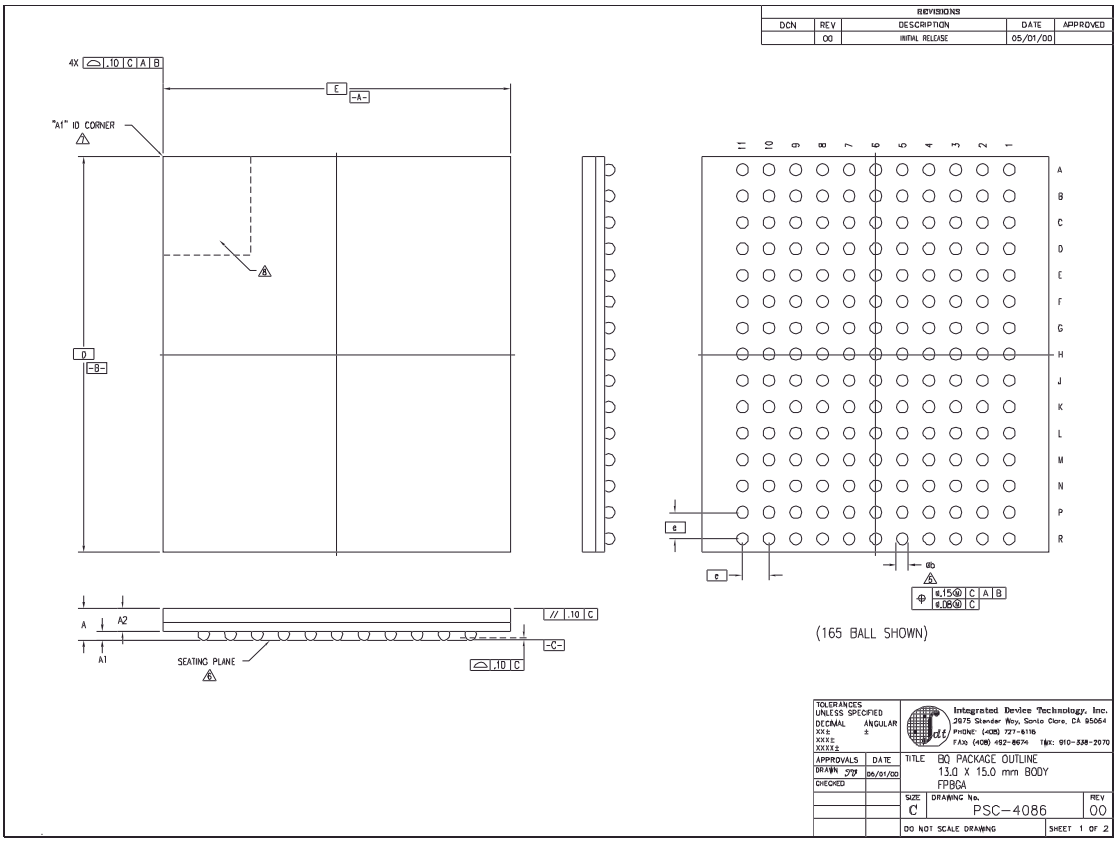


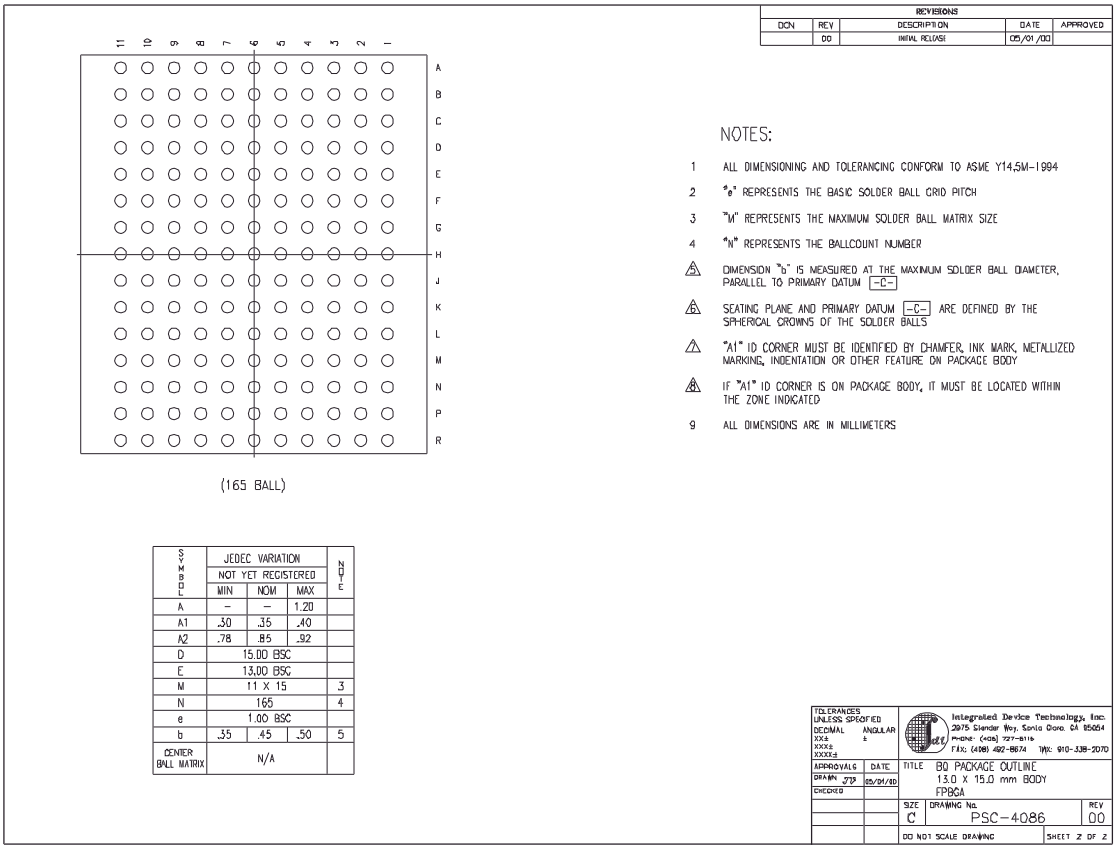
5285 drw 09

Read Port previously deselected. $\overline{BW}$x assumed active.

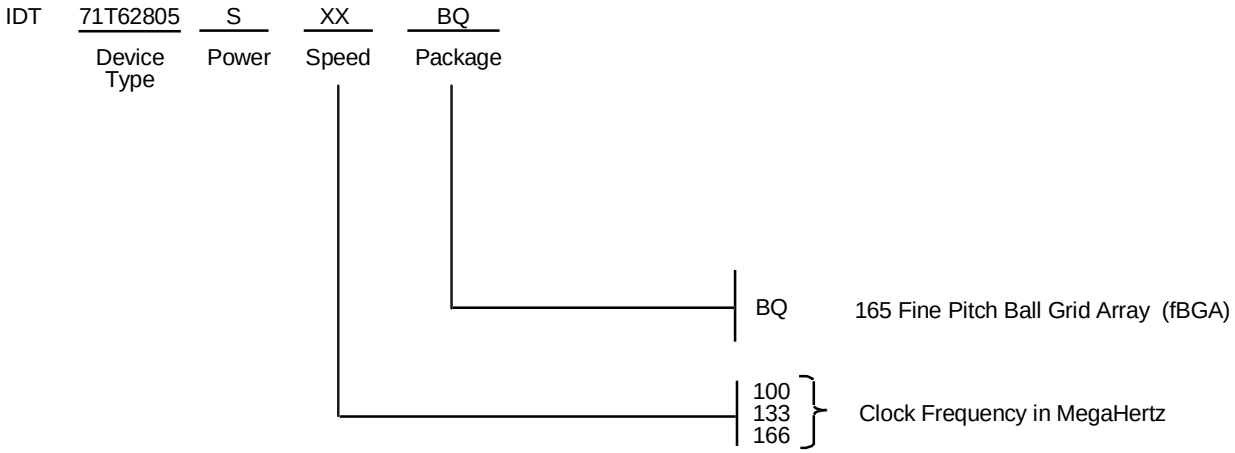
= Don't Care = Undefined

Package Diagram Outline for 165-Ball Fine Pitch Grid Array





Ordering Information



PART NUMBER	t_{CD} PARAMETER	DATA RATE	SPEED IN MEGAHERTZ	CLOCK CYCLE TIME
71T62805S100BQ	3.0 ns	200 MHz	100 MHz	10.0 ns
71T62805S133BQ	3.0 ns	266MHz	133 MHz	7.5 ns
71T62805S166BQ	2.5 ns	333MHz	166 MHz	6.0 ns

5285 drw 15

Advanced Datsheet:

"Advance Information" datasheets contain intial descriptions, subject to change, for products which are in development, including features and block diagrams.

Datasheet Document History

02/16/00		Created Datasheet
02/19/00	Pg 2,3,6	Modified Pin Defintions and Pin Configuration
	Pg 7	Modified Absolute Max Ratings
	Pg 10	Update DC Electrical Characteristics. Added Note #3.
	Pg 11	Modified AC electrical Characteristics. Added Note #4.
	Pg 12-14	ModifiedTiming Wave Diagrams
02/29/00	Pg 16	Modified Ordering Information
07/21/00	Pg. 3	Clarified V_{REF} definition
	Pg. 5,8,9	Labeled input and output databus D[17:0] and Q[17:0] for consistency
	Pg. 6	Changed NC A1 and A11 to DNU
	Pg. 7	Removed V_{ESD} and I_{LU}, refer to IDT corporate reliability report; Specified note on T_A parameter
	Pg. 8	Clarified $V_{TERMINATION}$ levels
	Pg. 10	Corrected AC Test Load reference levels and rise and fall conditions; Corrected DC output parameter V_{OH}, V_{OL}, I_{OH}, I_{OL} in reference to impedance controlled by ZQ functionality
	Pg. 11,12	Renamed clock parameters tKHKH to tKHK#H
	Pg. 15	Added BQ165 package diagram outline
	Pg. 16	Corrected ordering information package designator, from BF to BQ
08/12/00		Change part number to IDT71T62805

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
sramhelp@idt.com
800-544-7726, x4033