7542 Group
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0006-0200Z
Rev.2.00
2003.04.21

DESCRIPTION

The 7542 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7542 Group has serial I/Os, 8-bit timers, 16-bit timers, and an A-D converter, and is useful for control of home electric appliances and office automation equipment.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .. ***0.25 µs (Target Spec.)***
  (at 8 MHz oscillation frequency, double-speed mode for the shortest instruction)
- Memory size
  Flash memory version: ROM .... 32K + 4K bytes
  RAM .... 1024 bytes
  Mask ROM version: ROM .... 8K to 16K bytes
  RAM .... 384 to 512 bytes
  RSS version RAM .... 1024 bytes
- Programmable I/O ports .... 29 (25 in 32-pin version)
- Interrupts .... 18 sources, 16 vectors
  (14 sources, 14 vectors in 32-pin version)
- Timers .... 8-bit ✕ 2
  .... 16-bit ✕ 2
- Output compare 4-channel
- Input capture 2-channel
- Serial I/O .... 8-bit ✕ 2 (UART or Clock-synchronized)
- A-D converter .... 10-bit ✕ 8 channels
  .... (6 channels in 32-pin version)
- Clock generating circuit .... Built-in type
  (low-power dissipation by a ring oscillator)
  (connected to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer .... 16-bit ✕ 1
- Power source voltage
  X_{IN} oscillation frequency at ceramic oscillation, in double-speed mode
  At 8 MHz .... ***TBD***
  X_{IN} oscillation frequency at ceramic oscillation, in high-speed mode
  At 8 MHz .... 4.0 to 5.5 V
  At 4 MHz .... 2.4 to 5.5 V
  At 2 MHz .... 2.2 to 5.5 V
  X_{IN} oscillation frequency at RC oscillation in high-speed mode or middle-speed mode
  At 4 MHz .... 4.0 to 5.5 V
  At 2 MHz .... 2.4 to 5.5 V
  At 1 MHz .... 2.2 to 5.5 V
- Power dissipation .... ***TBD***
- Operating temperature range .... –20 to 85 °C
  (–40 to 85 °C for extended operating temperature version)
  (–40 to 125 °C for extended operating temperature 125 °C version (**Note 1**))

Notes 1: In this version, the operating temperature range and total time are limited as follows;
55 °C to 85 °C: within total 6000 hours,
85 °C to 125 °C: within total 1000 hours.
2: This is not a final specification. Some parametric limits are subject to change.Please contact Renesas or an authorized Renesas product distributor in the case of examination of use.

APPLICATION

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, car, etc.

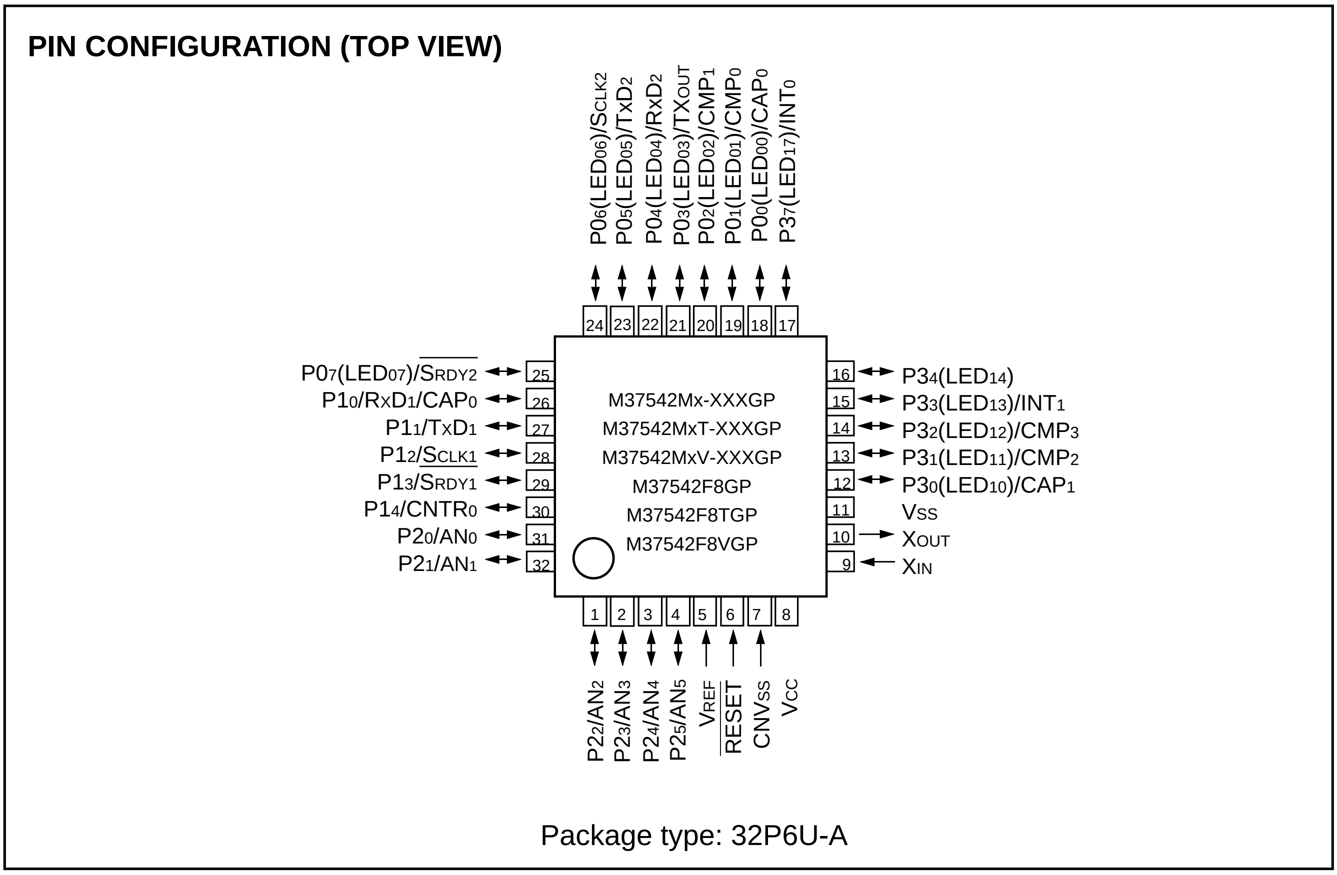


Fig. 1 Pin configuration (Package type: 32P6U-A)

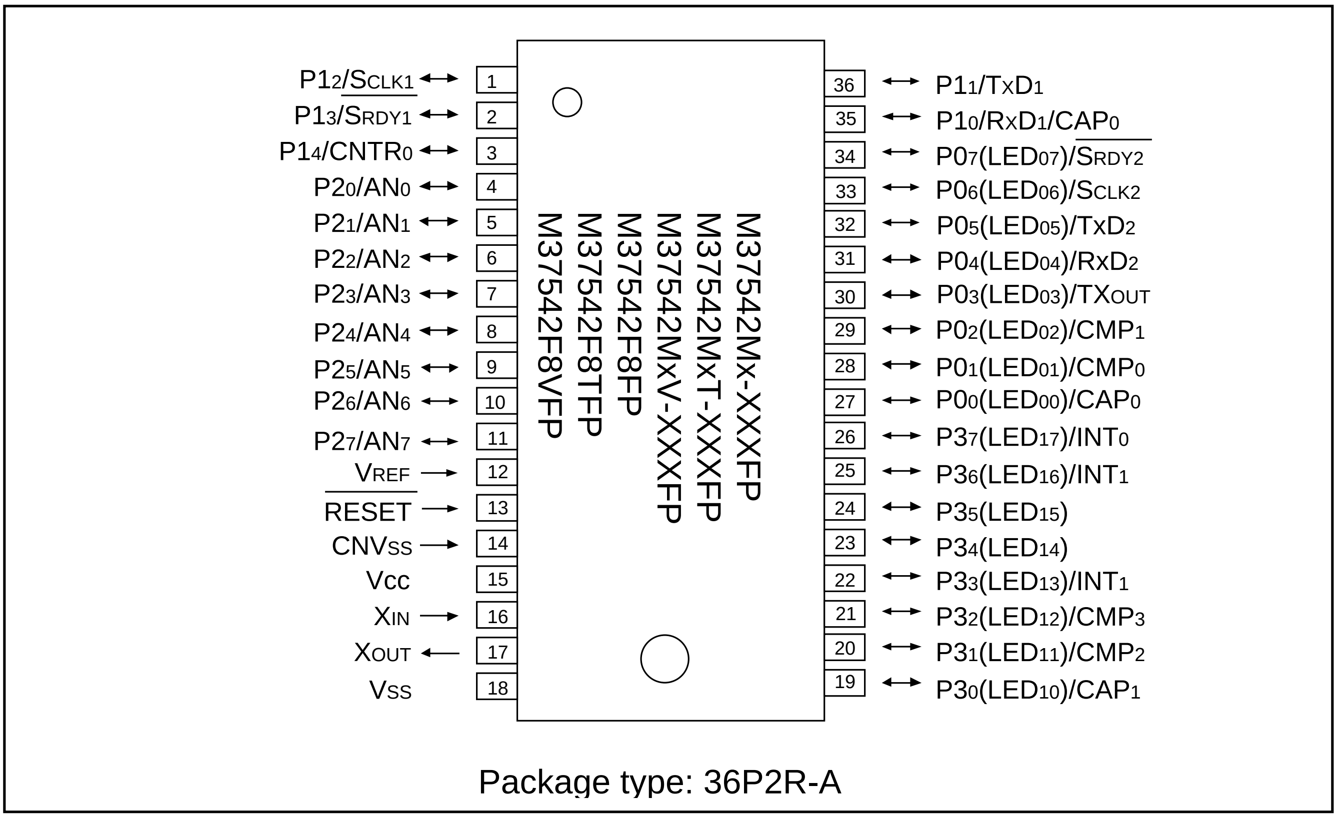


Fig. 2 Pin configuration (Package type: 36P2R-A)

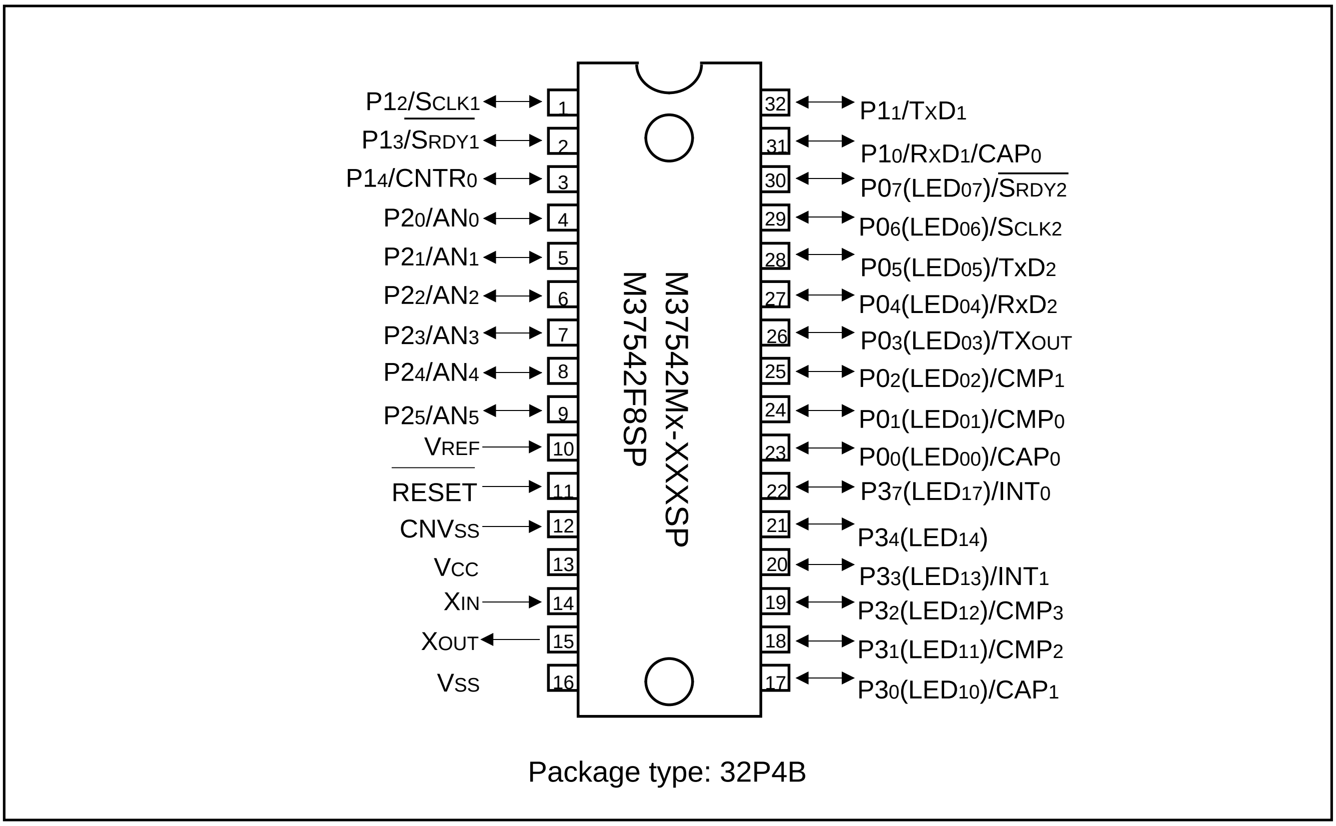


Fig. 3 Pin configuration (Package type: 32P4B)

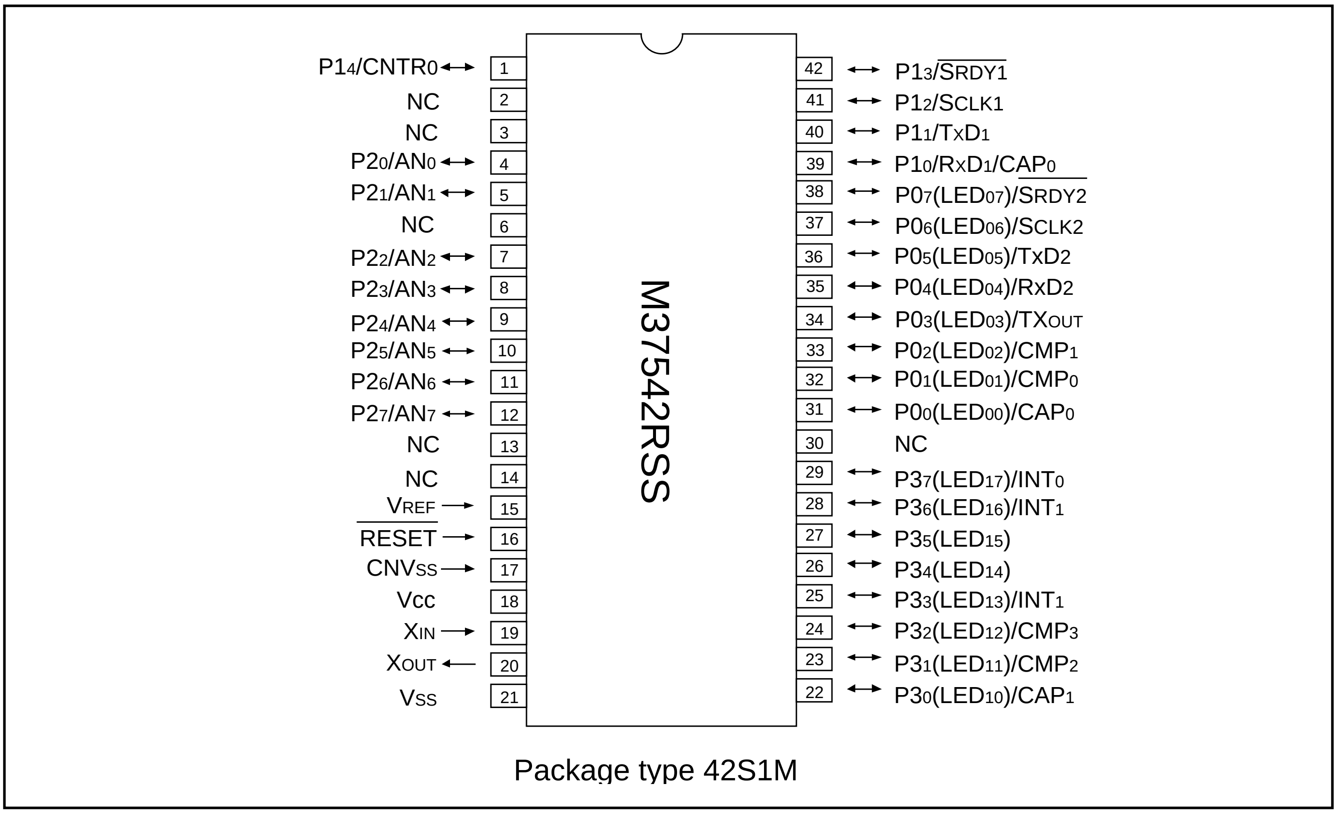


Fig. 4 Pin configuration (Package type: 42S1M)

FUNCTIONAL BLOCK

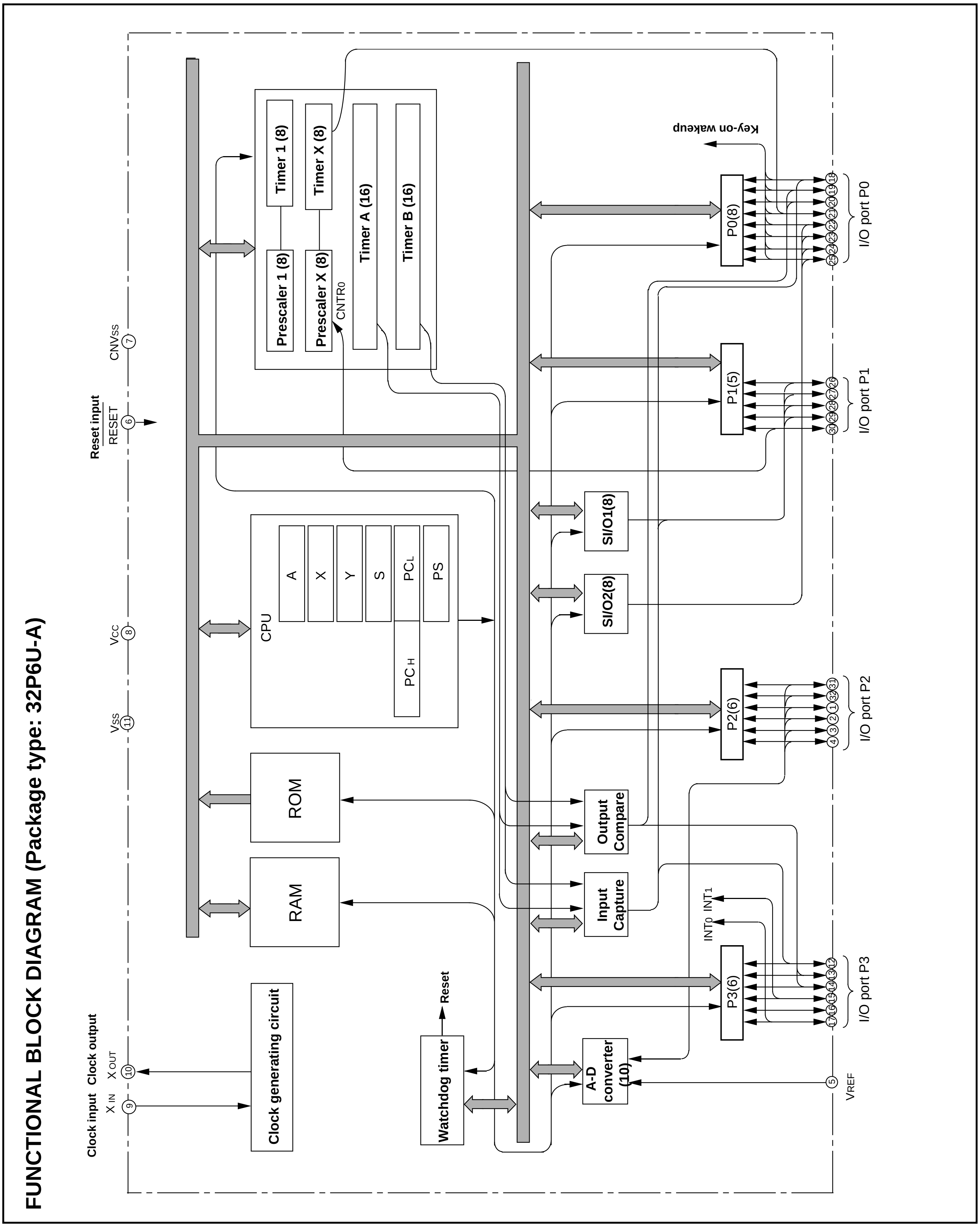


Fig. 5 Functional block diagram (Package type: 32P6U-A)

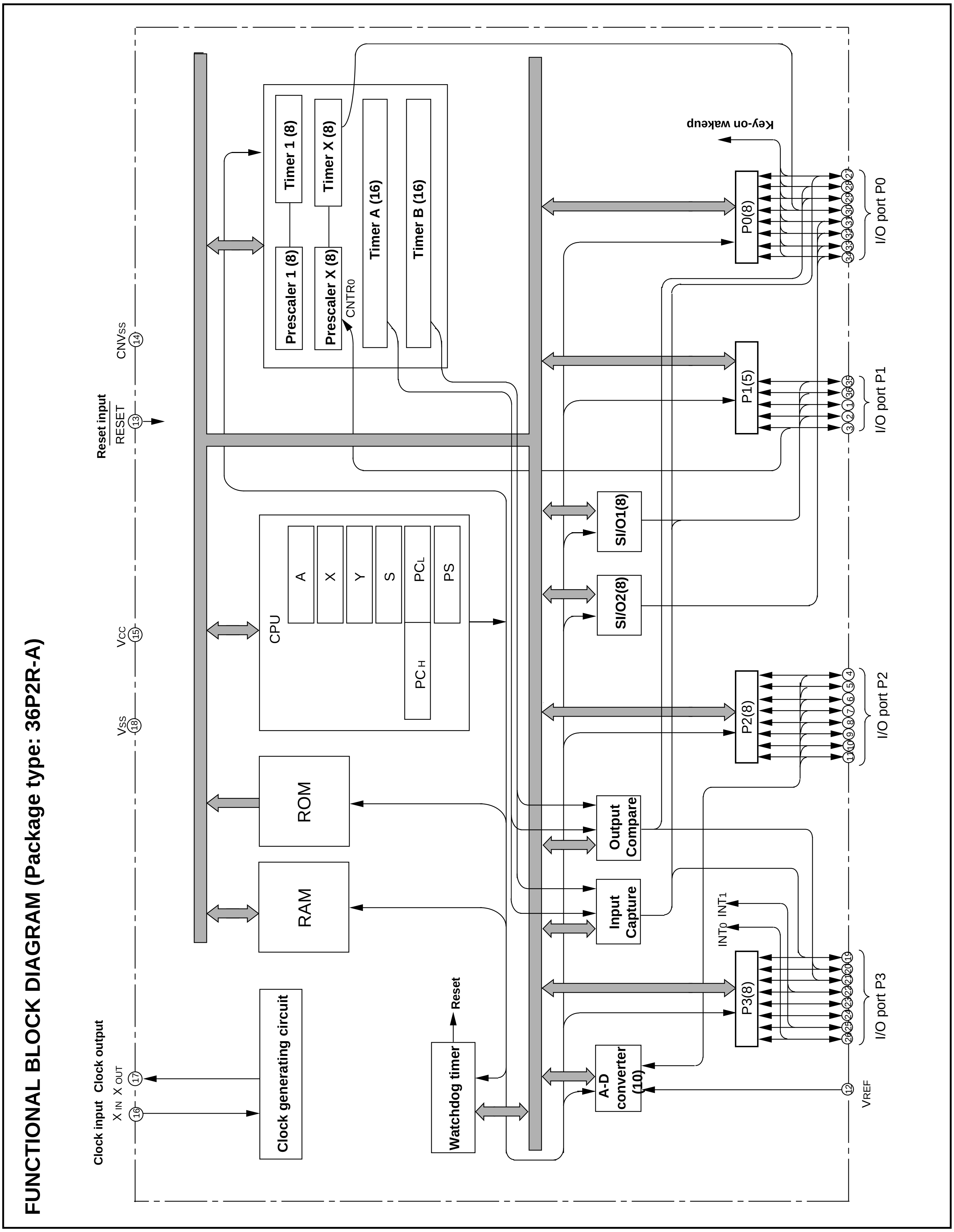


Fig. 6 Functional block diagram (Package type: 36P2R-A)

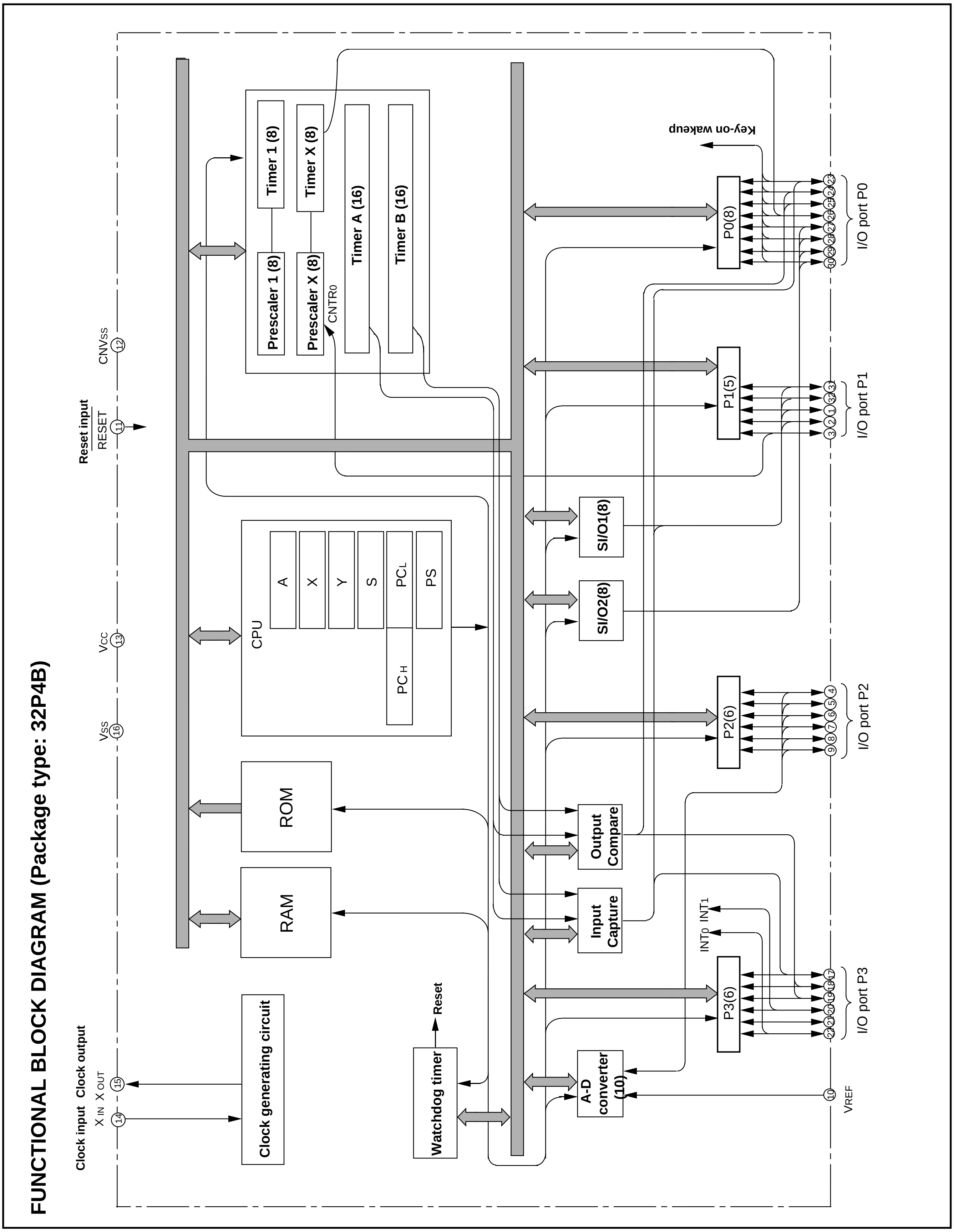


Fig. 7 Functional block diagram (Package type: 32P4B)

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function	
Vcc, Vss	Power source (Note 1)	•Apply voltage of 2.2 to 5.5 V to Vcc, and 0 V to Vss.		
V_{REF}	Analog reference voltage	•Reference voltage input pin for A-D converter.		
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.		
$\overline{RESET}$	Reset input	•Reset input pin for active "L"		
X_{IN}	Clock input	•Input and output pins for main clock generating circuit. •Connect a ceramic resonator or quartz crystal oscillator between the X_{IN} and X_{OUT} pins. •For using RC oscillator, short between the X_{IN} and X_{OUT} pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. •When the ring oscillator is selected as the main clock, connect X_{IN} pin to V_{CC} and leave X_{OUT} open.		
X_{OUT}	Clock output			
$P0_0(LED_{00})/CAP_0$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program. • High drive capacity for LED drive port can be selected by program.	• Capture function pin	• Key-input (key-on wake up interrupt input) pin
$P0_1(LED_{01})/CMP_0$ $P0_2(LED_{02})/CMP_1$			• Compare function pin	
$P0_3(LED_{03})/TX_{OUT}$			• Timer X function pin	
$P0_4(LED_{04})/RxD_2$ $P0_5(LED_{05})/TxD_2$ $P0_6(LED_{06})/S_{CLK2}$ $P0_7(LED_{07})/\overline{S_{RDY2}}$			• Serial I/O2 function pin	
$P1_0/RxD_1/CAP_0$	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for $P1_0$, $P1_2$ and $P1_3$	• Serial I/O1 function pin • Capture function pin	
$P1_1/TxD_1$ $P1_2/S_{CLK1}$ $P1_3/\overline{S_{RDY1}}$			• Serial I/O1 function pin	
$P1_4/CNTR_0$			• Timer X function pin	
$P2_0/AN_0$–$P2_7/AN_7$	I/O port P2 (Note 2)	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	• Input pins for A-D converter	
$P3_0(LED_{10})/CAP_1$	I/O port P3 (Note 3)	•8-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for $P3_6$ and $P3_7$). •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program. • High drive capacity for LED drive port can be selected by program.	• Capture function pin	
$P3_1(LED_{11})/CMP_2$ $P3_2(LED_{12})/CMP_3$			• Compare function pin	
$P3_3(LED_{13})/INT_1$			• Interrupt input pin	
$P3_4(LED_{14})$ $P3_5(LED_{15})$				
$P3_6(LED_{16})/INT_1$ $P3_7(LED_{17})/INT_0$			• Interrupt input pin	

Notes 1: V_{CC} = 2.4 to 5.5 V for the extended operating temperature version and the extended operating temperature 125 °C version.
2: $P2_6/AN_6$ and $P2_7/AN_7$ do not exist for the 32-pin version, so that Port P2 is a 6-bit I/O port.
3: $P3_5$ and $P3_6/INT_1$ do not exist for the 32-pin version, so that Port P3 is a 6-bit I/O port.

RENESAS

GROUP EXPANSION

Renesas plans to expand the 7542 group as follow:

Memory type

Support for Mask ROM version, Flash memory version, and Emulator MCU .

Memory size

Flash memory size .... 32 K + 4 K bytes
Mask ROM size .... 8 K to 16 K bytes
RAM size .... 384 to 1024 bytes

Package

32P4B .... 32-pin plastic molded SDIP
32P6U-A .... 0.8 mm-pitch 32-pin plastic molded LQFP
36P2R-A .... 0.8 mm-pitch 36-pin plastic molded SSOP
42S1M .... 42-pin shrink ceramic PIGGY BACK

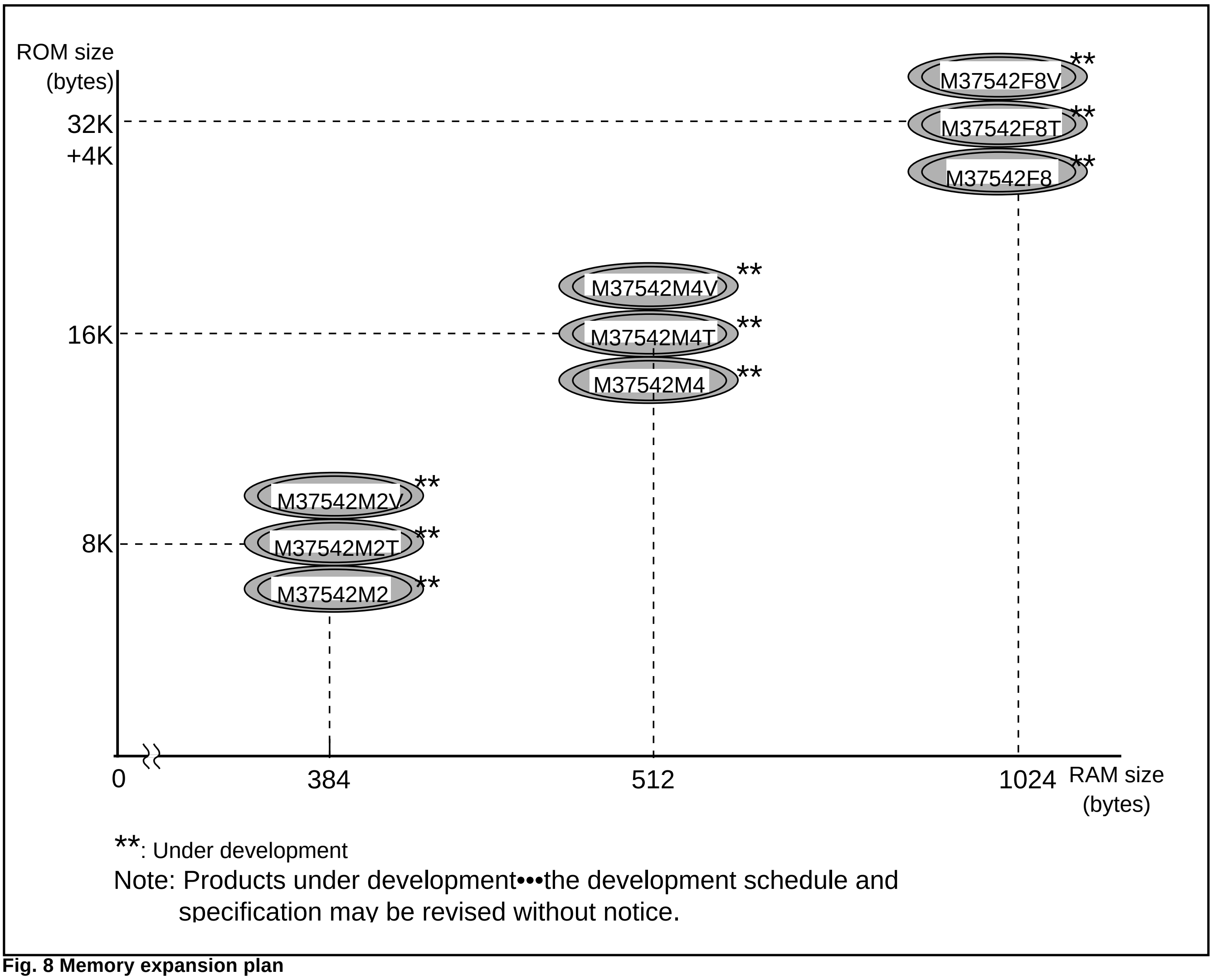


Fig. 8 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37542M2-XXXSP	8192 (8062)	384	32P4B	Mask ROM version
M37542M2-XXXFP			36P2R-A	Mask ROM version
M37542M2T-XXXFP				Mask ROM version (extended operating temperature version)
M37542M2V-XXXFP				Mask ROM version (extended operating temperature 125 °C version)
M37542M2-XXXGP			32P6U-A	Mask ROM version
M37542M2T-XXXGP				Mask ROM version (extended operating temperature version)
M37542M2V-XXXGP				Mask ROM version (extended operating temperature 125 °C version)
M37542M4-XXXSP	16384 (16254)	512	32P4B	Mask ROM version
M37542M4-XXXFP			36P2R-A	Mask ROM version
M37542M4T-XXXFP				Mask ROM version (extended operating temperature version)
M37542M4V-XXXFP				Mask ROM version (extended operating temperature 125 °C version)
M37542M4-XXXGP			32P6U-A	Mask ROM version
M37542M4T-XXXGP				Mask ROM version (extended operating temperature version)
M37542M4V-XXXGP				Mask ROM version (extended operating temperature 125 °C version)
M37542F8SP	32768 + 4096 (32638)	1024	32P4B	Flash memory version
M37542F8FP			36P2R-A	Flash memory version
M37542F8TFP				Flash memory version (extended operating temperature version)
M37542F8VFP				Flash memory version (extended operating temperature 125 °C version)
M37542F8GP			32P6U-A	Flash memory version
M37542F8TGP				Flash memory version (extended operating temperature version)
M37542F8VGP				Flash memory version (extended operating temperature 125 °C version)
M37542RSS	———	1024	42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.
Machine-resident 740 family instructions are as follows:
1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.
When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.
The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.
The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 9.

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

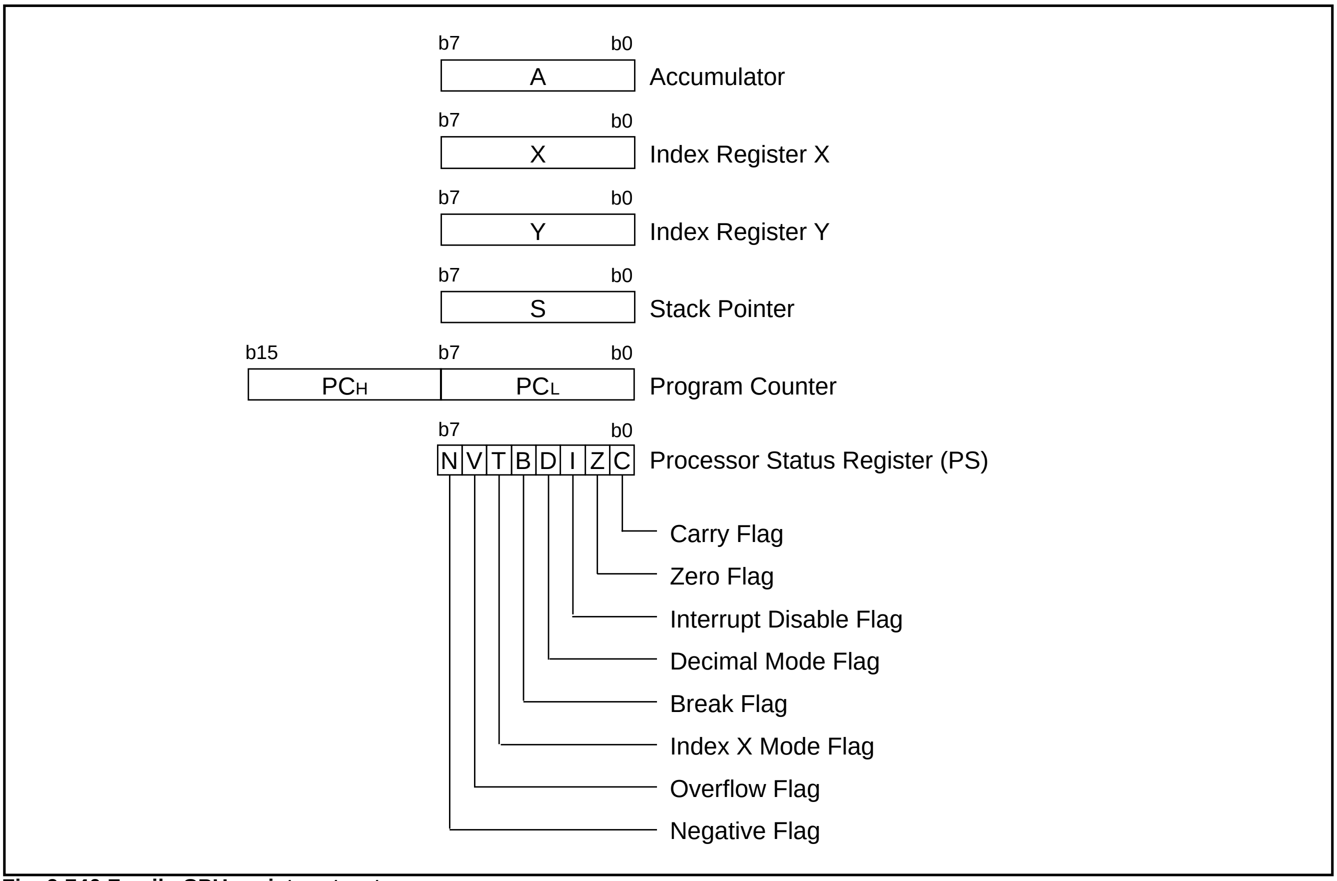


Fig. 9 740 Family CPU register structure

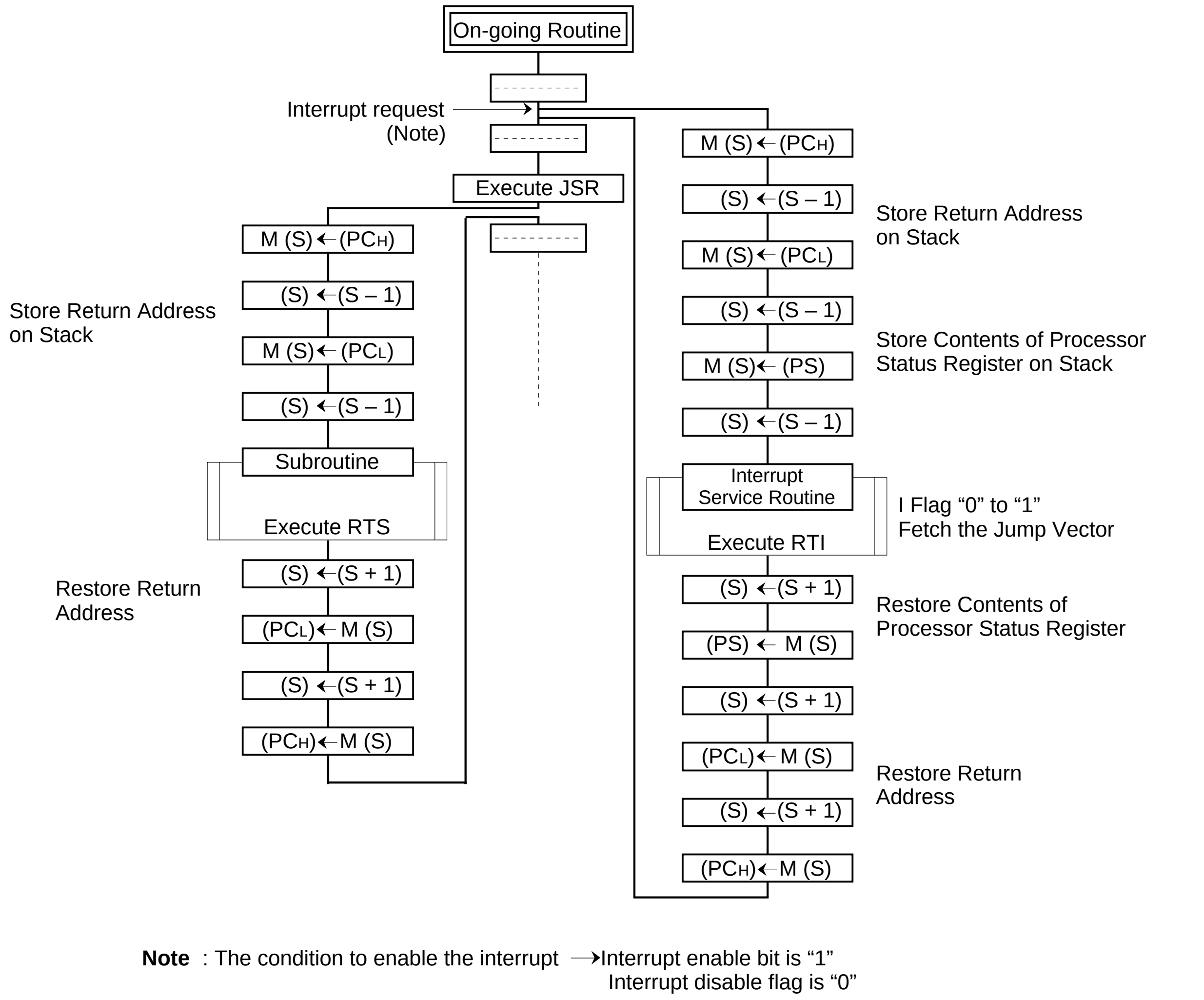


Fig. 10 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.
After reset, the Interrupt disable (I) flag is set to “1”, but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

(3) Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is “1”.
When an interrupt occurs, this flag is automatically set to “1” to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”. The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)
When the T flag is “0”, arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

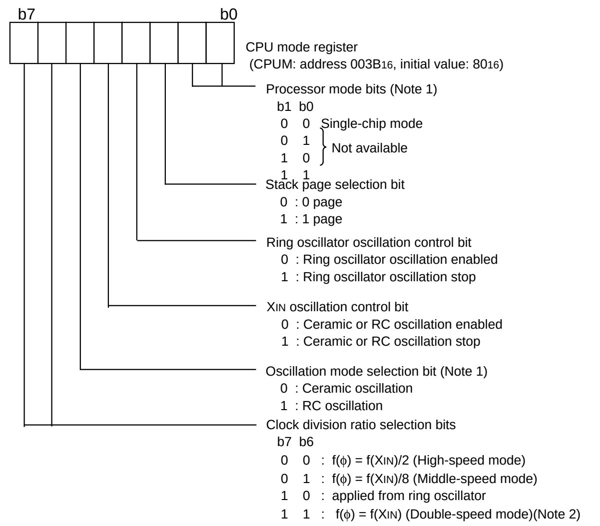
	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU mode register] CPUM

The CPU mode register contains the stack page selection bit, etc.. This register is allocated at address $003B_{16}$.

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.



Note 1: These bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to bits. However, by reset bits are initialized and can be rewritten, again.
(It is not disable to write any data to bits for emulator MCU "M37542RSS".)

2: These bits are used only when a ceramic oscillation is selected. Do not use these when an RC oscillation is selected.

Fig. 11 Structure of CPU mode register

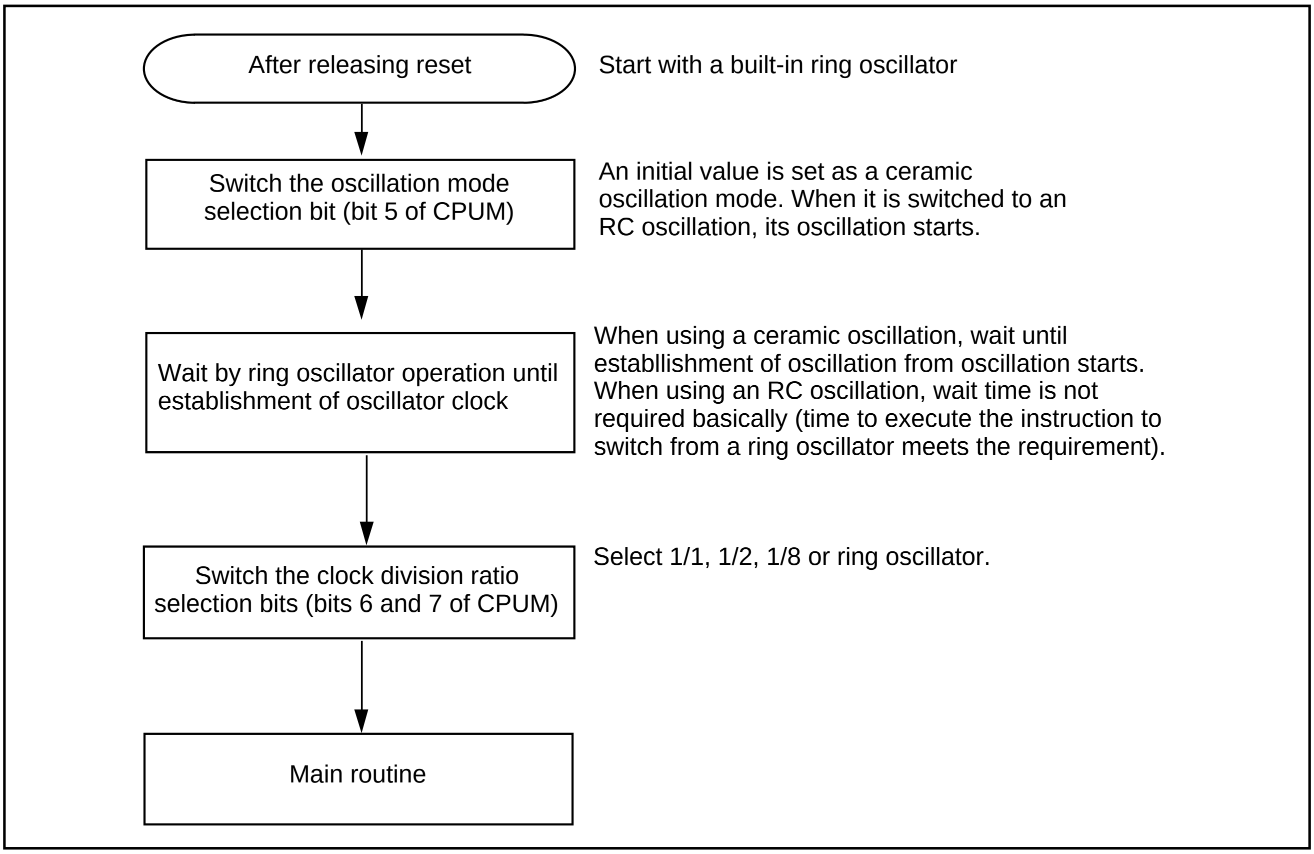


Fig. 12 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

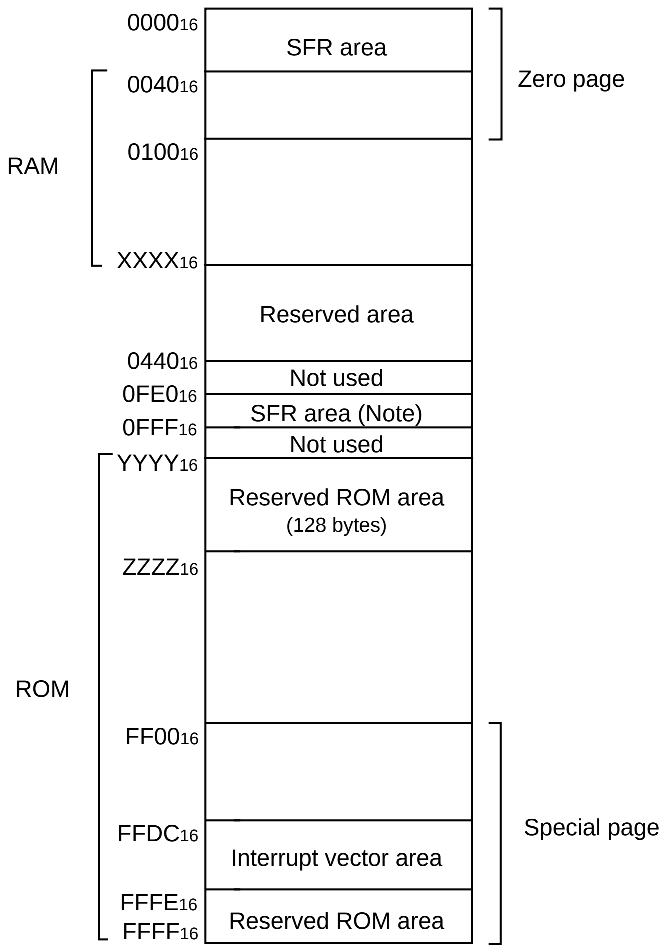
The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM capacity (bytes)	address $XXXX_{16}$
384	$01BF_{16}$
512	$023F_{16}$
1024	$043F_{16}$

ROM area

ROM capacity (bytes)	address $YYYY_{16}$	address $ZZZZ_{16}$
8192	$E000_{16}$	$E080_{16}$
16384	$C000_{16}$	$C080_{16}$
32768	8000_{16}	8080_{16}



Note: Only flash memory version has this SFR area.

Fig. 13 Memory map diagram

Address	Register	Address	Register
0000_{16}	Port P0 (P0)	0020_{16}	Capture mode register (CAPM)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Compare output mode register (CMOM)
0002_{16}	Port P1 (P1)	0022_{16}	Capture/compare status register (CCSR)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Compare interrupt source set register (CISR)
0004_{16}	Port P2 (P2)	0024_{16}	Timer A (low-order) (TAL)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer A (high-order) (TAH)
0006_{16}	Port P3 (P3)	0026_{16}	Timer B (low-order) (TBL)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer B (high-order) (TBH)
0008_{16}	Reserved	0028_{16}	Prescaler 1 (PRE1)
0009_{16}	Reserved	0029_{16}	Timer 1 (T1)
$000A_{16}$	Interrupt source set register (INTSET)	$002A_{16}$	Timer count source set register (TCSS)
$000B_{16}$	Interrupt source discrimination register (INTDIS)	$002B_{16}$	Timer X mode register (TXM)
$000C_{16}$	Capture register 0 (low-order) (CAP0L)	$002C_{16}$	Prescaler X (PREX)
$000D_{16}$	Capture register 0 (high-order) (CAP0H)	$002D_{16}$	Timer X (TX)
$000E_{16}$	Capture register 1 (low-order) (CAP1L)	$002E_{16}$	Transmit 2 / Receive 2 buffer register (TB2/RB2)
$000F_{16}$	Capture register 1 (high-order) (CAP1H)	$002F_{16}$	Serial I/O2 status register (SIO2STS)
0010_{16}	Compare register (low-order) (CMPL)	0030_{16}	Serial I/O2 control register (SIO2CON)
0011_{16}	Compare register (high-order) (CMPH)	0031_{16}	UART2 control register (UART2CON)
0012_{16}	Capture/compare register R/W pointer (CCRP)	0032_{16}	Baud rate generator 2 (BRG2)
0013_{16}	Capture software trigger register (CSTR)	0033_{16}	Reserved
0014_{16}	Compare register re-load register (CMPR)	0034_{16}	A-D control register (ADCON)
0015_{16}	Port P0P3 drive capacity control register (DCCR)	0035_{16}	A-D conversion register (low-order) (ADL)
0016_{16}	Pull-up control register (PULL)	0036_{16}	A-D conversion register (high-order) (ADH)
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	Ring oscillation division ratio selection register (RODR)
0018_{16}	Transmit 1 /Receive 1 buffer register (TB1/RB1)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART1 control register (UART1CON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator 1 (BRG1)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Timer A, B mode register (TABM)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	Capture/compare port register (CCPR)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Timer source selection register (TMSR)	$003F_{16}$	Interrupt control register 2 (ICON2)
		$0FE0_{16}$	Flash memory control register 0 (FMCR0) (Note 2)
		$0FE1_{16}$	Flash memory control register 1 (FMCR1) (Note 2)

Notes 1: Do not access to the SFR area including nothing.
2: Only flash memory version has this SFR area.

Fig. 14 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.
When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.
When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

Note: $P2_6$/AN_6, $P2_7$/AN_7, $P3_5$ and $P3_6$ do not exist for the 32-pin version. Accordingly, the following settings are required;
- Select $P3_3$ for the INT_1 function.
- Set direction registers of ports $P2_6$ and $P2_7$ to output.
- Set direction registers of ports $P3_5$ and $P3_6$ to output.

[Port P0P3 drive capacity control register] DCCR

By setting the Port P0P3 drive capacity control register (address 0015_{16}), the drive capacity of the N-channel output transistor for the port P0 and port P3 can be selected.

[Pull-up control register] PULL

By setting the pull-up control register (address 0016_{16}), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

[Port P1P3 control register] P1P3C

By setting the port P1P3 control register (address 0017_{16}), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ by program.

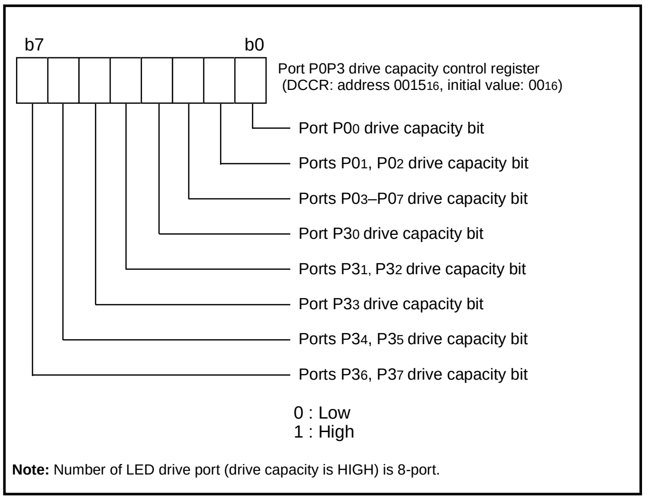


Fig. 15 Structure of port P0P3 drive capacity control register

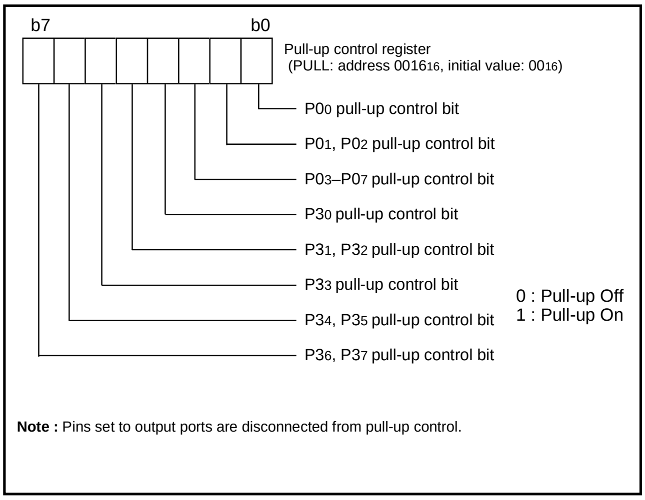


Fig. 16 Structure of pull-up control register

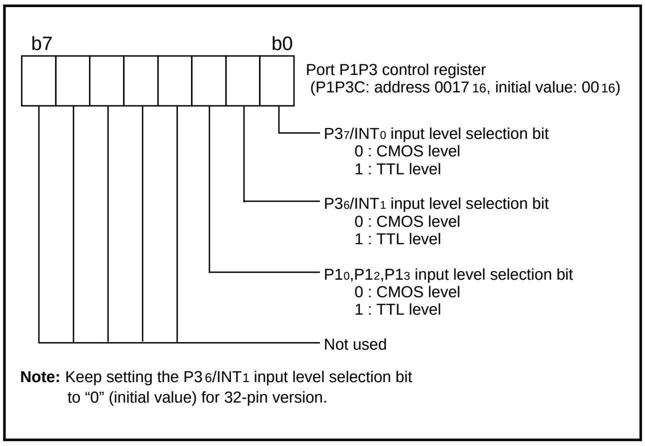


Fig. 17 Structure of port P1P3 control register

Table 5 I/O port function table

Pin	Name	I/O format	Non-port function	SFRs related each pin	Diagram No.
$P0_0$(LED$_{00}$)/CAP$_0$	I/O port P0	•CMOS compatible input level (**Note 1**) •CMOS 3-state output	• Capture function input • Key input interrupt	Capture/Compare port register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register	(1)
$P0_1$(LED$_{01}$)/CMP$_0$ $P0_2$(LED$_{02}$)/CMP$_1$			• Compare function output • Key input interrupt	Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register	(2)
$P0_3$(LED$_{03}$)/TX$_{OUT}$			• Timer X function output • Key input interrupt	Timer X mode register Pull-up control register Port P0P3 drive capacity control register	(3)
$P0_4$(LED$_{04}$)/RxD$_2$			• Serial I/O2 function input/output • Key input interrupt	Serial I/O2 control register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register	(4)
$P0_5$(LED$_{05}$)/TxD$_2$				Serial I/O2 control register Pull-up control register Port P0P3 drive capacity control register	(5)
$P0_6$(LED$_{06}$)/S$_{CLK2}$				Serial I/O2 control register Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register	(6)
$P0_7$(LED$_{07}$)/$\overline{S_{RDY2}}$				Serial I/O2 control register Pull-up control register Port P0P3 drive capacity control register	(7)
$P1_0$/RxD$_1$/CAP$_0$	I/O port P1		• Serial I/O1 function input • Capture function input	Serial I/O1 control register Capture/Compare port register Port P1P3 control register	(8)
$P1_1$/TxD$_1$			• Serial I/O1 function input/output	Serial I/O1 control register	(9)
$P1_2$/S$_{CLK1}$				Serial I/O1 control register Port P1P3 control register	(10)
$P1_3$/$\overline{S_{RDY1}}$				Serial I/O1 control register Port P1P3 control register	(11)
$P1_4$/CNTR$_0$			• Timer X function input/output • External interrupt input	Timer X mode register	(12)
$P2_0$/AN$_0$–$P2_7$/AN$_7$	I/O port P2 (**Note 2**)		• A-D conversion input	A-D control register	(13)
$P3_0$(LED$_{10}$)/CAP$_1$	I/O port P3 (**Note 3**)		• Capture function input	Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register	(14)
$P3_1$(LED$_{11}$)/CMP$_2$ $P3_2$(LED$_{12}$)/CMP$_3$			• Compare function output	Capture/Compare port register Pull-up control register Port P0P3 drive capacity control register	(15)
$P3_3$(LED$_{13}$)/INT$_1$			• External interrupt input	Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register	(16)
$P3_4$(LED$_{14}$) $P3_5$(LED$_{15}$)				Pull-up control register Port P0P3 drive capacity control register	(17)
$P3_6$(LED$_{16}$)/INT$_1$ $P3_7$(LED$_{17}$)/INT$_0$			• External interrupt input	Interrupt edge selection register Pull-up control register Port P0P3 drive capacity control register Port P1P3 control register	(18) (19)

Notes 1: Ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ are CMOS/TTL level.
2: $P2_6$/AN$_6$ and $P2_7$/AN$_7$ do not exist for the 32-pin version.
3: $P3_5$ and $P3_6$/INT$_1$ do not exist for the 32-pin version.

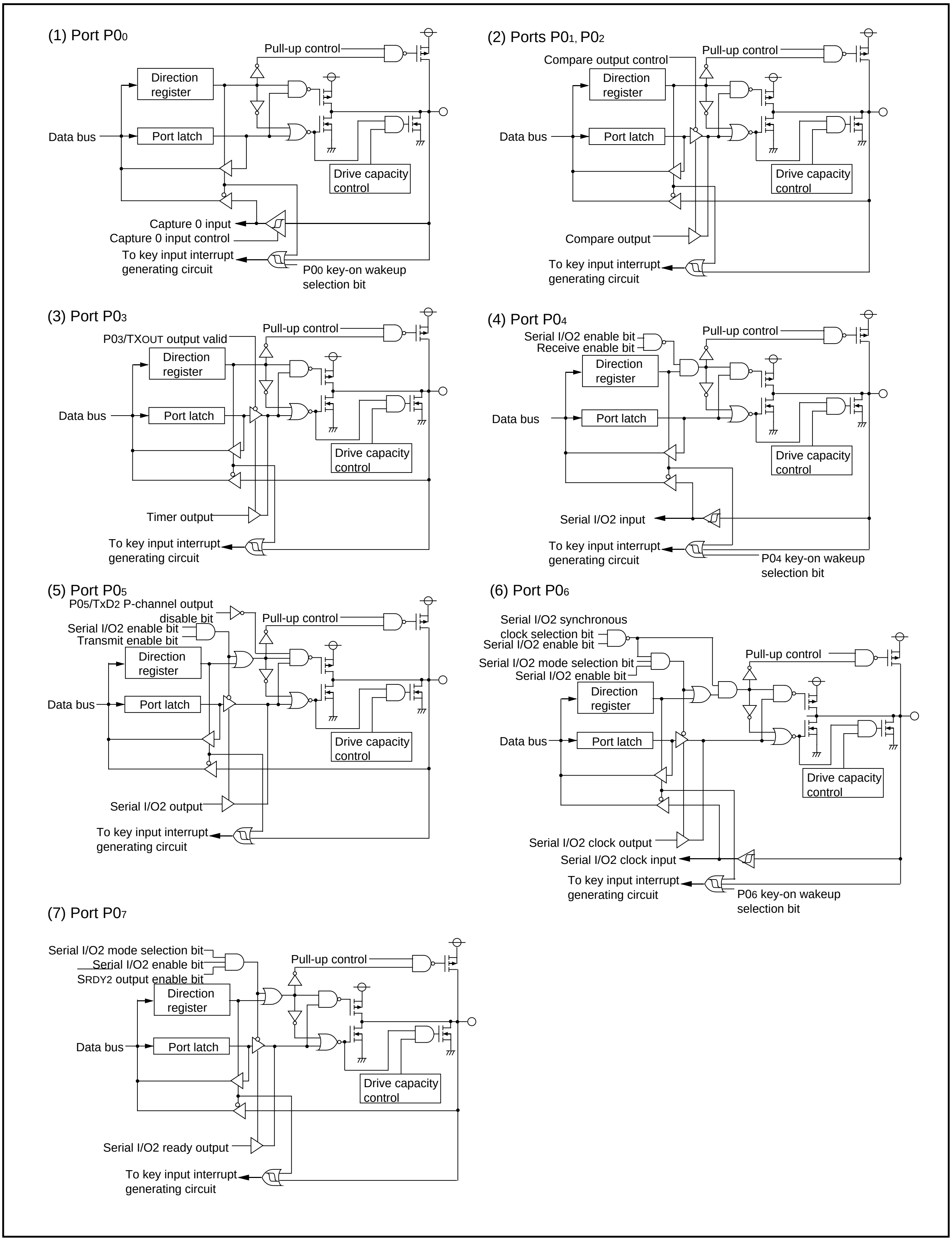
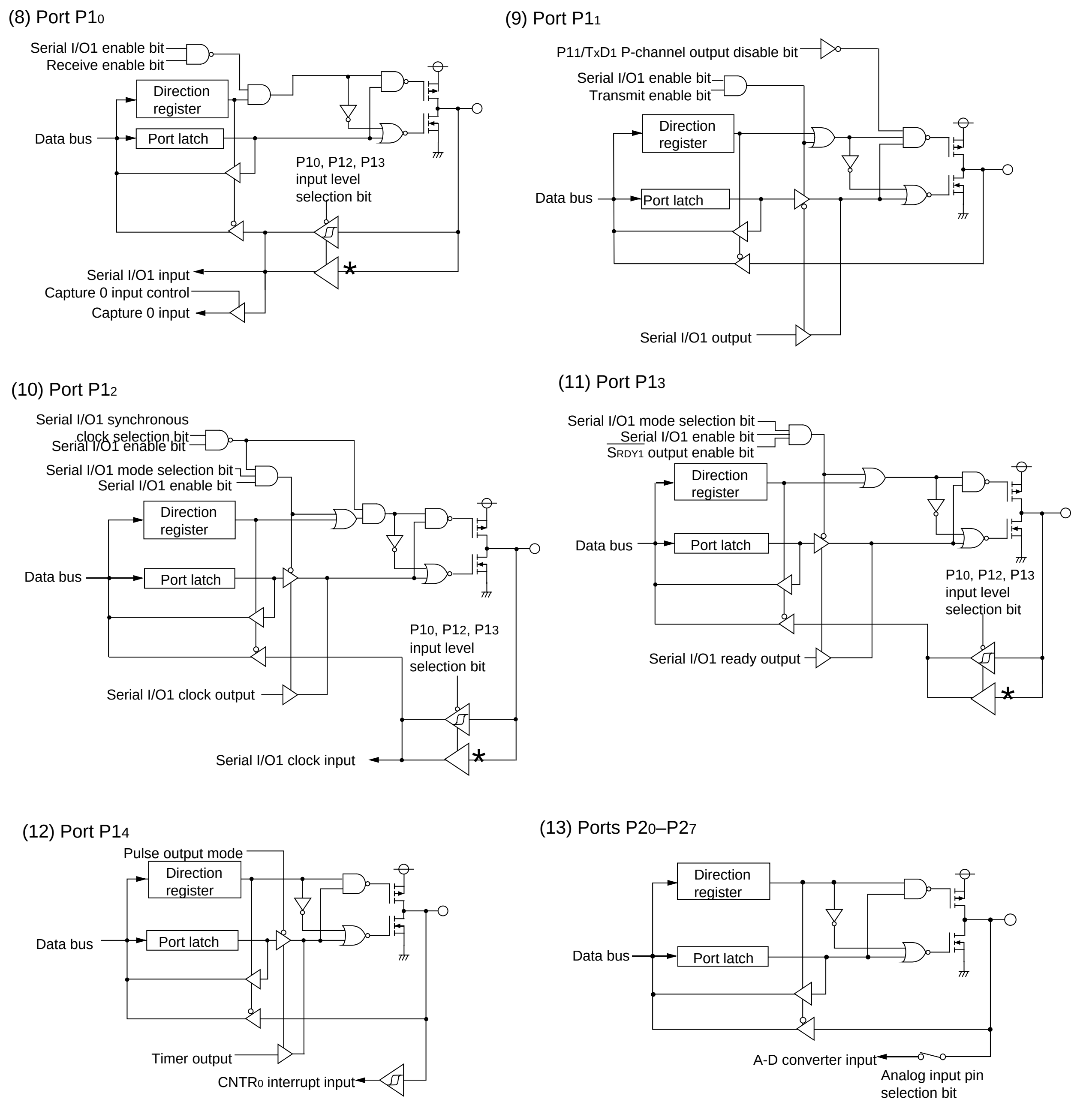
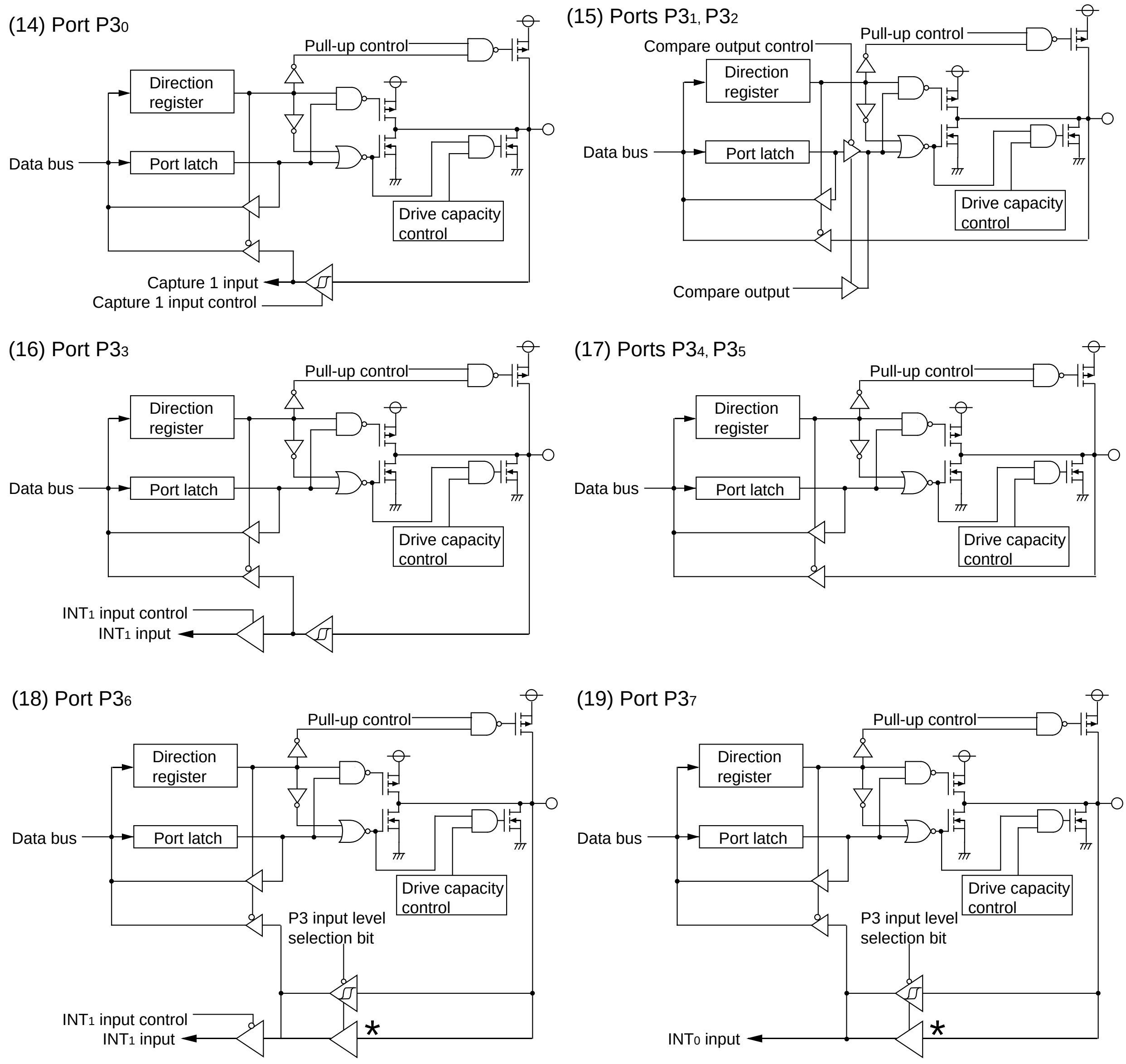


Fig. 18 Block diagram of ports (1)



* P10, P12, P13, P36, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 19 Block diagram of ports (2)



* $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 20 Block diagram of ports (3)

Interrupts

Interrupts occur by 18 different sources : 6 external sources, 11 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to “1” and the interrupt disable flag is set to “0”, an interrupt is accepted.
The interrupt request bit can be cleared by program but not be set. The interrupt enable bit can be set and cleared by program.
The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.
When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:
1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

[Interrupt source set register] INTSET

When two interrupt sources are assigned to the same interrupt vector, the valid/invalid of each interrupt is set by this register.
When both two interrupt sources are set to be valid, which interrupt request occurs is confirmed by the next interrupt source discrimination register.

[Interrupt source discrimination register] INTDIS

When two interrupt sources are assigned to the same interrupt vector, which interrupt source occurs is confirmed by this register.
If an interrupt request of a key-on wakeup, UART1 bus collision detection, A-D conversion or timer 1 occurs, an interrupt discrimination bit is set to “1” regardless of valid/invalid state by the interrupt source set register.
However, when the interrupt valid bit of an interrupt source set register is “0” (invalid), the interrupt request bit of an interrupt control register is not set to “1.”
Moreover, since an interrupt discrimination bit is not automatically cleared to “0” by interrupt, please clear it by program.
An interrupt discrimination bit can be cleared to “0” by program but not be set to “1.”

[Interrupt edge selection register] INTEDGE

The valid edge of external interrupt INT_0 and INT_1 can be selected by the interrupt edge selection bit, respectively.
For the external interrupt INT_1, the external input pin $P3_3/INT_1$ or $P3_6/INT_1$ can be selected by the INT_1 input port selection bit.
However, since there is no $P3_6/INT_1$ pin in the 32-pin version, select $P3_3/INT_1$ pin. By the key-on wakeup selection bit, enable/disable of a key-on wakeup of $P0_0$, $P0_4$, and $P0_6$ pins can be selected, respectively.

■ Notes on use

(1) When setting the followings, the interrupt request bit may be set to “1”.
•When switching external interrupt active edge
Related register:
Interrupt edge selection register (address $003A_{16}$)
Timer X mode register (address $002B_{16}$)
Capture mode register (address 0020_{16})

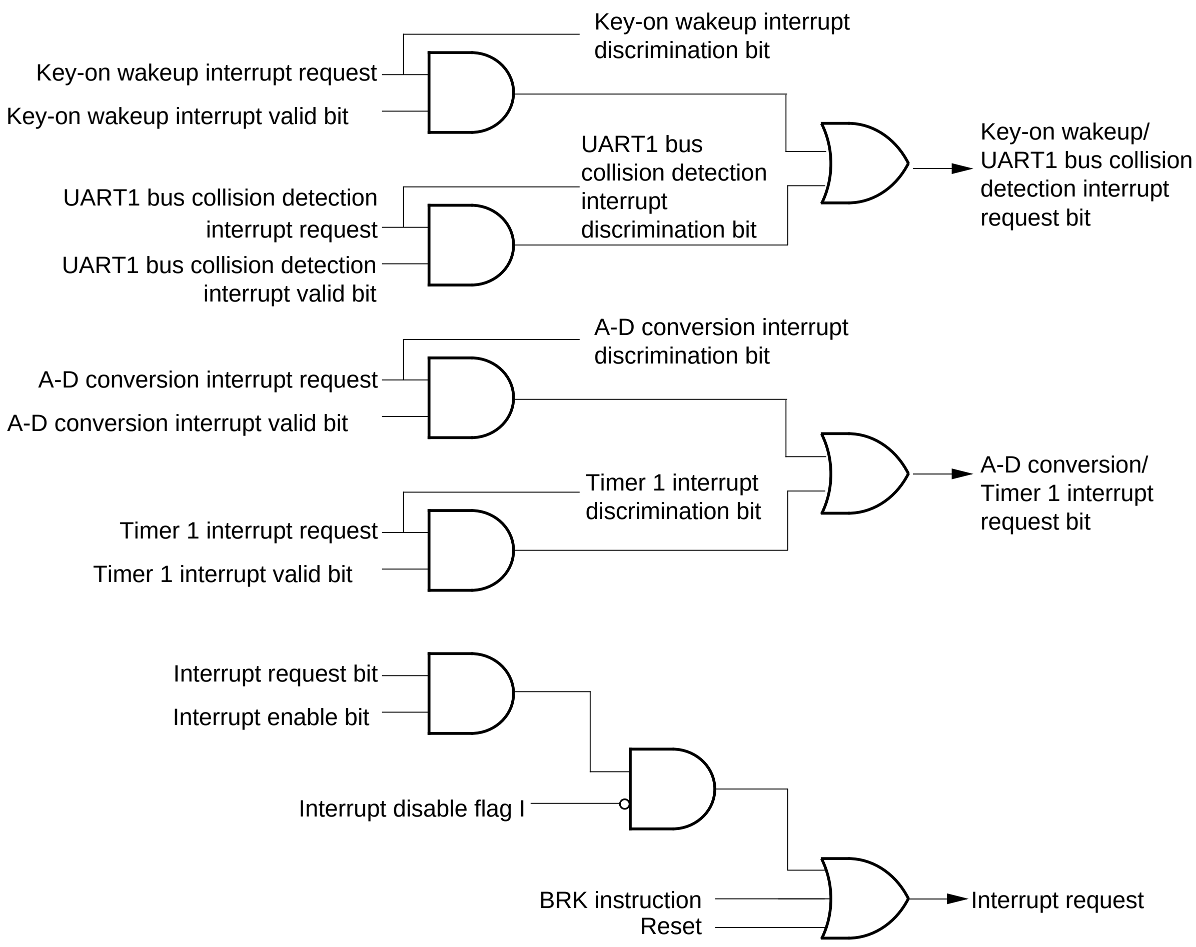
When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
① Set the corresponding interrupt enable bit to “0” (disabled).
② Set the interrupt edge select bit (active edge switch bit, trigger mode bit).
③ Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to “1” (enabled).

(2) Use a LDM instruction to clear an interrupt discrimination bit.
LDM #$0n, $0Bn
Set the following values to “n”
“0”: an interrupt discrimination bit to clear
“1”: other interrupt discrimination bits
Ex.) When a key-on wakeup interrupt discrimination bit is cleared;
LDM #00001110B and $0B.

Table 6 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Serial I/O1 receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of serial I/O1 transmit shift or when transmit buffer is empty	Valid only when serial I/O1 is selected
Serial I/O2 receive	4	$FFF7_{16}$	$FFF6_{16}$	At completion of serial I/O2 data receive	Valid only when serial I/O2 is selected
Serial I/O2 transmit	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O2 transmit shift or when transmit buffer is empty	Valid only when serial I/O2 is selected
INT_0	6	$FFF3_{16}$	$FFF2_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	7	$FFF1_{16}$	$FFF0_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Key-on wake-up/ UART1 bus collision detection (Note 3)	8	$FFEF_{16}$	$FFEE_{16}$	At falling of conjunction of input logical level for port P0 (at input) At detection of UART1 bus collision detection	External interrupt (valid at falling, when key-on wakeup interrupt is enabled) When UART1 bus collision detection interrupt is enabled.
$CNTR_0$	9	$FFED_{16}$	$FFEC_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
Capture 0	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of Capture 0 input	External interrupt (active edge selectable)
Capture 1	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of Capture 1 input	External interrupt (active edge selectable)
Compare	12	$FFE7_{16}$	$FFE6_{16}$	At compare matched	Compare interrupt source is selected.
Timer X	13	$FFE5_{16}$	$FFE4_{16}$	At timer X underflow	
Timer A	14	$FFE3_{16}$	$FFE2_{16}$	At timer A underflow	
Timer B	15	$FFE1_{16}$	$FFE0_{16}$	At timer B underflow	
A-D conversion/ Timer 1 (Note 4)	16	$FFDF_{16}$	$FFDE_{16}$	At completion of A-D conversion At timer 1 underflow	When A-D conversion interrupt is enabled. STP release timer underflow (When Timer 1 interrupt is enabled)
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.
3: Key-on wakeup interrupt and UART1 bus collision detection interrupt can be enabled by setting of interrupt source set register. The occurrence of these interrupts are discriminated by interrupt source discrimination register.
4: A-D conversion interrupt and Timer 1 interrupt can be enabled by setting of interrupt source set register. The occurrence of these interrupts are discriminated by interrupt source discrimination register.



Note: For key-on wakeup, UART1 bus collision detection, A-D conversion and Timer 1 interrupt, even if interrupt valid bit ($000A_{16}$) is set "0: Invalid", interrupt discrimination bit ($000B_{16}$) is set to "1: interrupt occurs" when corresponding interrupt request occurs. But corresponding interrupt request bit ($003C_{16}$, $003D_{16}$) is not set to "1".

Fig. 21 Interrupt control

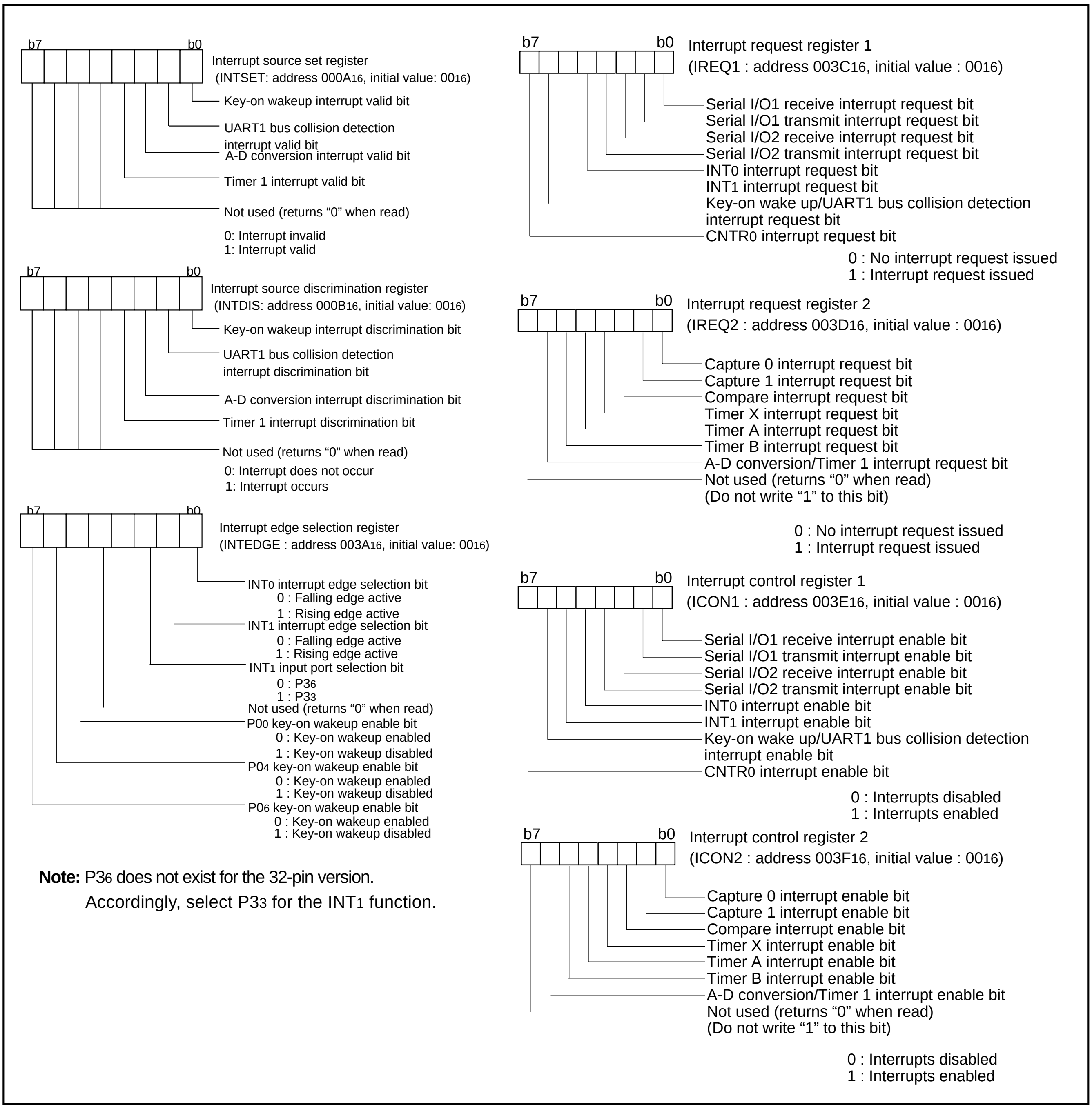


Fig. 22 Structure of Interrupt-related registers

Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying “L” level to any pin of port P0 that has been set to input mode.
In other words, it is generated when the AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 21, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P0₀ to P0₃ as input ports.

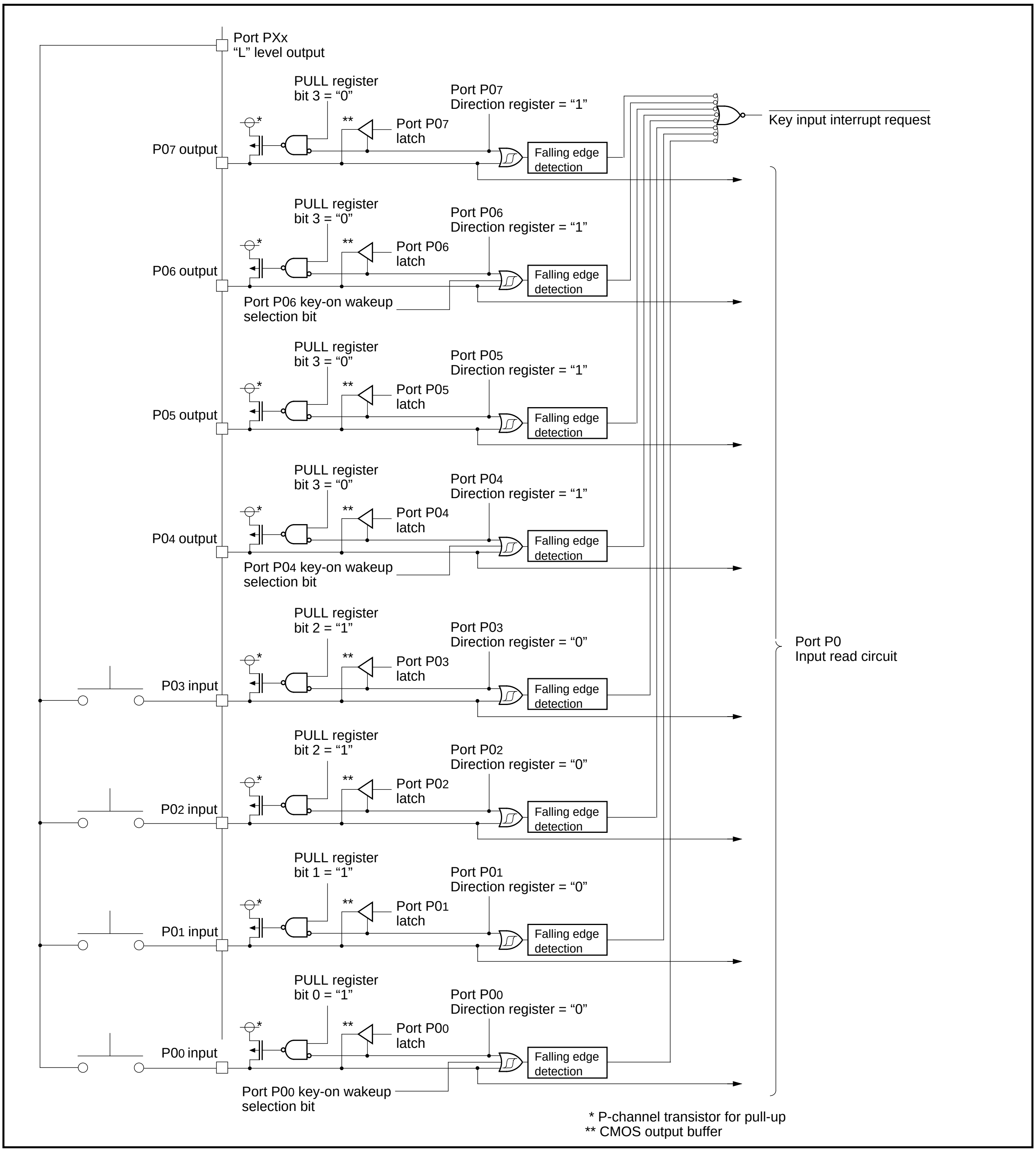


Fig. 23 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7542 Group has 4 timers: timer 1, timer X, timer A and timer B.
The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.
All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

• Frequency divider for timer
According to the clock division selection bits (b7 and b6) of CPU mode register ($003B_{16}$), the count source of frequency divider is set as follows;
b7b6 = "00"(high-speed), "01"(middle-speed), "11"(double-speed): X_{IN}
b7b6 = "10"(Ring oscillator): Ring oscillator

●Timer 1

Timer 1 is an 8-bit timer and counts the prescaler output.
When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".
Prescaler 1 is an 8-bit prescaler and counts the signal which is the oscillation frequency divided by 16.
Prescaler 1 and Timer 1 have the prescaler 1 latch and the timer 1 latch to retain the reload value, respectively. The value of prescaler 1 latch is set to Prescaler 1 when Prescaler 1 underflows.The value of timer 1 latch is set to Timer 1 when Timer 1 underflows.
When writing to Prescaler 1 (PRE1) is executed, the value is written to both the prescaler 1 latch and Prescaler 1.
When writing to Timer 1 (T1) is executed, the value is written to both the timer 1 latch and Timer 1.
When reading from Prescaler 1 (PRE1) and Timer 1 (T1) is executed, each count value is read out.
Timer 1 always operates in the timer mode.
Prescaler 1 counts the signal which is the oscillation frequency divided by 16. Each time the count clock is input, the contents of Prescaler 1 is decremented by 1. When the contents of Prescaler 1 reach "00_{16}", an underflow occurs at the next count clock, and the prescaler 1 latch is reloaded into Prescaler 1 and count continues. The division ratio of Prescaler 1 is 1/(n+1) provided that the value of Prescaler 1 is n.
The contents of Timer 1 is decremented by 1 each time the underflow signal of Prescaler 1 is input. When the contents of Timer 1 reach "00_{16}", an underflow occurs at the next count clock, and the timer 1 latch is reloaded into Timer 1 and count continues. The division ratio of Timer 1 is 1/(m+1) provided that the value of Timer 1 is m. Accordingly, the division ratio of Prescaler 1 and Timer 1 is $1/((n+1)\times(m+1))$ provided that the value of Prescaler 1 is n and the value of Timer 1 is m.
Timer 1 cannot stop counting by software.

●Timer X

Timer X is an 8-bit timer and counts the prescaler X output.
When Timer X underflows, the timer X interrupt request bit is set to "1".
Prescaler X is an 8-bit prescaler and counts the signal selected by the timer X count source selection bit.
Prescaler X and Timer X have the prescaler X latch and the timer X latch to retain the reload value, respectively. The value of prescaler X latch is set to Prescaler X when Prescaler X underflows.The value of timer X latch is set to Timer X when Timer X underflows.
When writing to Prescaler X (PREX) is executed, the value is written to both the prescaler X latch and Prescaler X.
When writing to Timer X (TX) is executed, the value is written to both the timer X latch and Timer X.
When reading from Prescaler X (PREX) and Timer X (TX) is executed, each count value is read out.

Timer X can can be selected in one of 4 operating modes by setting the timer X operating mode bits of the timer X mode register.

(1) Timer mode
Prescaler X counts the count source selected by the timer X count source selection bits. Each time the count clock is input, the contents of Prescaler X is decremented by 1. When the contents of Prescaler X reach "00_{16}", an underflow occurs at the next count clock, and the prescaler X latch is reloaded into Prescaler X and count continues. The division ratio of Prescaler X is 1/(n+1) provided that the value of Prescaler X is n.
The contents of Timer X is decremented by 1 each time the underflow signal of Prescaler X is input. When the contents of Timer X reach "00_{16}", an underflow occurs at the next count clock, and the timer X latch is reloaded into Timer X and count continues. The division ratio of Timer X is 1/(m+1) provided that the value of Timer X is m. Accordingly, the division ratio of Prescaler X and Timer X is $1/((n+1)\times(m+1))$ provided that the value of Prescaler X is n and the value of Timer X is m.

(2) Pulse output mode
In the pulse output mode, the waveform whose polarity is inverted each time timer X underflows is output from the $CNTR_0$ pin.
The output level of $CNTR_0$ pin can be selected by the $CNTR_0$ active edge switch bit. When the $CNTR_0$ active edge switch bit is "0", the output of $CNTR_0$ pin is started at "H" level. When this bit is "1", the output is started at "L" level.
Also, the inverted waveform of pulse output from $CNTR_0$ pin can be output from TX_{OUT} pin by setting "1" to the $P0_3/TX_{OUT}$ output valid bit.
When using a timer in this mode, set the port $P1_4$ and $P0_3$ direction registers to output mode.

(3) Event counter mode
The timer A counts signals input from the $P1_4/CNTR_0$ pin.
Except for this, the operation in event counter mode is the same as in timer mode.
The active edge of $CNTR_0$ pin input signal can be selected from rising or falling by the $CNTR_0$ active edge switch bit .

(4) Pulse width measurement mode

In the pulse width measurement mode, the pulse width of the signal input to P14/CNTR0 pin is measured.
The operation of Timer X can be controlled by the level of the signal input from the CNTR0 pin.
When the CNTR0 active edge switch bit is “0”, the signal selected by the timer X count source selection bit is counted while the input signal level of CNTR0 pin is “H”. The count is stopped while the pin is “L”. Also, when the CNTR0 active edge switch bit is “1”, the signal selected by the timer X count source selection bit is counted while the input signal level of CNTR0 pin is “L”. The count is stopped while the pin is “H”.

Timer X can stop counting by setting “1” to the timer X count stop bit in any mode.
Also, when Timer X underflows, the timer X interrupt request bit is set to “1”.

Note on Timer X is described below;

■ **Note on Timer X**

(1) CNTR0 interrupt active edge selection-1
CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.
When this bit is “0”, the CNTR0 interrupt request bit is set to “1” at the falling edge of CNTR0 pin input signal. When this bit is “1”, the CNTR0 interrupt request bit is set to “1” at the rising edge of CNTR0 pin input signal.

(2) CNTR0 interrupt active edge selection-2
According to the setting value of CNTR0 active edge switch bit, the interrupt request bit may be set to “1”.
When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
① Set the corresponding interrupt enable bit to “0” (disabled).
② Set the active edge switch bit.
③ Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to “1” (enabled).

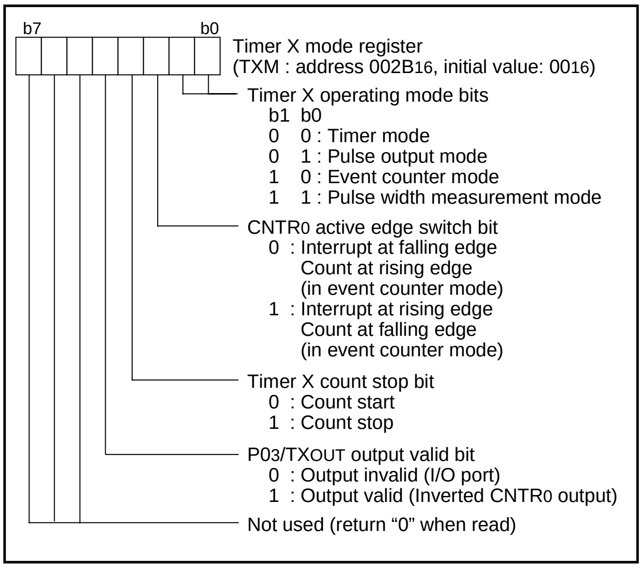


Fig. 24 Structure of timer X mode register

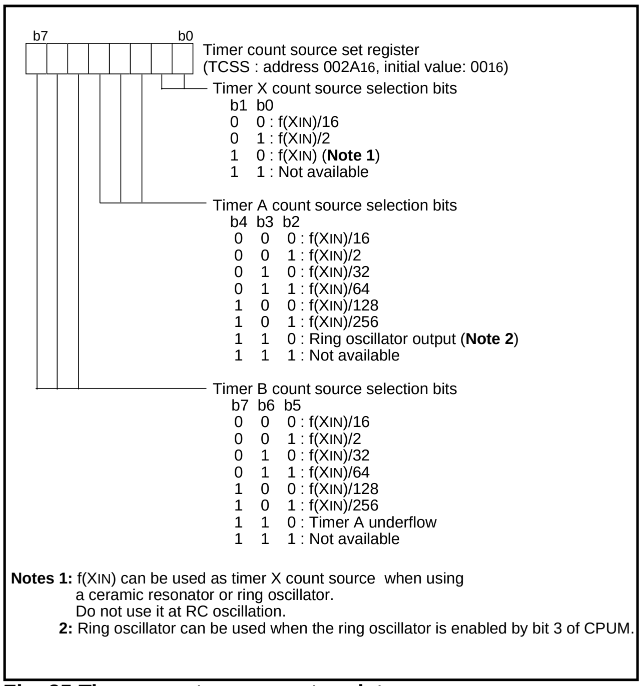


Fig. 25 Timer count source set register

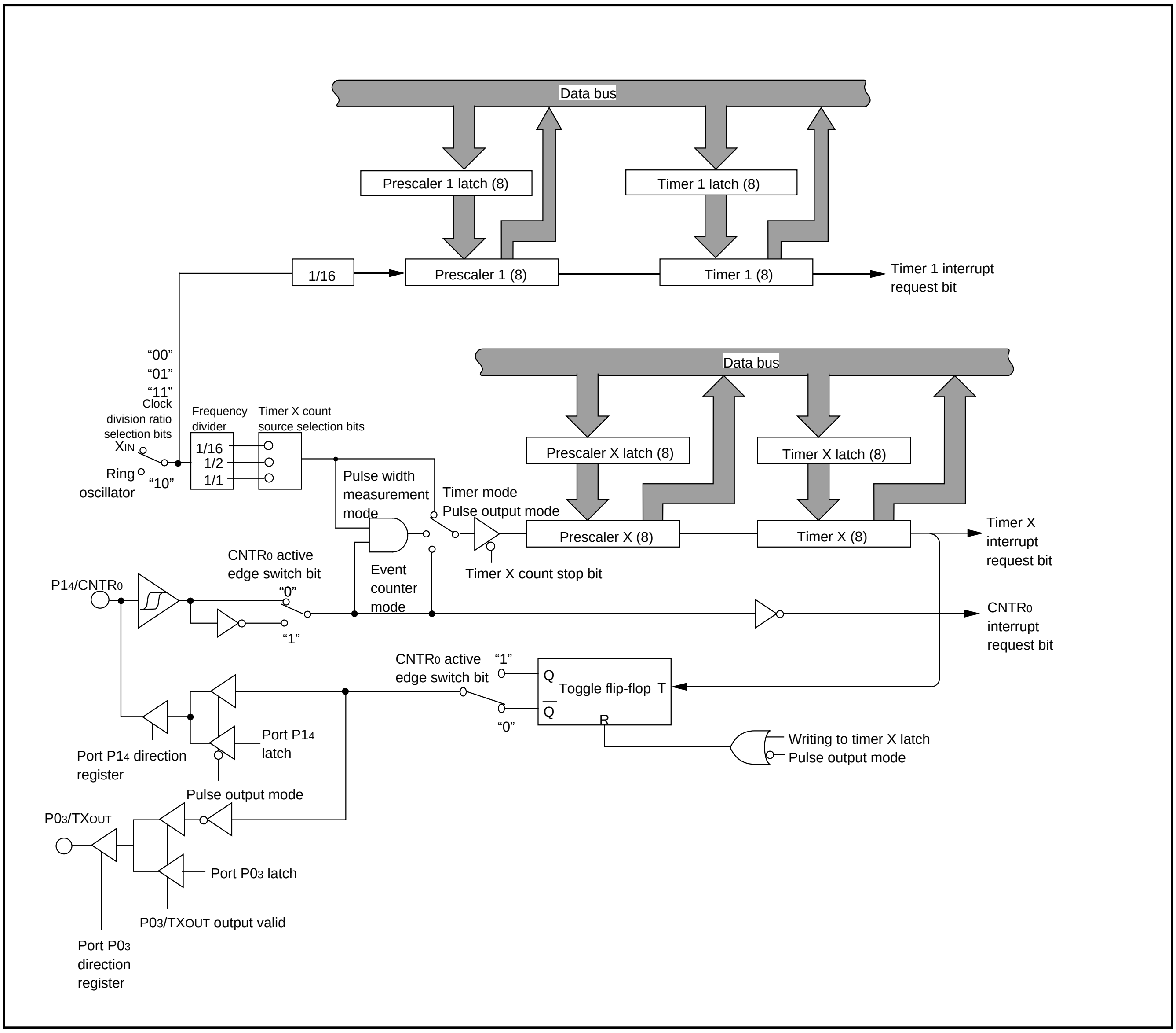


Fig. 26 Block diagram of timer 1 and timer X

●Timer A,B

Timer A and Timer B are 16-bit timers and counts the signal which is the oscillation frequency selected by setting of the timer count source set register (TCSS). Timer A and Timer B have the same function except of the count source clock selection.

The count source clock of Timer A is selected from among 1/2,1/16, 1/32, 1/64, 1/128, 1/256 of f(XIN) clock and ring oscillator clock.
The count source clock of Timer B is selected from among 1/2, 1/16, 1/32, 1/64, 1/128, 1/256 of f(XIN) clock and Timer A underflow.

Timer A (B) consists of the low-order of Timer A: TAL (Timer B: TBL) and the high-order of Timer A: TAH (Timer B: TBH). Timer A (B) is decremented by 1 when each time of the count clock is input. When the contents of Timer A (B) reach "0000_{16}", an underflow occurs at the next count clock, and the timer latch is reloaded into timer. When Timer A (B) underflows, the Timer A (B) interrupt request bit is set to "1".
Timer A (B) has the Timer A (B) latch to retain the load value. The value of timer A (B) latch is set to Timer A (B) at the timing of Timer A (B) underflow. The division ratio of Timer A (B) is 1/(n+1) provided that the value of Timer A (B) is n.

When writing to both the low-order of Timer A (B) and the high order of Timer A (B) is executed, writing to "latch only" or "latch and timer" can be selected by the setting value of the timer A (B) write control bit.
When reading from Timer A (B) register is executed, the count value of Timer A (B) is read out.

Be sure to write to/read out the low-order of Timer A (B) and the high-order of Timer A (B) in the following order;
• Read
Read the high-order of Timer A (B) first, and the low-order of Timer A (B) next and be sure to read both high-order and low-order.
• Write
Write to the low-order of Timer A (B) first, and the high-order of Timer A (B) next and be sure to write both low-order and high order.

Timer A and Timer B can be used for the timing timer of Input capture and Output compare function.

■ Notes on Timer A, B

(1) Setting of timer value
When "1: Write to only latch" is set to the timer A (B) write control bit, written data to timer register is set to only latch even if timer is stopped. Accordingly, in order to set the initial value for timer when it is stopped, set "0: Write to latch and timer simultaneously" to timer A (B) write control bit.

(2) Read/write of timer A
Stop timer A to read/write its data when the system is in the following state;
• CPU operation clock source: XIN oscillation
• Timer A count source: Ring oscillator output

(3) Read/write of timer B
Stop timer B to read/write its data when the system is in the following state;
• CPU operation clock source: XIN oscillation
• Timer B count source: Timer A underflow
• Timer A count source: Ring oscillator output

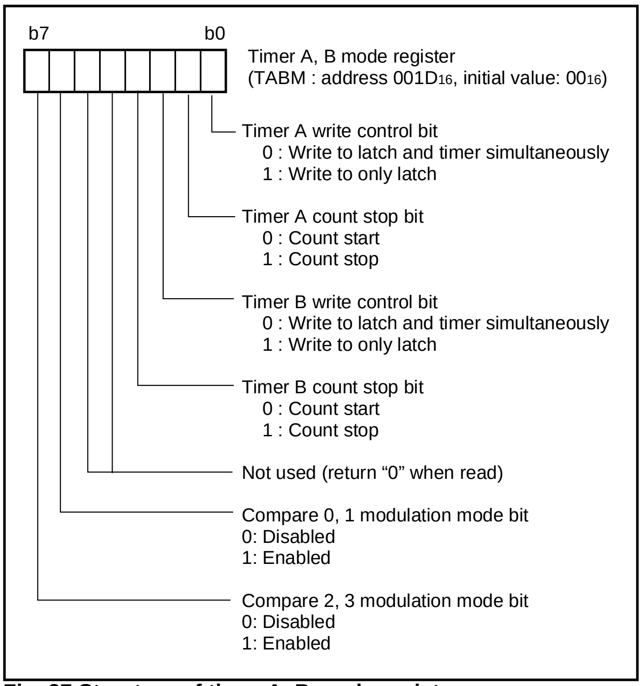


Fig. 27 Structure of timer A, B mode register

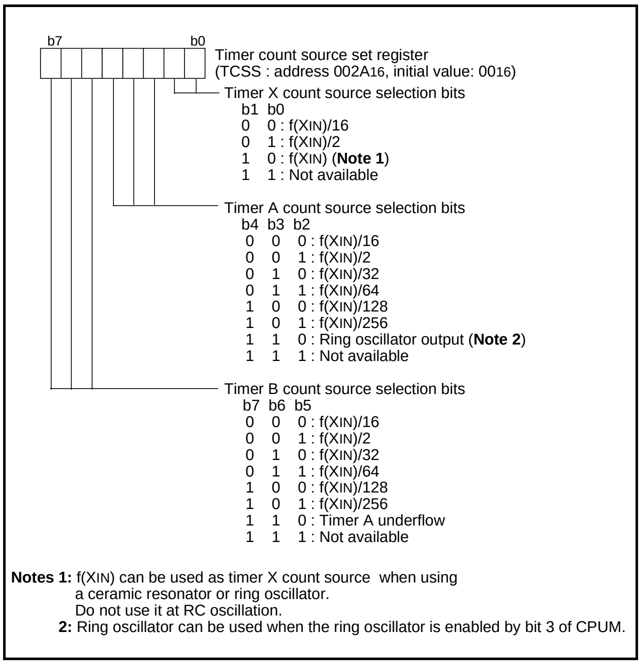


Fig. 28 Timer count source set register

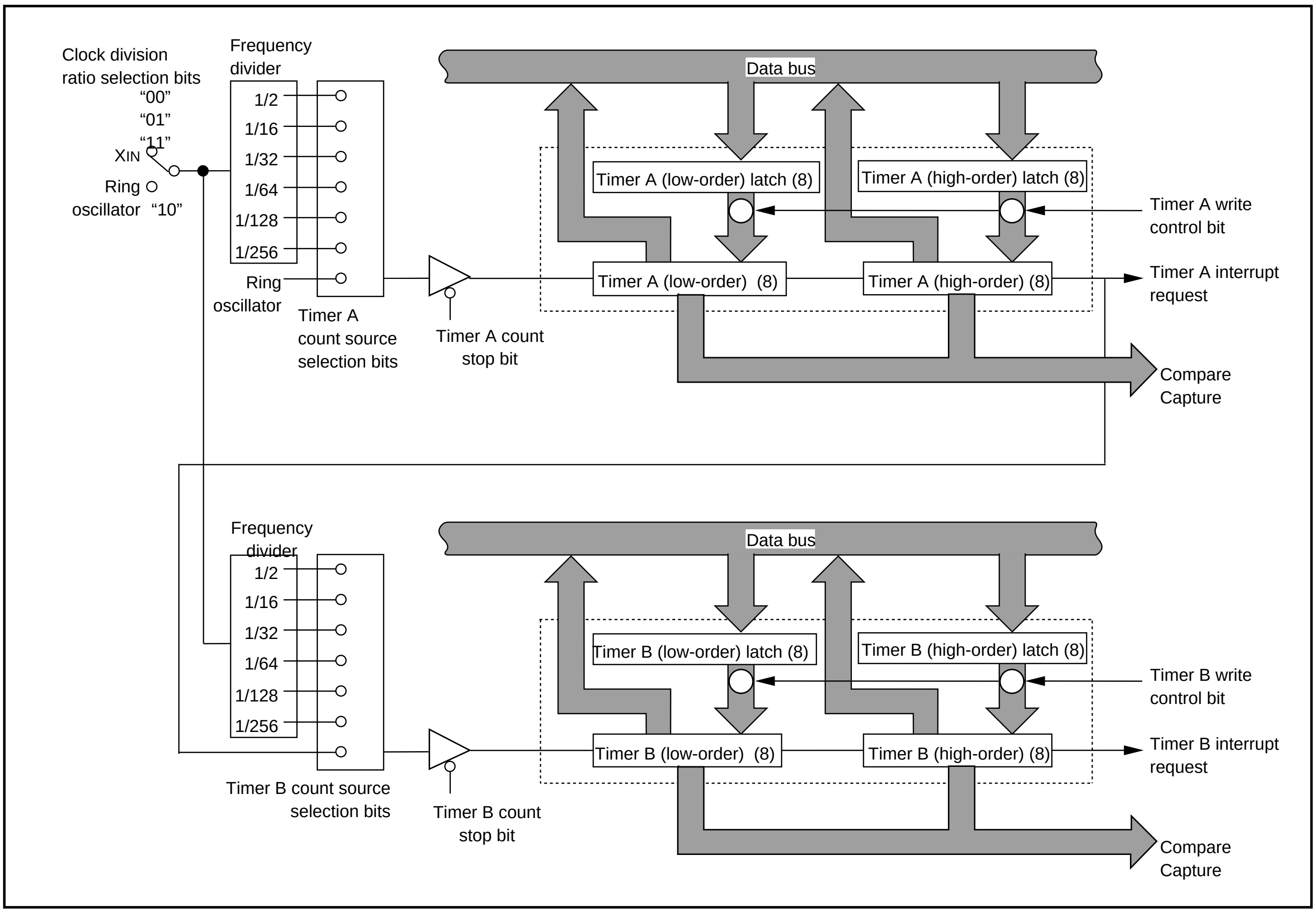


Fig. 29 Block diagram of timer A and timer B

Output compare

7542 group has 4-output compare channels. Each channel (0 to 3) has the same function and can be used to output waveform by using count value of either Timer A or Timer B.
The source timer for each channel is selected by setting value of the compare x (x = 0, 1, 2, 3) timer source bit. Timer A and Timer B can be selected for the source timer to each channel, respectively.

To use each compare channel, set "1" to the compare x output port bit and set the port direction register corresponding to compare channel to output mode.

The compare value for each channel is set to the compare register (low-order) and compare register (high-order).
Writing to the register for each channel is controlled by setting value of compare register write pointer. Writing to each register is in the following order;

1. Set the value of corresponded output compare channel to the compare register write pointer.
2. Write a value to the compare register (low-order) and compare register (high-order).
3. Set "1" to the compare latch y (y = 00, 01, 10, 11, 20, 21, 30, 31) re-load bit.
   When "1" is set to the compare latch y re-load bit, the value set to the compare register is loaded to compare latch when the next timer underflow.

When count value of timer and setting value of compare latch is matched, compare output trigger occurs.
When "1: Enabled" is set to the compare trigger x enable bit, the output waveform from port is inverted by compare trigger.
When "0: Disabled" is set to the compare trigger x enable bit, the output waveform is not inverted, so port output can be fixed to "H" or "L".

When "0: Positive" is set to the compare x output level latch, the compare output waveform is turned to "H level" at compare latch x0's match and turned to "L level" at compare latch x1's match.
When "1 :Negative" is set to the compare x output level latch, the compare output waveform is turned to "L level" at compare latch x0's match and turned to "H level" at compare latch x1's match.
The compare output level of each channel can be confirmed by reading the compare x output status bit.

Compare output interrupt is available when match of each compare channel and timer count value. The interrupt request from each channel can be disabled or enabled by setting value of compare latch y interrupt source bit.

Compare 0,1 (2,3) modulation mode

In compare modulation mode, modulation waveform can be generated by using compare channel 0 and 1, or compare channel 2 and 3.
To use this mode,

- Set "1: Enabled" to the compare 0,1 (2, 3) modulation mode bit.
- Set Timer A underflow for Timer B count source.
- Set Timer A for the timer source of compare channel 0 (2).
- Set Timer B for the timer source of compare channel 1 (3).

In this mode, AND waveform of compare 0 (1) and compare 2 (3) is generated from Port $P0_1$ and $P3_1$, respectively. Accordingly, in order to use this mode, set "1" to the compare 0 output port bit or compare 2 output port bit.

■ Notes on Output Compare

- When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
- Do not write the same data to both of compare latch x0 and x1.
- When setting value of the compare latch is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to "L" or "H" level.
  However, when setting value of another compare latch is smaller than timer setting value, this compare match signal is generated. Accordingly, compare match interrupt occurs.
- When the compare x trigger enable bit is cleared to "0" (disabled), the match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to "L" or "H" level.
  However, in this case, the compare match signal is generated. Accordingly, compare match interrupt occurs.

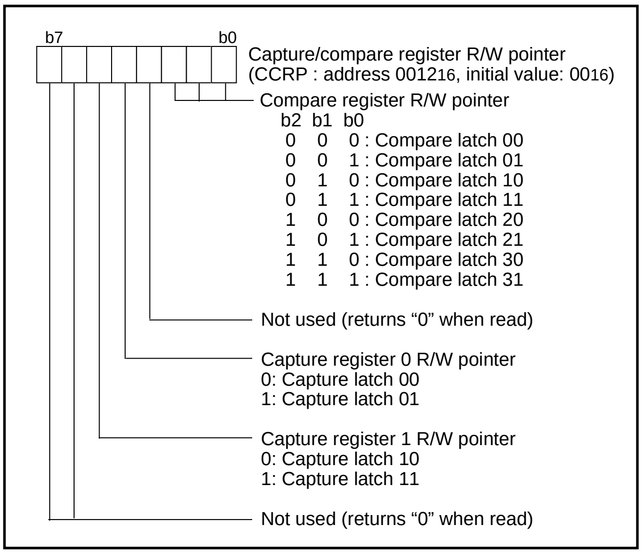


Fig. 30 Structure of capture/compare register R/W pointer

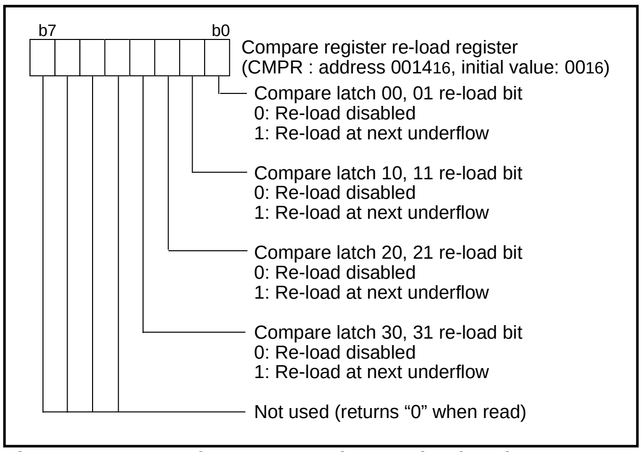


Fig. 31 Structure of compare register re-load register

b7 b0
Capture/Compare port register
(CCPR : address $001E_{16}$, initial value: 00_{16})

- Capture 0 input port bits
  b1 b0
  0 0: Capture from $P0_0$
  0 1: Capture from $P1_0$
  1 0: Ring/512
  1 1: Not available
- Compare 0 output port bit
  0: $P0_1$ is I/O port
  1: $P0_1$ is Compare 0
- Compare 1 output port bit
  0: $P0_2$ is I/O port
  1: $P0_2$ is Compare 1
- Capture 1 input port bit
  0: Capture from $P3_0$
  1: Ring/512
- Compare 2 output port bit
  0: $P3_1$ is I/O port
  1: $P3_1$ is Compare 2
- Compare 3 output port bit
  0: $P3_2$ is I/O port
  1: $P3_2$ is Compare 3
- Not used (returns “0” when read)

Fig. 32 Structure of capture/compare port register

b7 b0
Timer source selection register
(TMSR : address $001F_{16}$, initial value: 00_{16})

- Compare 0 timer source bit
- Compare 1 timer source bit
- Compare 2 timer source bit
- Compare 3 timer source bit
- Capture 0 timer source bit
- Capture 1 timer source bit
- Not used (returns “0” when read)

0: Timer A
1: Timer B

Fig. 33 Structure of timer source selection register

b7 b0
Compare output mode register
(CMOM : address 0021_{16}, initial value: 00_{16})

- Compare 0 output level latch
  0: Positive
  1: Negative
- Compare 1 output level latch
  0: Positive
  1: Negative
- Compare 2 output level latch
  0: Positive
  1: Negative
- Compare 3 output level latch
  0: Positive
  1: Negative
- Compare 0 trigger enable bit
  0: Disabled
  1: Enabled
- Compare 1 trigger enable bit
  0: Disabled
  1: Enabled
- Compare 2 trigger enable bit
  0: Disabled
  1: Enabled
- Compare 3 trigger enable bit
  0: Disabled
  1: Enabled

Fig. 34 Structure of compare output mode register

b7 b0
Capture/Compare status register
(CCSR : address 0022_{16}, initial value: 00_{16})

- Compare 0 output status bit
  0: “L” level output
  1: “H” level output
- Compare 1 output status bit
  0: “L” level output
  1: “H” level output
- Compare 2 output status bit
  0: “L” level output
  1: “H” level output
- Compare 3 output status bit
  0: “L” level output
  1: “H” level output
- Capture 0 status bit
  0: latch 00 captured
  1: latch 01 captured
- Capture 1 status bit
  0: latch 10 captured
  1: latch 11 captured
- Not used (returns “0” when read)

Fig. 35 Structure of capture/compare status register

b7 b0
Compare interrupt source register
(CISR : address 0023_{16}, initial value: 00_{16})

- Compare latch 00 interrupt source bit
- Compare latch 01 interrupt source bit
- Compare latch 10 interrupt source bit
- Compare latch 11 interrupt source bit
- Compare latch 20 interrupt source bit
- Compare latch 21 interrupt source bit
- Compare latch 30 interrupt source bit
- Compare latch 31 interrupt source bit

0: Disabled
1: Enabled

Fig. 36 Structure of compare interrupt source register

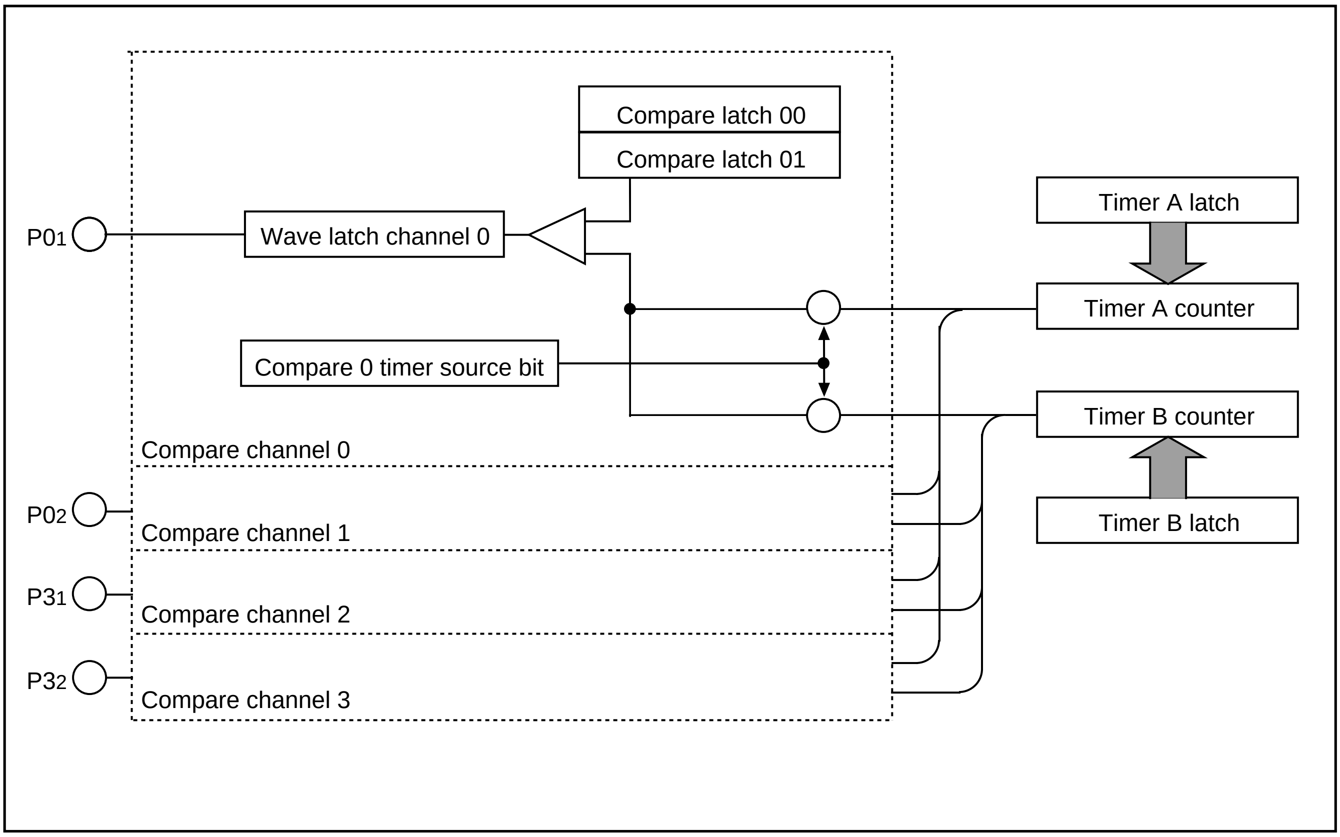


Fig. 37 Block diagram of output compare

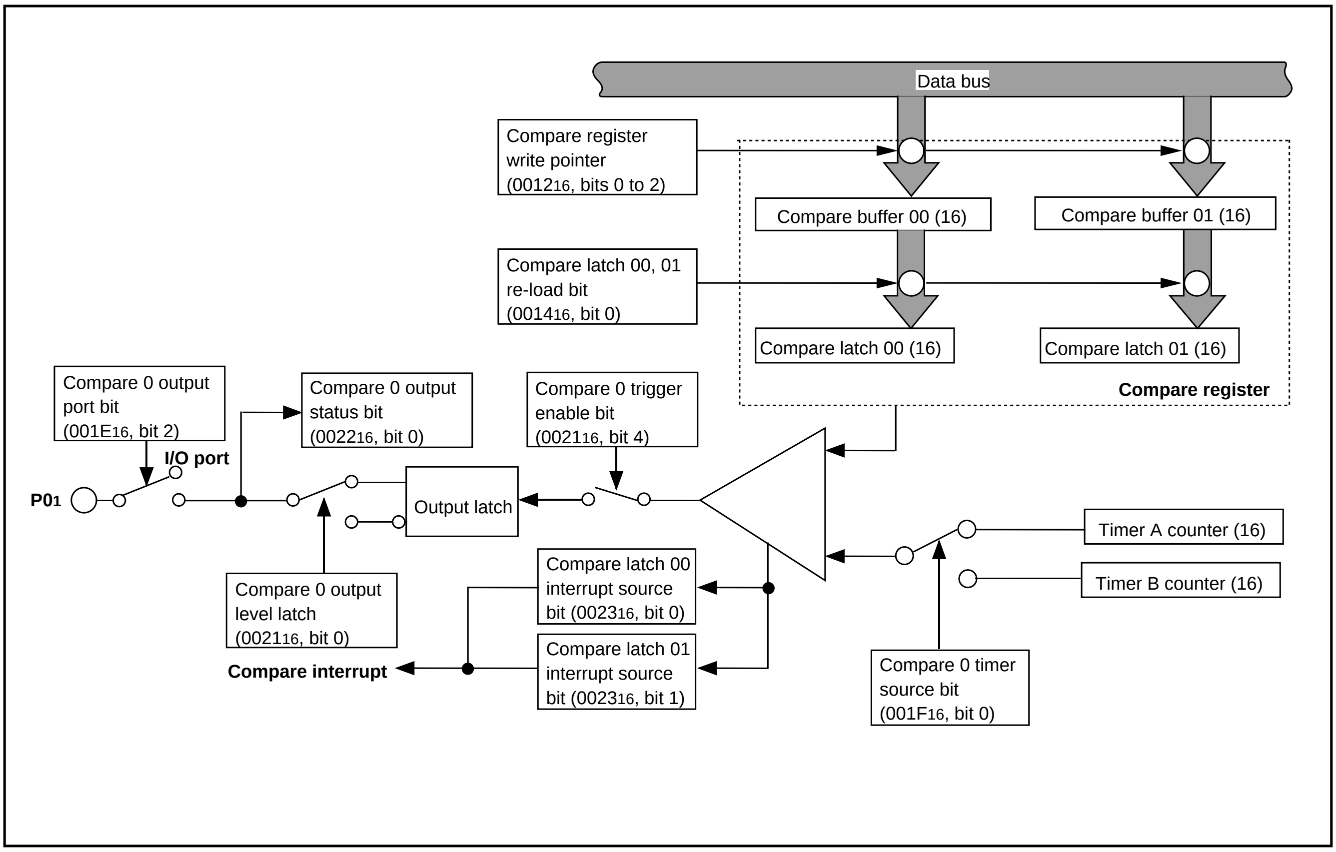


Fig. 38 Block diagram of compare channel 0

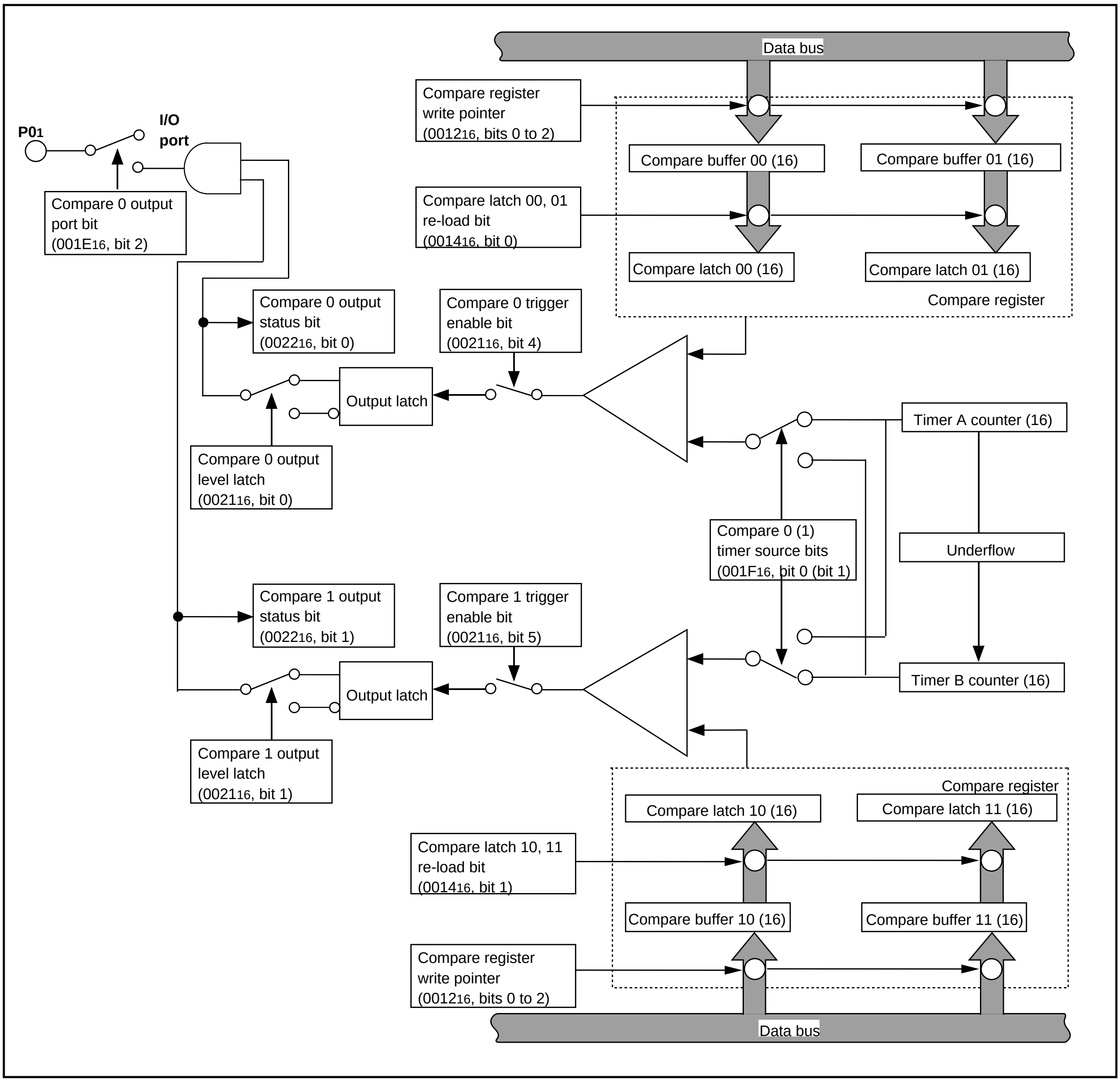


Fig. 39 Block diagram of compare channel 0, 1

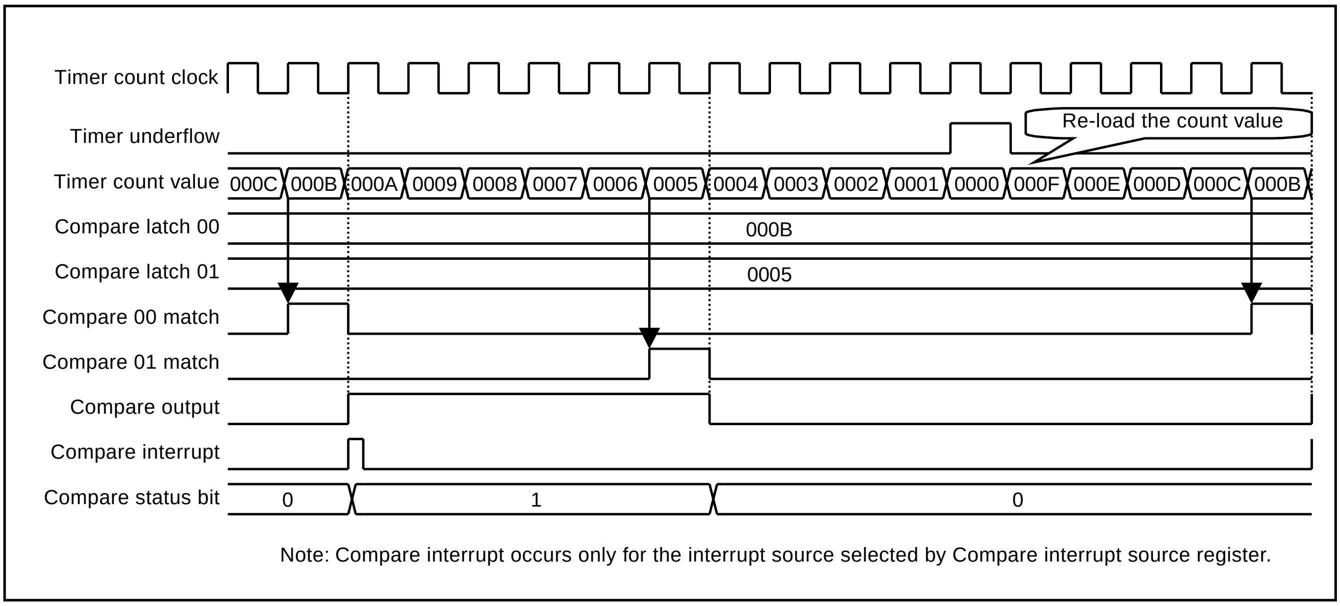


Fig. 40 Output compare mode (general waveform)

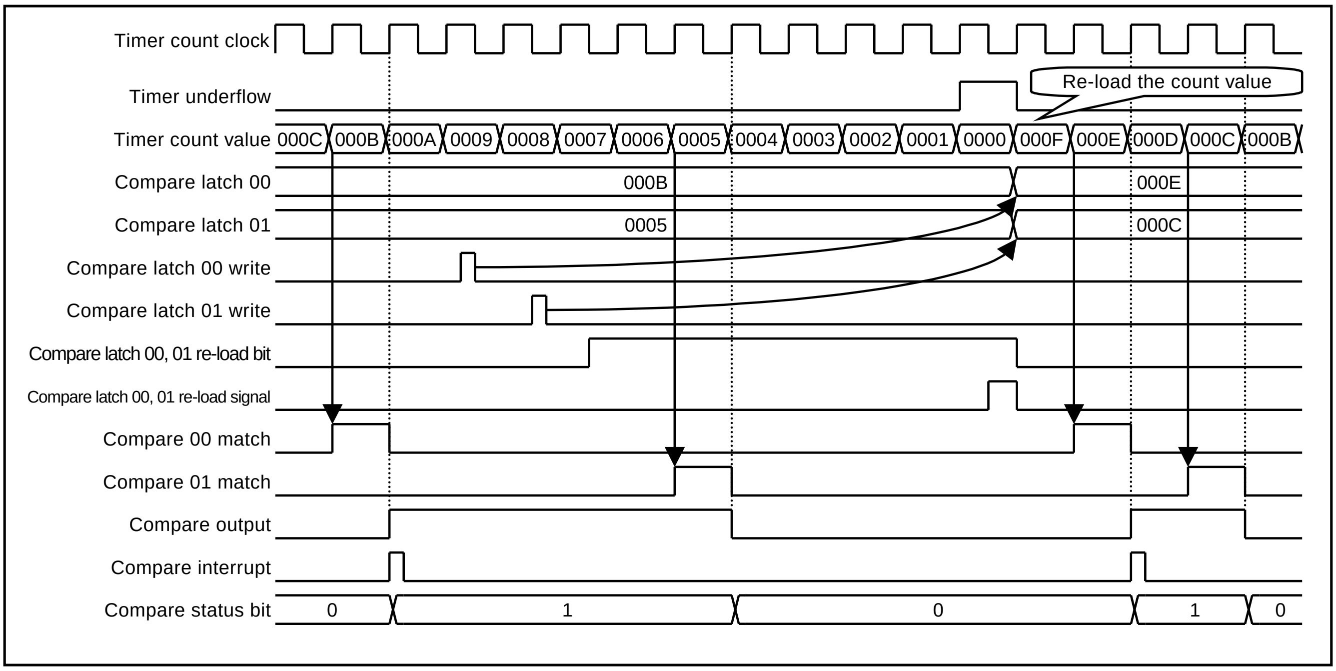


Fig. 41 Output compare mode (compare register write timing)

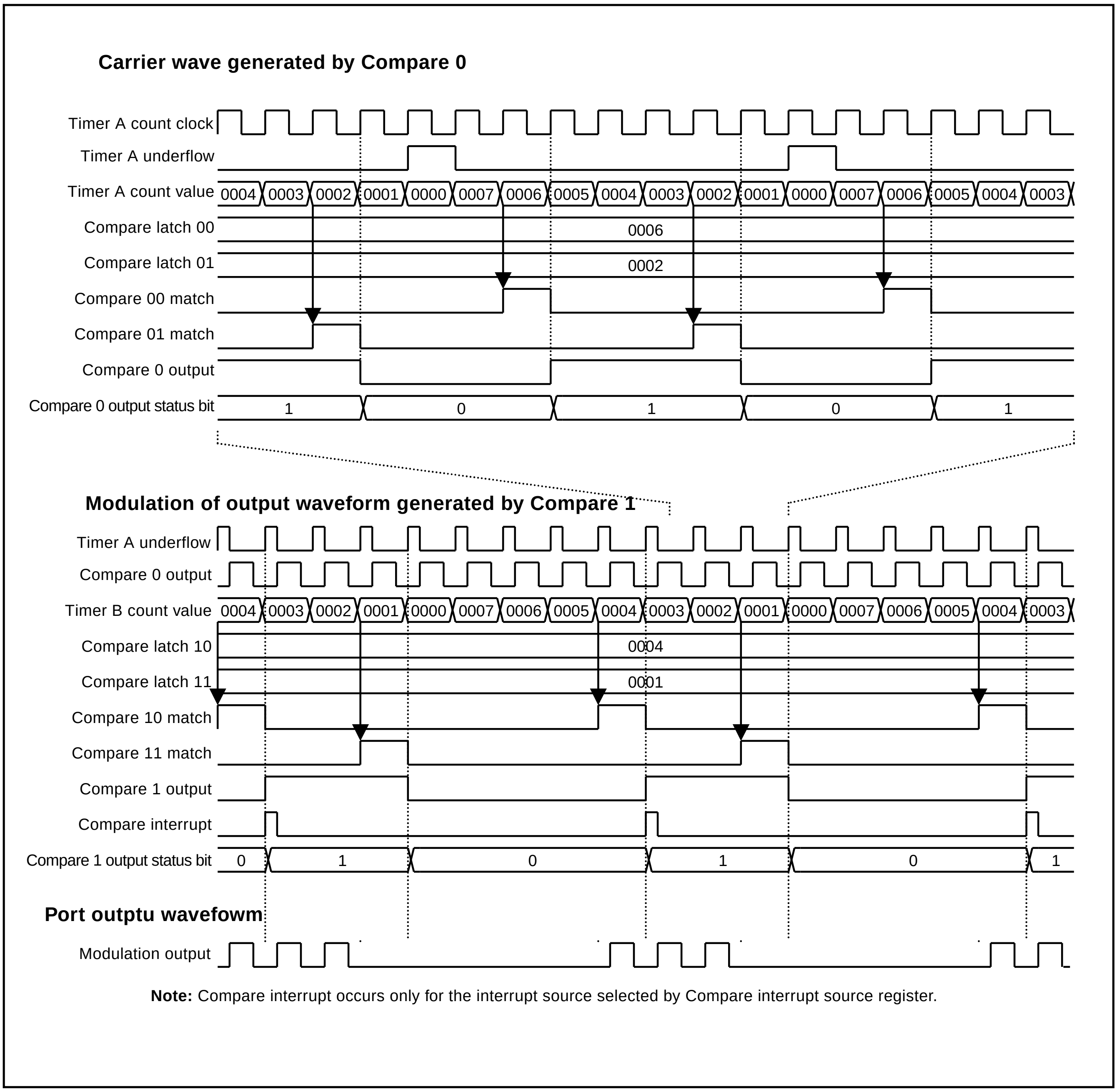


Fig. 42 Output compare mode (compare 0, 1 modulation mode)

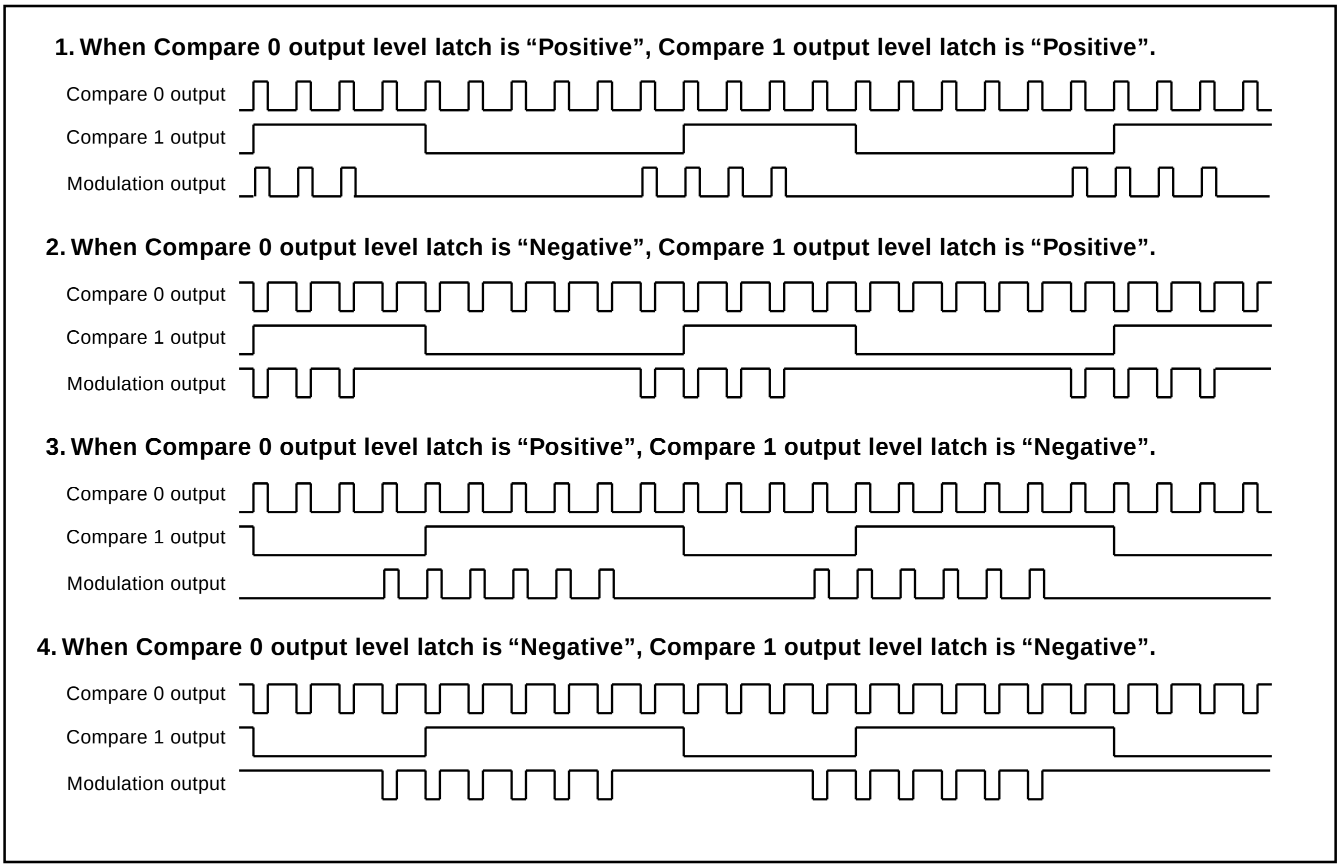


Fig. 43 Output compare mode (compare 0, 1 modulation mode: effect of output level latch)

Input capture

7542 group has 2-input capture channels. Each channel (0 and 1) has the same function and can be used to capture count value of either Timer A or Timer B.
The source timer for each channel is selected by setting value of the capture x (x = 0, 1) timer source bit. Timer A and Timer B can be selected for the source timer to each channel, respectively.

To use each capture channel, set the capture x input port bits and set the port direction register corresponding to capture channel to input mode.

The input capture circuit retains the count value of selected timer when external trigger is input. The timer count value is retained to the capture latch x0 when rising edge is input and is retained to the capture latch x1 when falling edge is input.
The count value of timer can be retained by software by capture y (y = 00, 01, 10, 11) software trigger bit too. When "1" is set to this bit, count value of timer is retained to the corresponded capture latch.
When reading from the capture y software trigger bit is executed, "0" is read out.
The latest status of capture latch can be confirmed by reading of the capture x status bit. This bit indicates the capture latch which latest data is in.

The valid trigger edge for capture interrupt is set by the capture x interrupt edge selection bits. (Regardless of the setting value of capture x interrupt edge selection bits, timer count values for both edges are retained to the capture latch.)

Each capture input has the noise filter circuit that judges continuous 4-time same level with sampling clock to be valid. The sampling clock of noise filter is set by the capture x noise filter clock selection bits.

Reading from the register for each channel is controlled by setting value of the capture register read pointer. Reading from each register is in the following order;

1. Set the value of the corresponded input capture channel to the capture register read pointer.
2. Read from the capture register (low-order) and capture register (high-order).

■ Notes on Input Capture

- If the capture trigger is input while the capture register (low-order and high-order) is in read, captured value is changed between high-order reading and low-order reading. Accordingly, some countermeasure by software is recommended, for example comparing the values that twice of read.
- When the ring-oscillator is selected for Timer A count source, Timer A cannot be used for the capture source timer.
  Timer B cannot be used for the capture source timer when the system is in the following state;
  - CPU operation clock source: X_{IN} oscillation
  - Timer B count source: Timer A underflow
  - Timer A count source: Ring oscillator output
- When writing "1" to capture latch x0 (x1) software trigger bit of capture latch x0 and x1 at the same time, or external trigger and software trigger occur simultaneously, the set value of capture x status bit is undefined.
- When setting the interrupt active edge selection bit and noise filter clock selection bit of external interrupt CAP_0, CAP_1, the interrupt request bit may be set to "1".
  When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

① Set the corresponding interrupt enable bit to "0" (disabled).
② Set the interrupt edge selection bit or noise filter clock selection bit.
③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to "1" (enabled).

- When the capture interrupt is used as the interrupt for return from stop mode, set the capture x noise filter clock selection bits to "00 (Filter stop)".

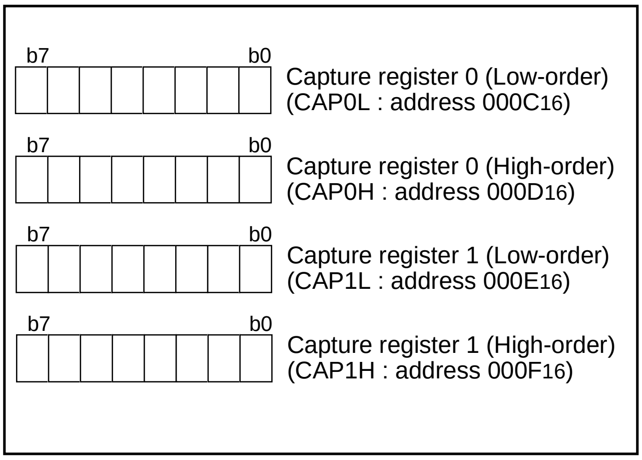


Fig. 44 Structure of capture software trigger register

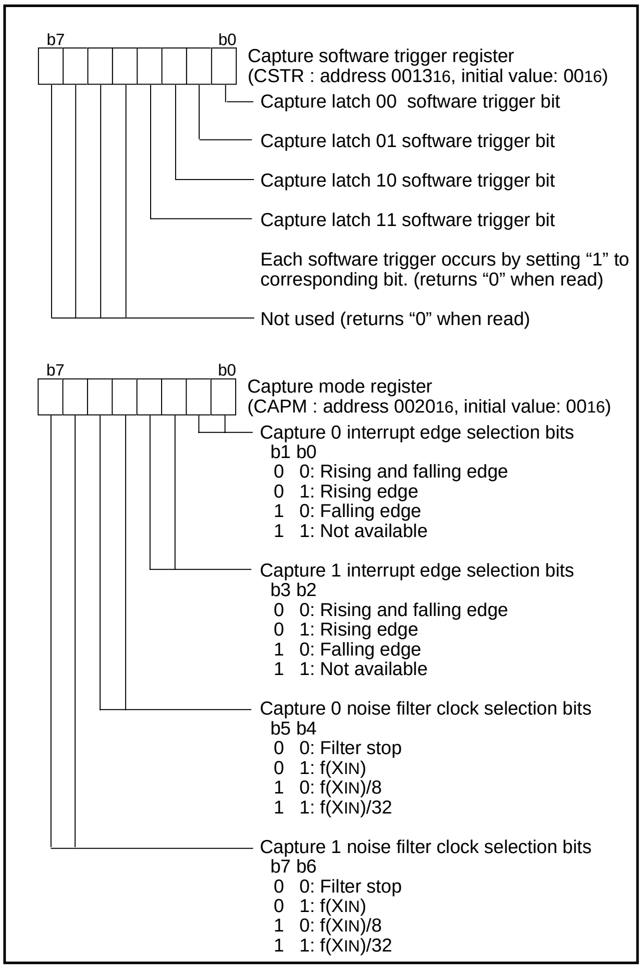


Fig. 45 Structure of capture software trigger register/capture mode register

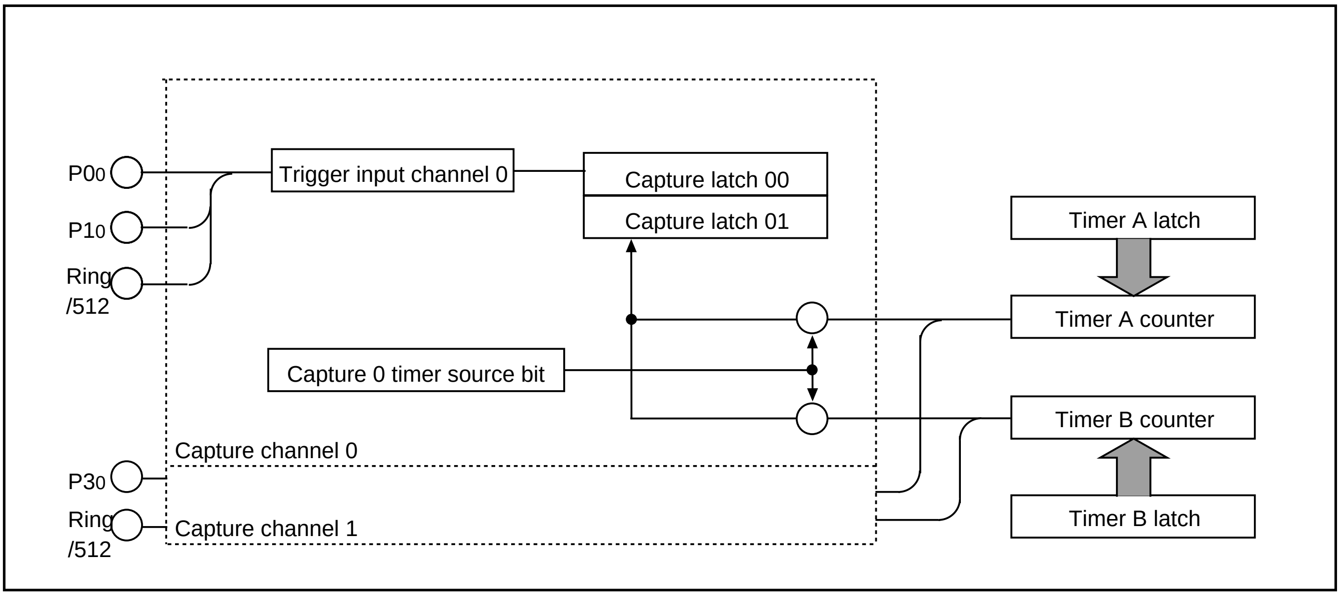


Fig. 46 Block diagram of input capture

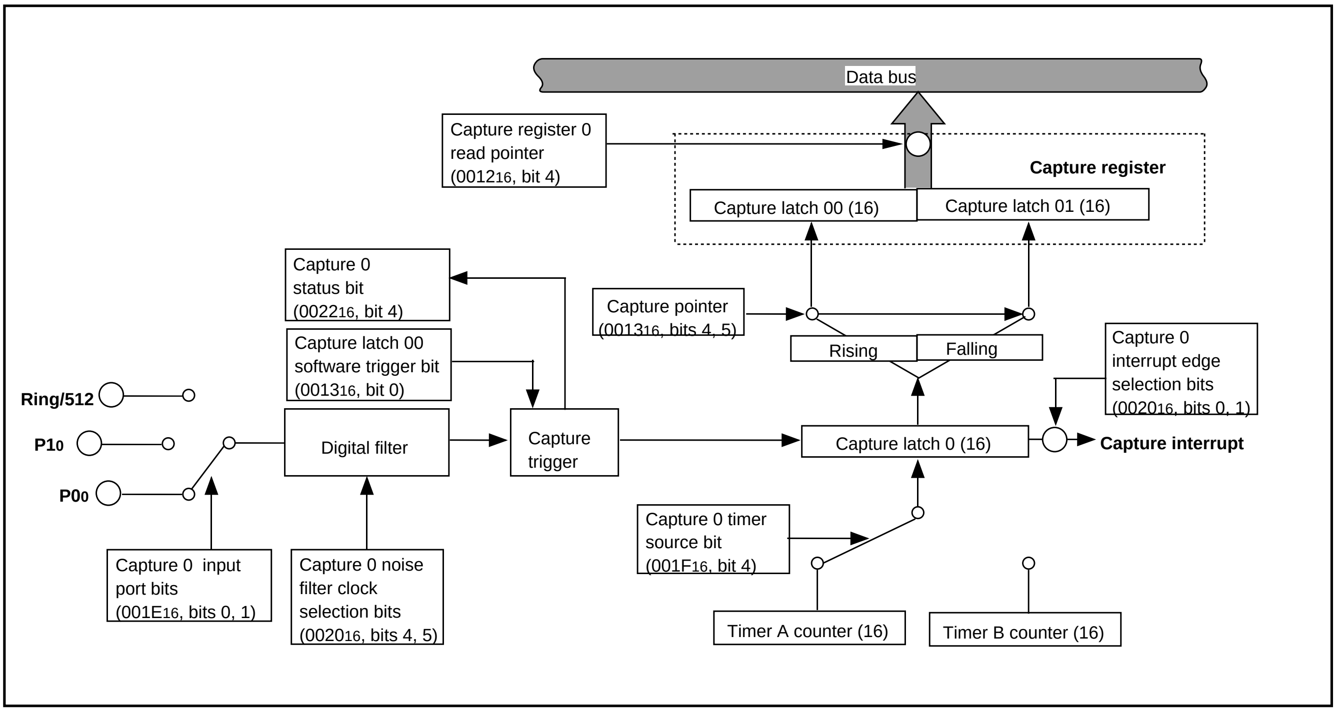


Fig. 47 Block diagram of capture channel 0

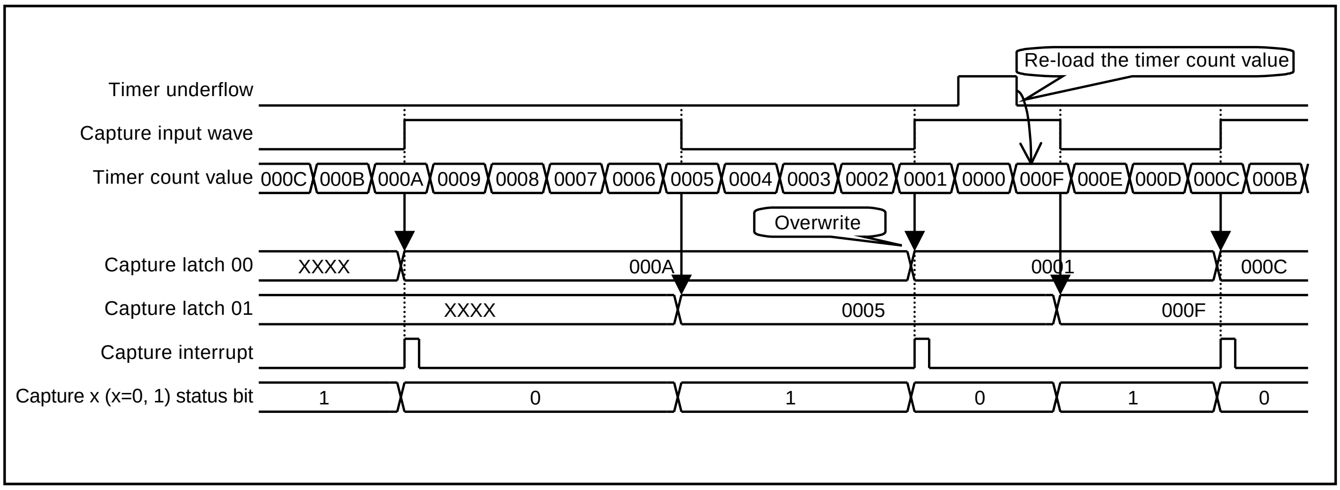


Fig. 48 Capture interrupt edge selection = "rising edge"

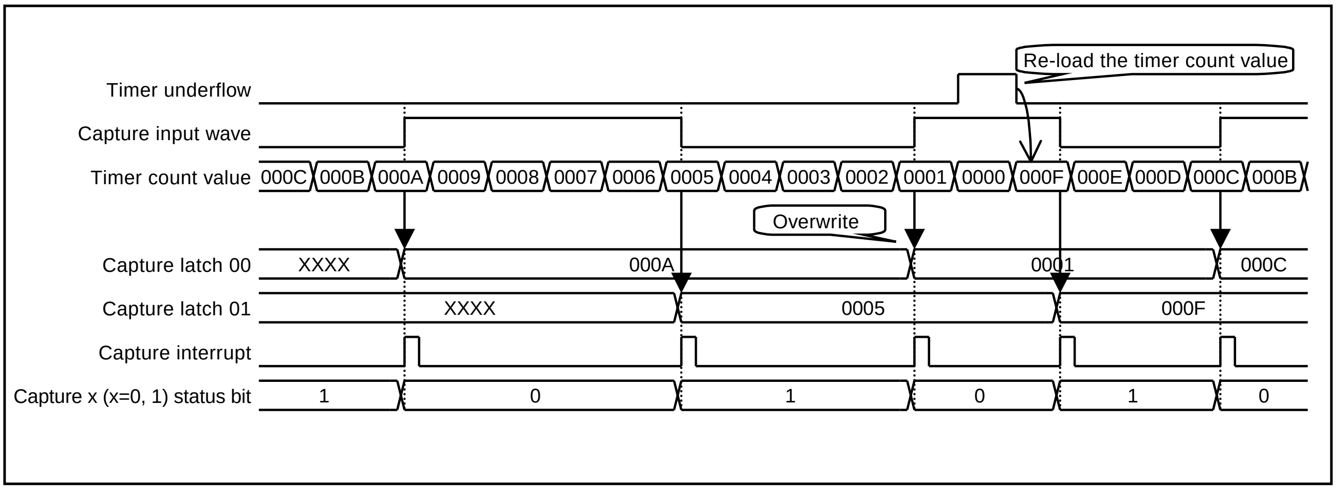


Fig. 49 Capture interrupt edge selection = "rising and falling edge"

Serial I/O

The 7542 Group has Serial I/O1 and Serial I/O2. Except that Serial I/O1 has the bus collision detection function, they have the same function.

●Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O1 Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6) to "1".

For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

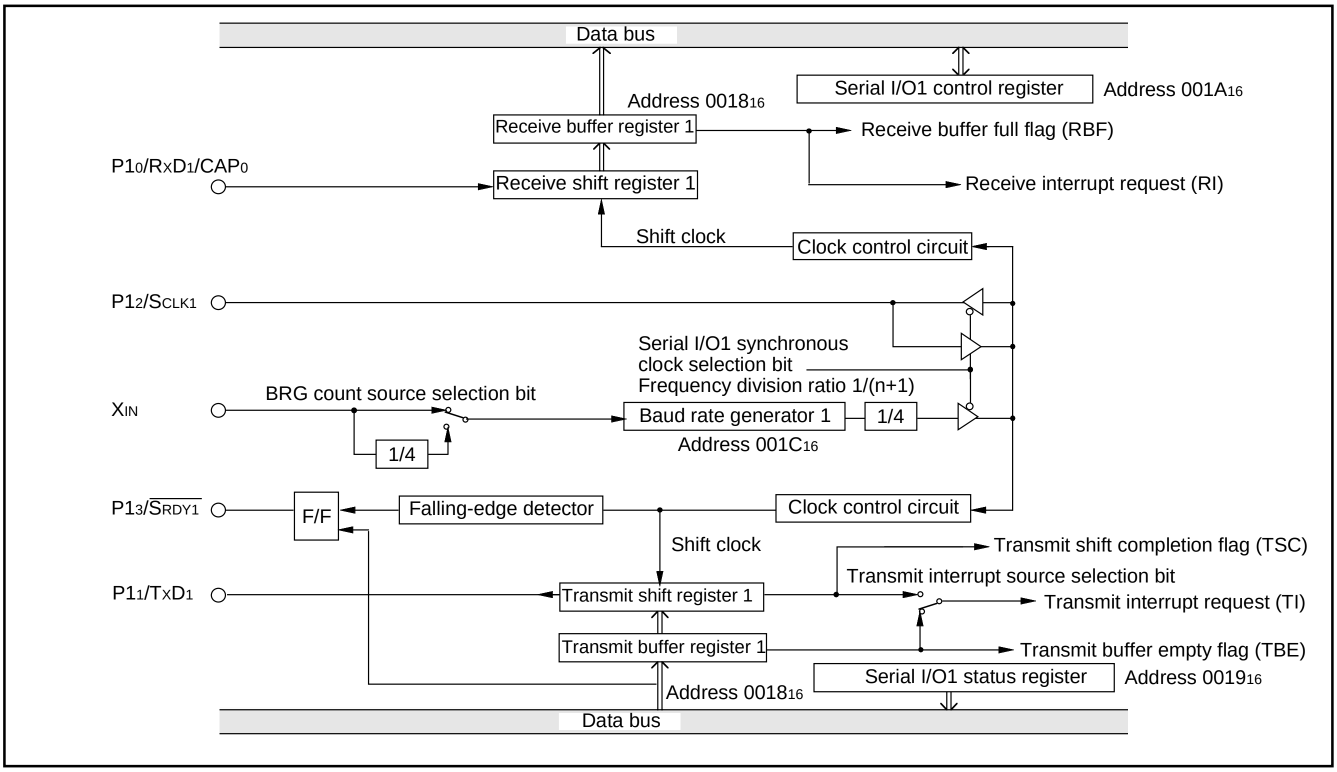
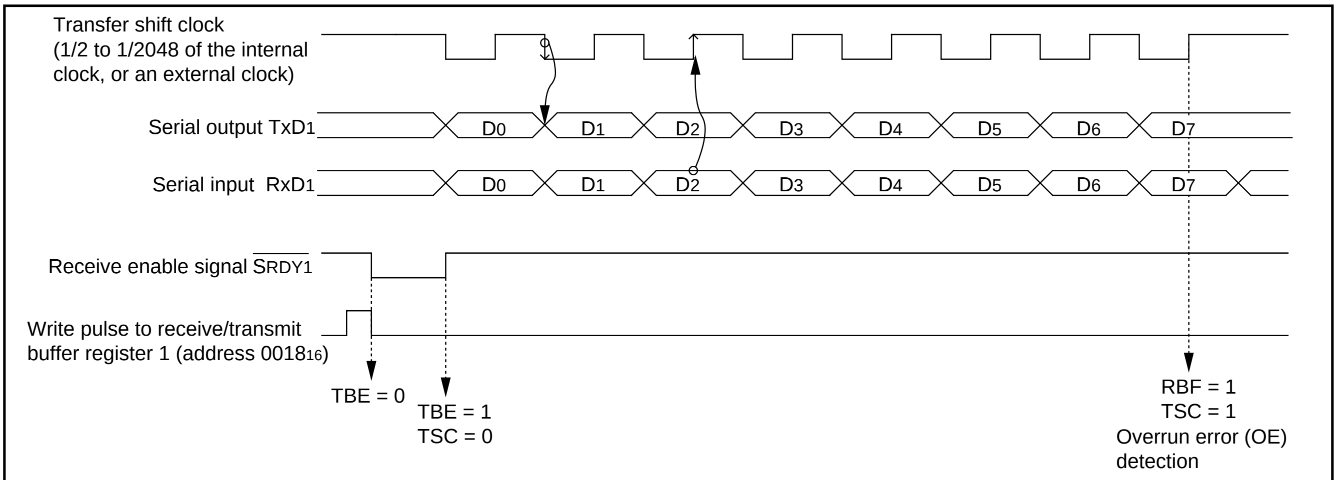


Fig. 50 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD_1 pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 51 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O1 (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

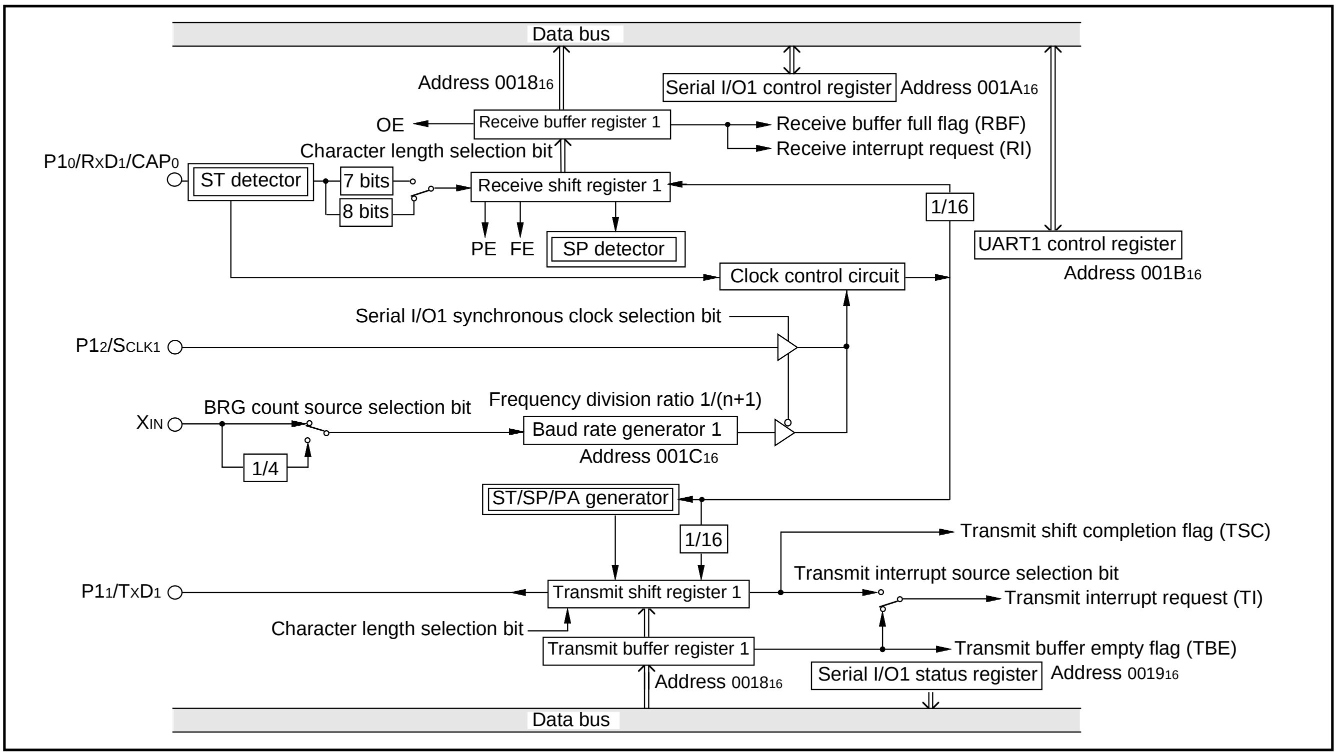
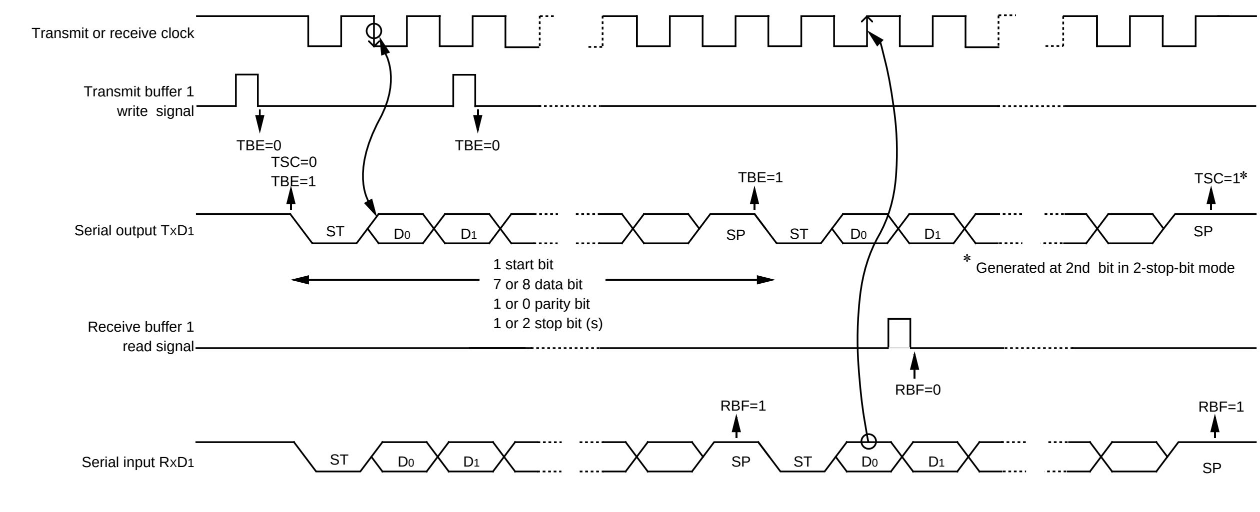


Fig. 52 Block diagram of UART serial I/O1



Notes **1:** Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1.”
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 53 Operation of UART serial I/O1 function

[Transmit buffer register 1/receive buffer register 1 (TB1/RB1)] 0018_{16}

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Serial I/O1 status register (SIO1STS)] 0019_{16}

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.
Bits 0 to 6 of the serial I/O1 status register are initialized to “0” at reset, but if the transmit enable bit of the serial I/O1 control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O1 control register (SIO1CON)] $001A_{16}$

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART1 control register (UART1CON)] $001B_{16}$

The UART1 control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the $P1_1/TxD_1$ pin.

[Baud rate generator 1 (BRG1)] $001C_{16}$

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■ Notes on Serial I/O1

• Serial I/O interrupt
When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.
① Set the serial I/O transmit interrupt enable bit to “0” (disabled).
② Set the transmit enable bit to “1”.
③ Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
⑤ Set the serial I/O transmit interrupt enable bit to “1” (enabled).

• I/O pin function when serial I/O1 is enabled.
The functions of $P1_2$ and $P1_3$ are switched with the setting values of a serial I/O1 mode selection bit and a serial I/O1 synchronous clock selection bit as follows.

(1) Serial I/O1 mode selection bit → “1” :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O1 synchronous clock selection bit
“0” : $P1_2$ pin turns into an output pin of a synchronous clock.
“1” : $P1_2$ pin turns into an input pin of a synchronous clock.
Setup of a $\overline{SRDY_1}$ output enable bit (SRDY)
“0” : $P1_3$ pin can be used as a normal I/O pin.
“1” : $P1_3$ pin turns into a $\overline{SRDY_1}$ output pin.

(2) Serial I/O1 mode selection bit → “0” :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O1 synchronous clock selection bit
“0”: $P1_2$ pin can be used as a normal I/O pin.
“1”: $P1_2$ pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is $P1_3$ pin. It can be used as a normal I/O pin.

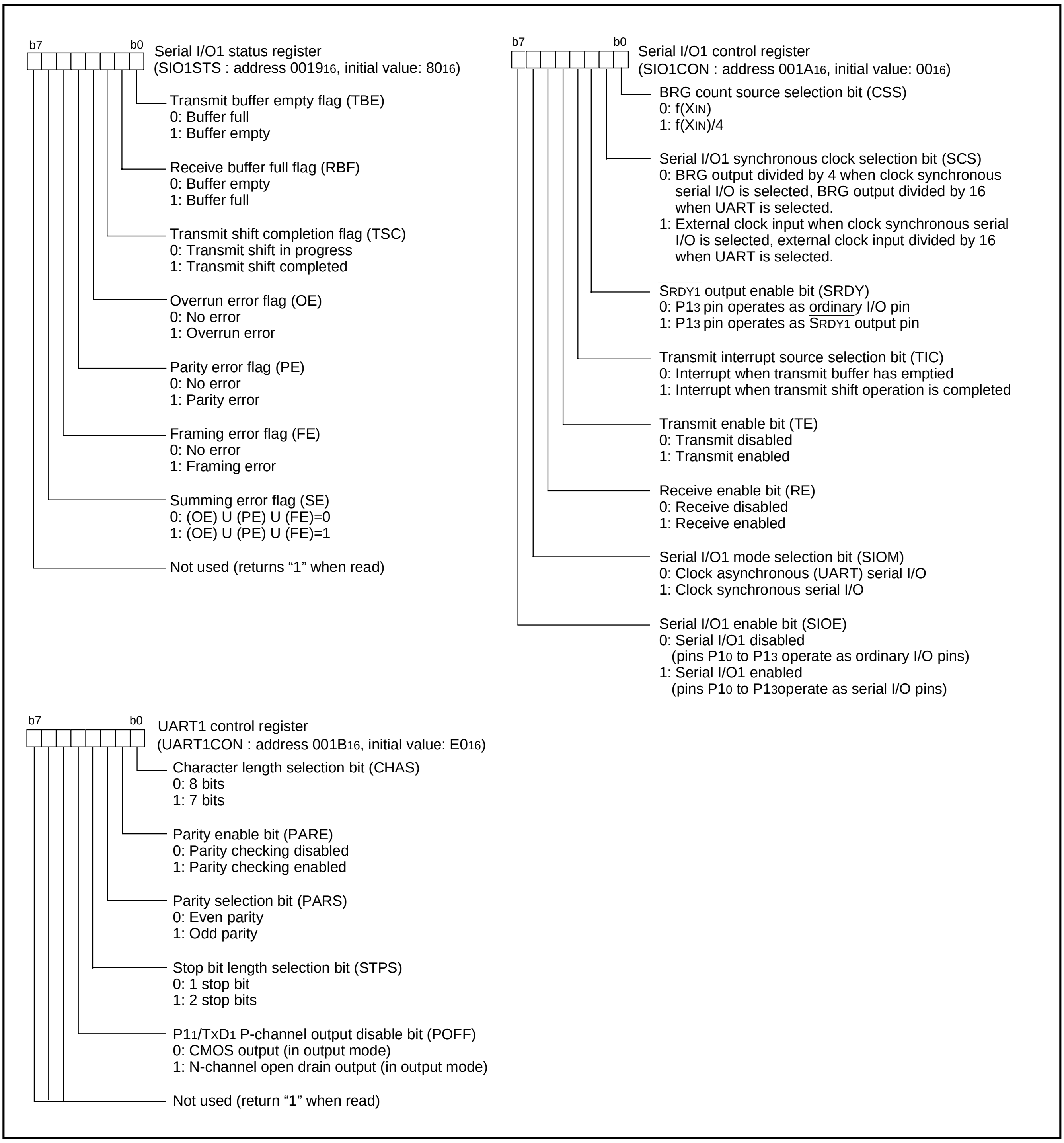


Fig. 54 Structure of serial I/O1-related registers

Bus collision detection (SIO1)

SIO1 can detect a bus collision by setting UART1 bus collision detection interrupt enable bit.

When transmission is started in the clock synchronous or asynchronous (UART) serial I/O mode, the transmit pin TxD_1 is compared with the receive pin RxD_1 in synchronization with rising edge of transmit shift clock. If they do not coincide with each other, a bus collision detection interrupt request occurs.

When a transmit data collision is detected between LSB and MSB of transmit data in the clock synchronous serial I/O mode or between the start bit and stop bit of transmit data in UART mode, a bus collision detection can be performed by both the internal clock and the external clock.

A block diagram is shown in Fig. 56.
A timing diagram is shown in Fig. 57.

Note: Bus collision detection can be used when SIO1 is operating at full-duplex communication. When SIO1 is operating at half-duplex communication, set bus collision detection interrupt to be disabled.

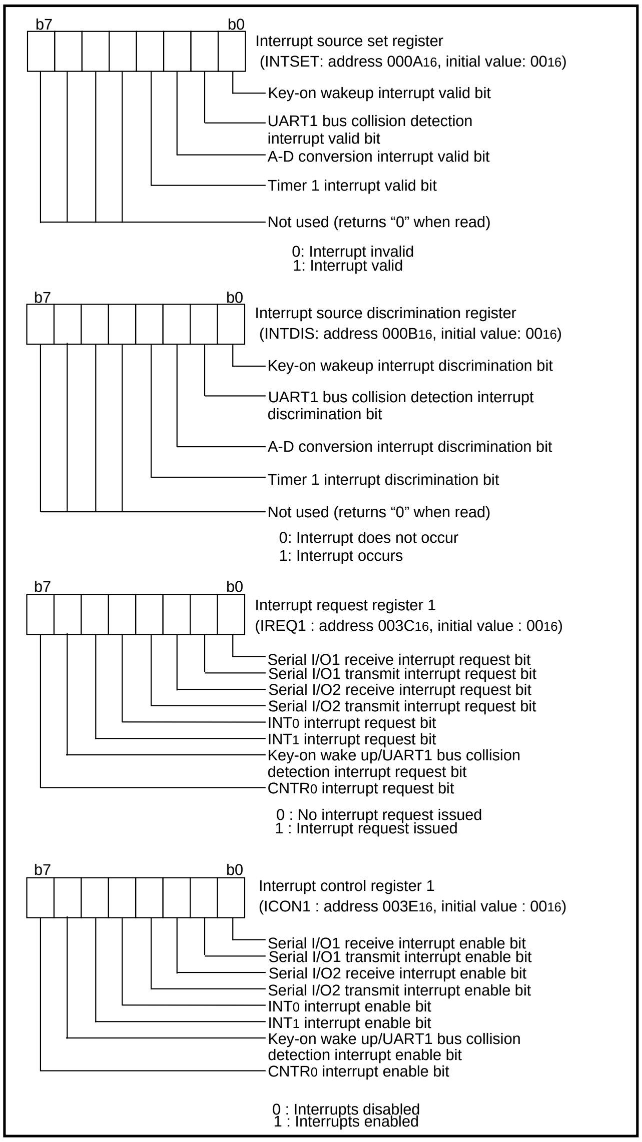


Fig. 55 Bus collision detection circuit related registers

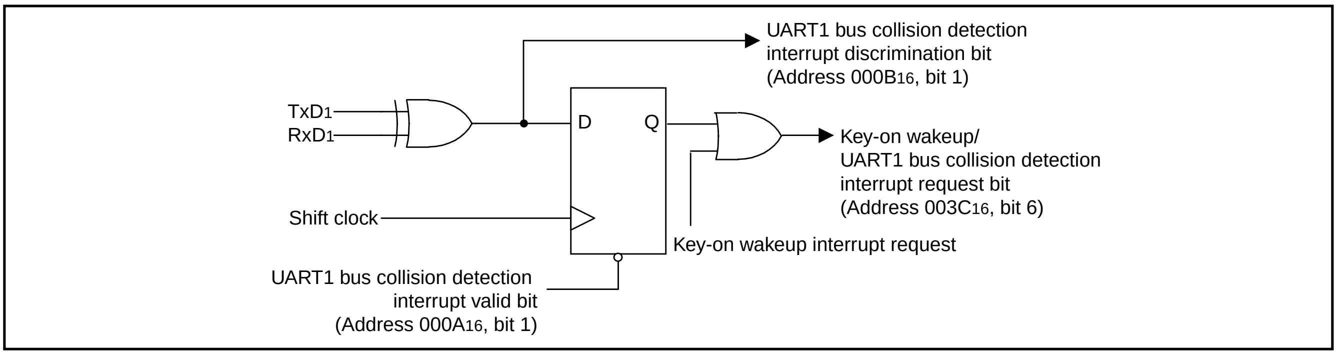


Fig. 56 Block diagram of bus collision detection interrupt circuit

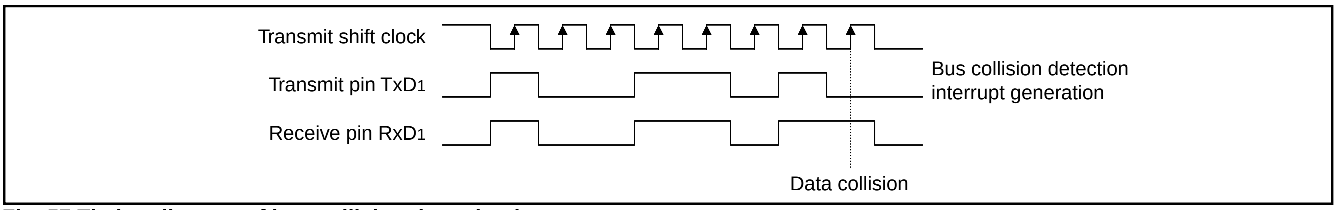


Fig. 57 Timing diagram of bus collision detection interrupt

●Serial I/O2

Serial I/O2 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O2 Mode

Clock synchronous serial I/O2 mode can be selected by setting the serial I/O2 mode selection bit of the serial I/O2 control register (bit 6) to "1".

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

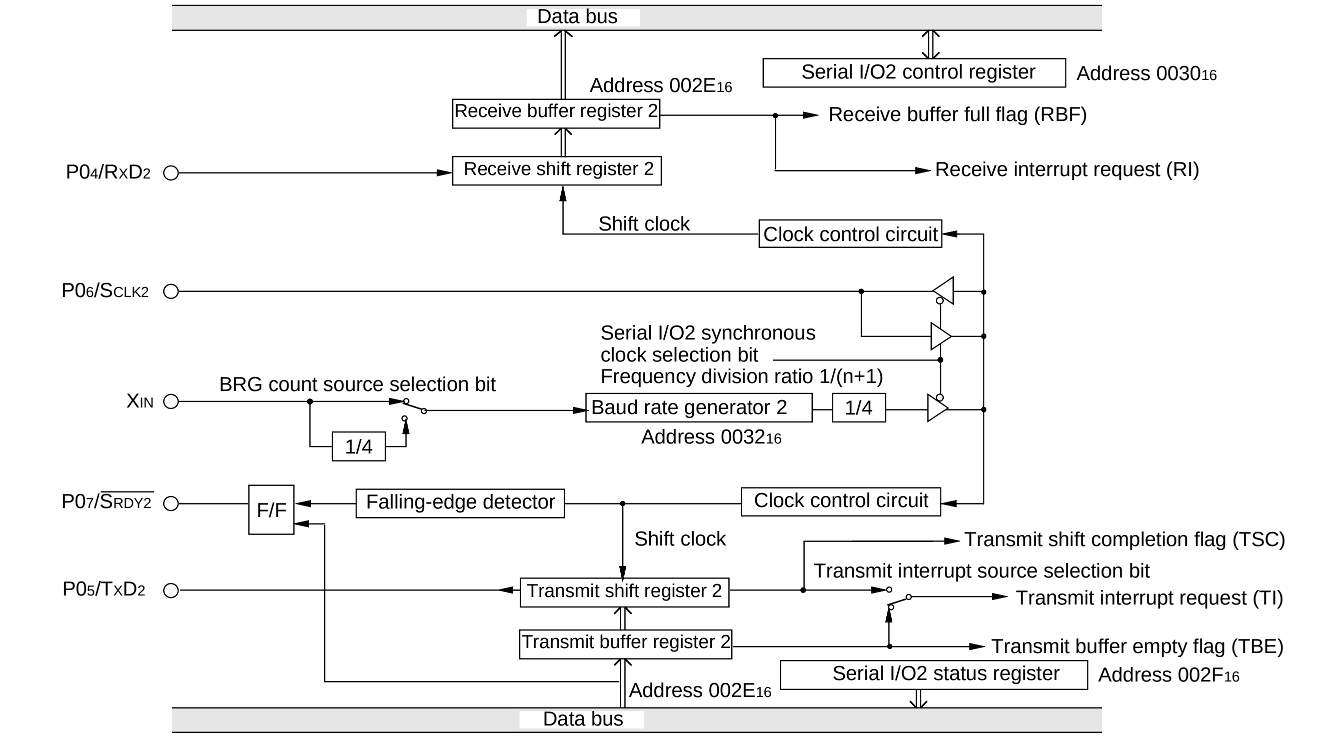
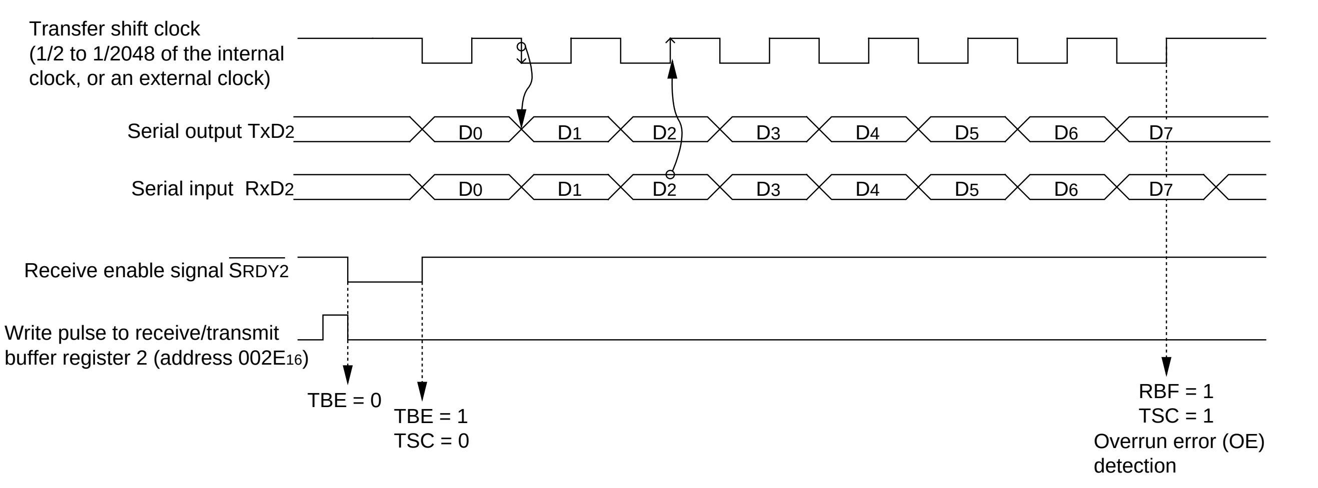


Fig. 58 Block diagram of clock synchronous serial I/O2



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O2 control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD$_2$ pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 59 Operation of clock synchronous serial I/O2 function

(2) Asynchronous Serial I/O2 (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O2 mode selection bit of the serial I/O2 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

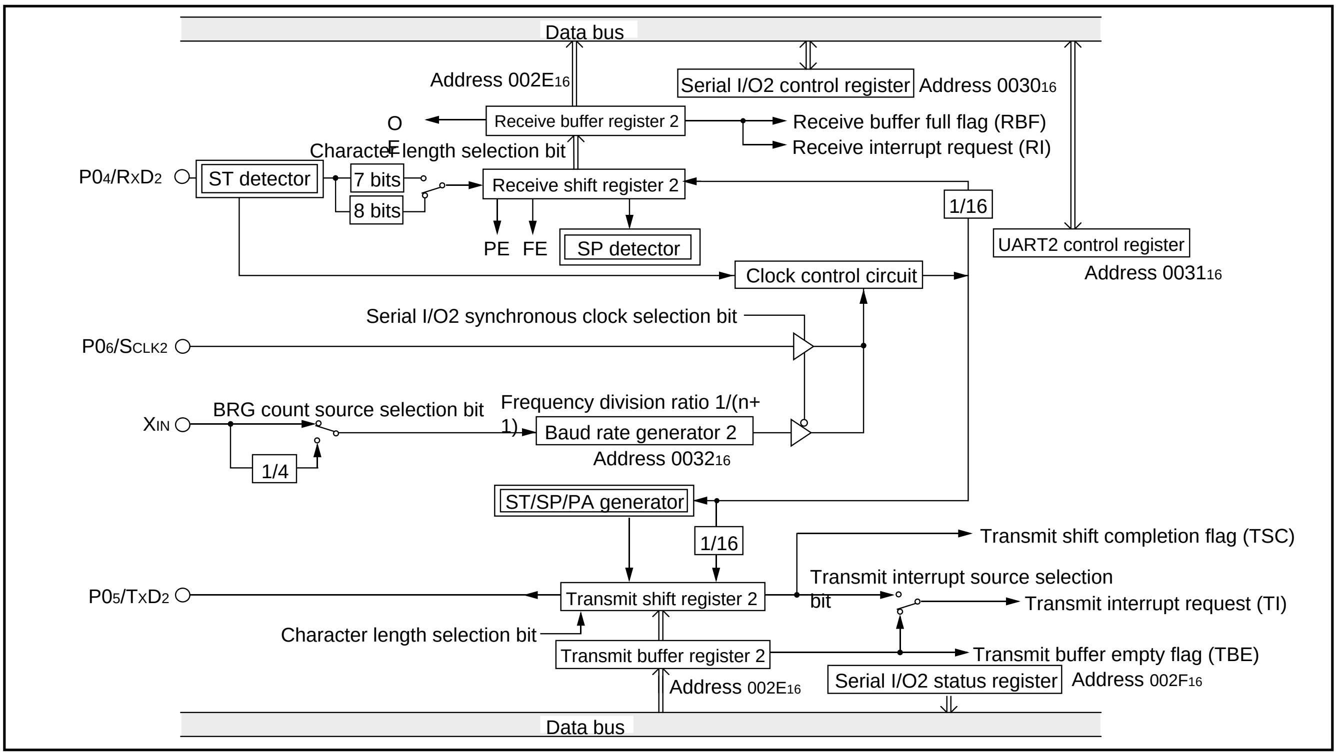
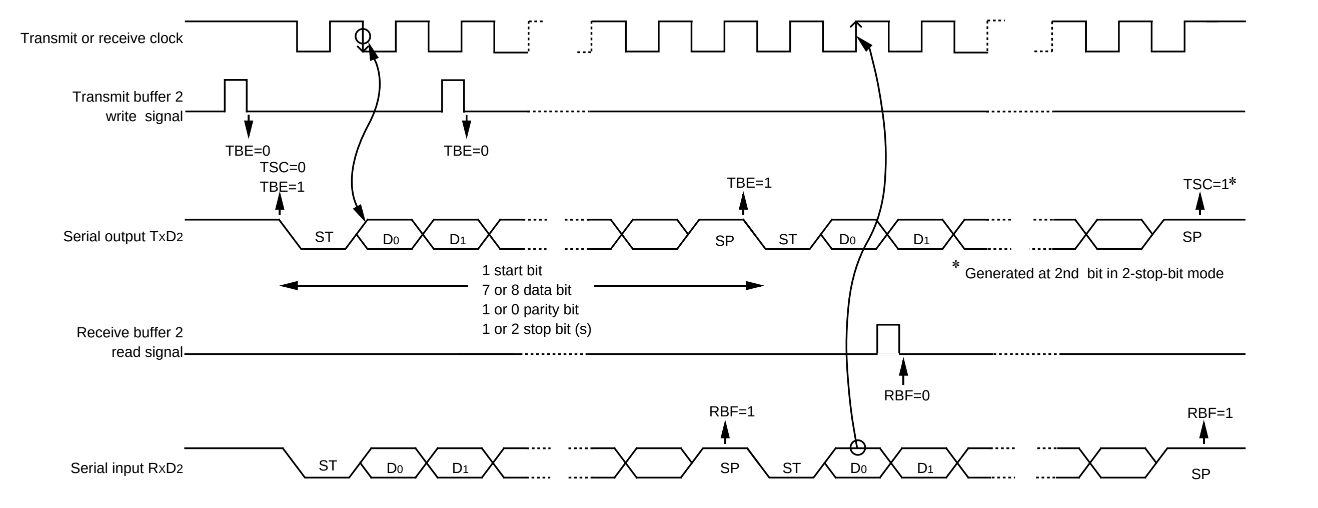


Fig. 60 Block diagram of UART serial I/O2



Notes
1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O2 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1.”
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 61 Operation of UART serial I/O2 function

[Transmit buffer register 2/receive buffer register 2 (TB2/RB2)] 002E16

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Serial I/O2 status register (SIO2STS)] 002F16

The read-only serial I/O2 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O2 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O2 enable bit SIOE (bit 7 of the serial I/O2 control register) also clears all the status flags, including the error flags.
Bits 0 to 6 of the serial I/O2 status register are initialized to “0” at reset, but if the transmit enable bit of the serial I/O2 control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O2 control register (SIO2CON)] 003016

The serial I/O2 control register consists of eight control bits for the serial I/O2 function.

[UART2 control register (UART2CON)] 003116

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P05/TxD2 pin.

[Baud rate generator 2 (BRG2)] 003216

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■ Notes on Serial I/O2

• Serial I/O interrupt

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.
① Set the serial I/O transmit interrupt enable bit to “0” (disabled).
② Set the transmit enable bit to “1”.
③ Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
⑤ Set the serial I/O transmit interrupt enable bit to “1” (enabled).

• I/O pin function when serial I/O2 is enabled.

The functions of P06 and P07 are switched with the setting values of a serial I/O2 mode selection bit and a serial I/O2 synchronous clock selection bit as follows.

(1) Serial I/O2 mode selection bit → “1” :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O2 synchronous clock selection bit
“0” : P06 pin turns into an output pin of a synchronous clock.
“1” : P06 pin turns into an input pin of a synchronous clock.
Setup of a $\overline{\text{SRDY2}}$ output enable bit (SRDY)
“0” : P07 pin can be used as a normal I/O pin.
“1” : P07 pin turns into a $\overline{\text{SRDY2}}$ output pin.

(2) Serial I/O2 mode selection bit → “0” :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O2 synchronous clock selection bit
“0”: P06 pin can be used as a normal I/O pin.
“1”: P06 pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is P07 pin. It can be used as a normal I/O pin.

Serial I/O2 status register (SIO2STS : address $002F_{16}$, initial value: 80_{16}) (b7 … b0)

- b0: Transmit buffer empty flag (TBE)
  0: Buffer full
  1: Buffer empty
- b1: Receive buffer full flag (RBF)
  0: Buffer empty
  1: Buffer full
- b2: Transmit shift completion flag (TSC)
  0: Transmit shift in progress
  1: Transmit shift completed
- b3: Overrun error flag (OE)
  0: No error
  1: Overrun error
- b4: Parity error flag (PE)
  0: No error
  1: Parity error
- b5: Framing error flag (FE)
  0: No error
  1: Framing error
- b6: Summing error flag (SE)
  0: (OE) U (PE) U (FE)=0
  1: (OE) U (PE) U (FE)=1
- b7: Not used (returns “1” when read)

Serial I/O2 control register (SIO2CON : address 0030_{16}, initial value: 00_{16}) (b7 … b0)

- b0: BRG count source selection bit (CSS)
  0: f(X_{IN})
  1: f(X_{IN})/4
- b1: Serial I/O2 synchronous clock selection bit (SCS)
  0: BRG output divided by 4 when clock synchronous serial I/O is selected, BRG output divided by 16 when UART is selected.
  1: External clock input when clock synchronous serial I/O is selected, external clock input divided by 16 when UART is selected.
- b2: $\overline{S_{RDY2}}$ output enable bit (SRDY)
  0: $P0_7$ pin operates as ordinary I/O pin
  1: $P0_7$ pin operates as $\overline{S_{RDY2}}$ output pin
- b3: Transmit interrupt source selection bit (TIC)
  0: Interrupt when transmit buffer has emptied
  1: Interrupt when transmit shift operation is completed
- b4: Transmit enable bit (TE)
  0: Transmit disabled
  1: Transmit enabled
- b5: Receive enable bit (RE)
  0: Receive disabled
  1: Receive enabled
- b6: Serial I/O2 mode selection bit (SIOM)
  0: Clock asynchronous (UART) serial I/O
  1: Clock synchronous serial I/O
- b7: Serial I/O2 enable bit (SIOE)
  0: Serial I/O2 disabled (pins $P0_4$ to $P0_7$ operate as ordinary I/O pins)
  1: Serial I/O2 enabled (pins $P0_4$ to $P0_7$ operate as serial I/O pins)

UART2 control register (UART2CON : address 0031_{16}, initial value: $E0_{16}$) (b7 … b0)

- b0: Character length selection bit (CHAS)
  0: 8 bits
  1: 7 bits
- b1: Parity enable bit (PARE)
  0: Parity checking disabled
  1: Parity checking enabled
- b2: Parity selection bit (PARS)
  0: Even parity
  1: Odd parity
- b3: Stop bit length selection bit (STPS)
  0: 1 stop bit
  1: 2 stop bits
- b4: $P0_5$/T_XD_2 P-channel output disable bit (POFF)
  0: CMOS output (in output mode)
  1: N-channel open drain output (in output mode)
- b5–b7: Not used (return “1” when read)

Fig. 62 Structure of serial I/O2-related registers

A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

[A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the A-D conversion completion bit. The value of this bit remains at “0” during A-D conversion, and changes to “1” at completion of A-D conversion.
A-D conversion is started by setting this bit to “0”.

[Comparison voltage generator]

The comparison voltage generator divides the voltage between AVSS and VREF by 1024, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of ports P2$_7$/AN$_7$ to P2$_0$/AN$_0$, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to “1”. Because the comparator is constructed linked to a capacitor, set f(XIN) to 500 kHz or more during A-D conversion.

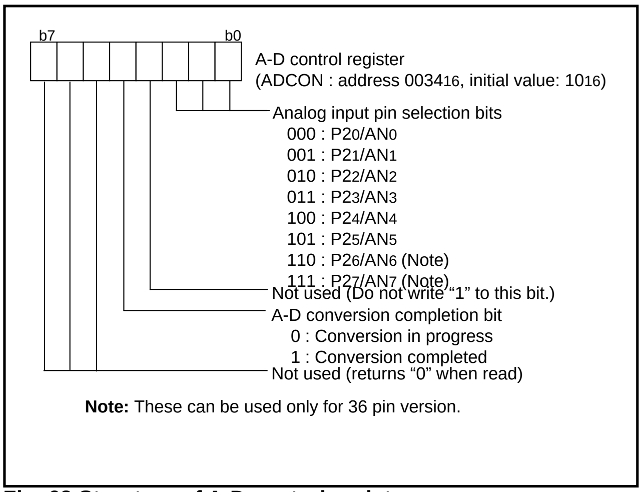


Fig. 63 Structure of A-D control register

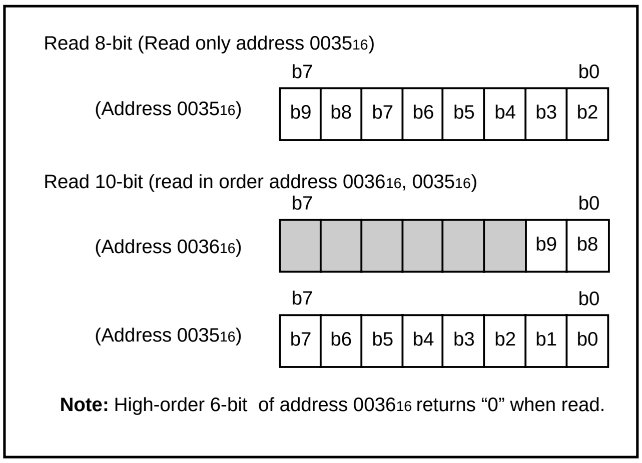


Fig. 64 Structure of A-D conversion register

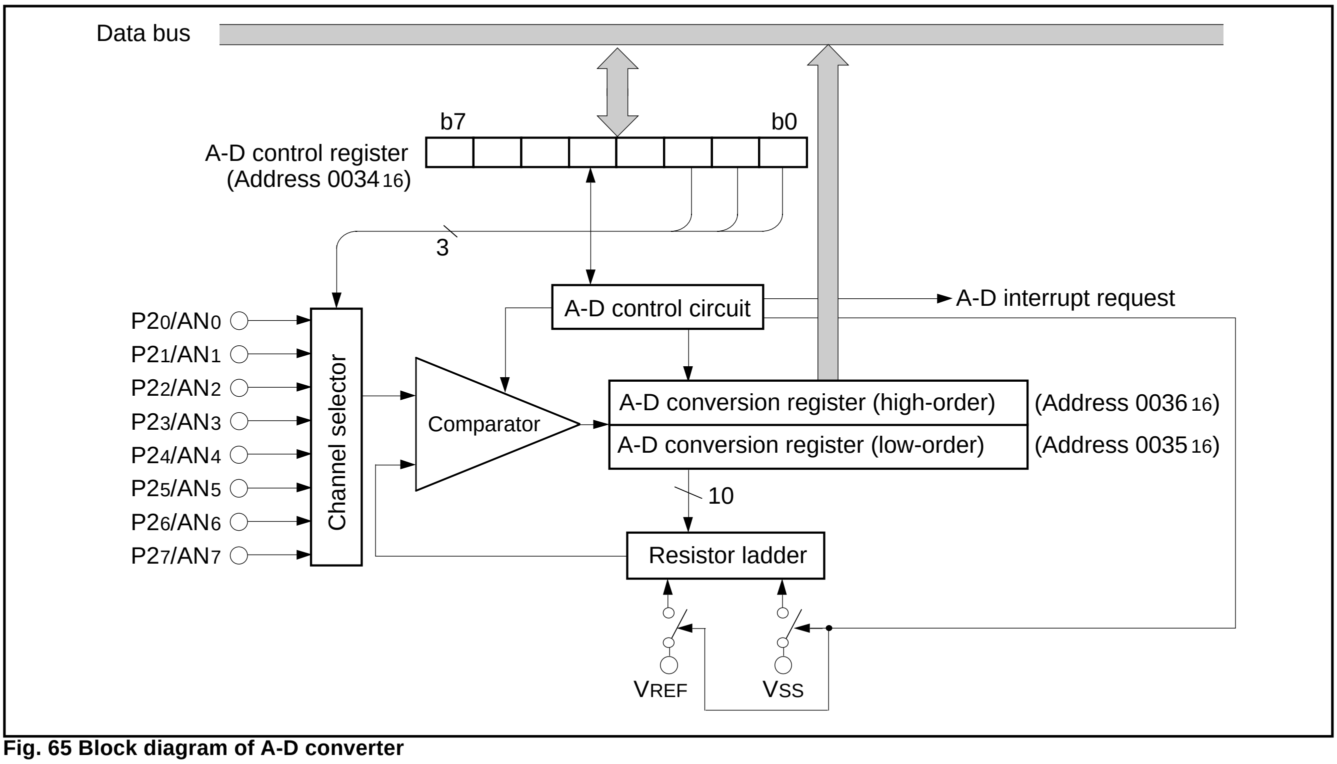


Fig. 65 Block diagram of A-D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039_{16}) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039_{16}) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039_{16}) can be set before an underflow occurs.
When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039_{16}), the watchdog timer H is set to "FF_{16}" and the watchdog timer L is set to "FF_{16}".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039_{16}). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at $f(X_{IN})$=8 MHz.
When this bit is "1", the count source becomes $f(X_{IN})/16$. In this case, the detection time is 512 µs at $f(X_{IN})$=8 MHz.
This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039_{16}).
When this bit is "0", the STP instruction is enabled.
When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.
Once this bit is set to "1", it cannot be changed to "0" by program.
This bit is cleared to "0" after reset.

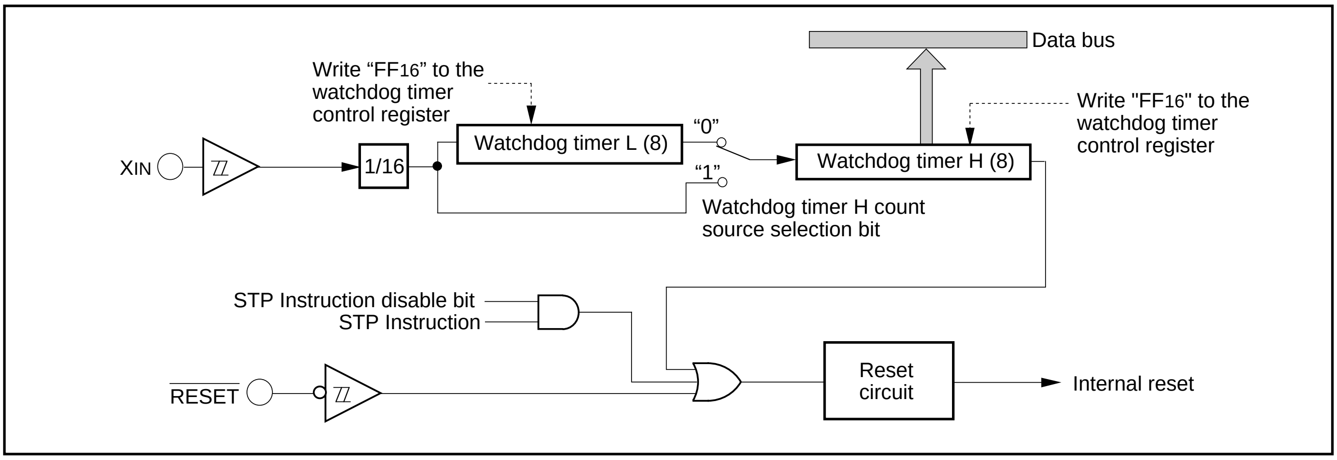


Fig. 66 Block diagram of watchdog timer

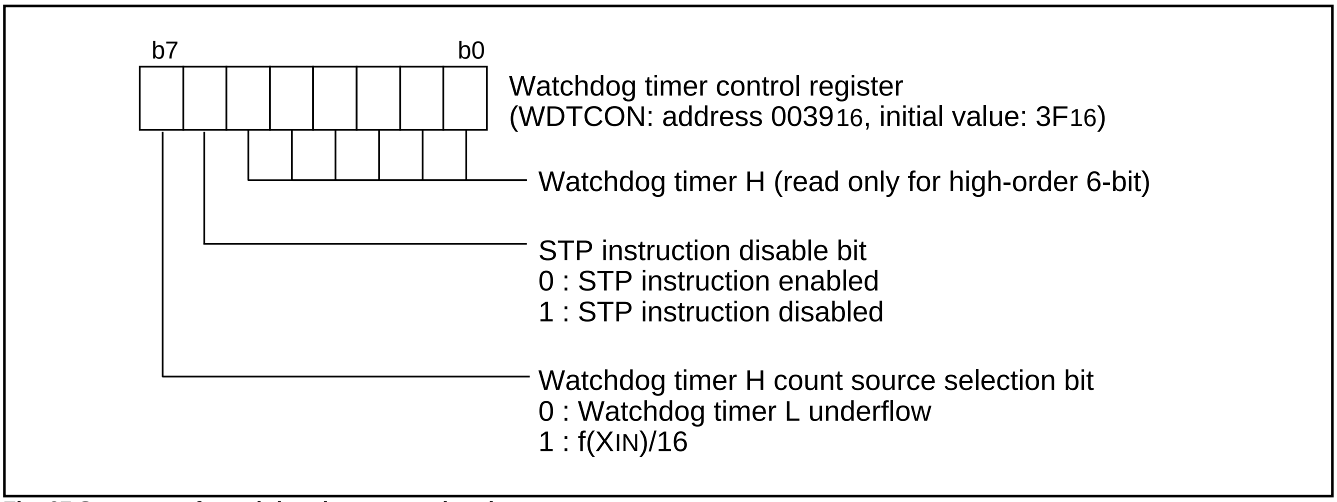


Fig. 67 Structure of watchdog timer control register

Reset Circuit

The 7542 group starts operation by the built-in ring oscillator after system is released from reset.

Accordingly, when the rising of power supply voltage passes 2.2V, set the reset input voltage to become below 0.2Vcc (0.44V).

Moreover, switch CPU clock to the external oscillator after the rising of power supply voltage passes the minimum operation voltage and after an oscillation is stabilized.

Note: The minimum operation voltage is decided by the division ratio of an external oscillator's frequency and a CPU clock. Decide on an external oscillatior's oscillation stabilizing time after fully evaluating an oscillatior's stabilizing time used.

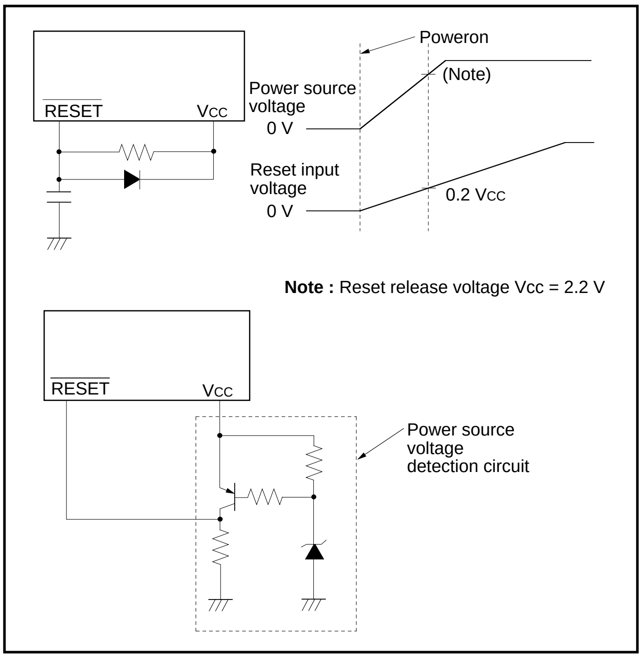


Fig. 68 Example of reset circuit

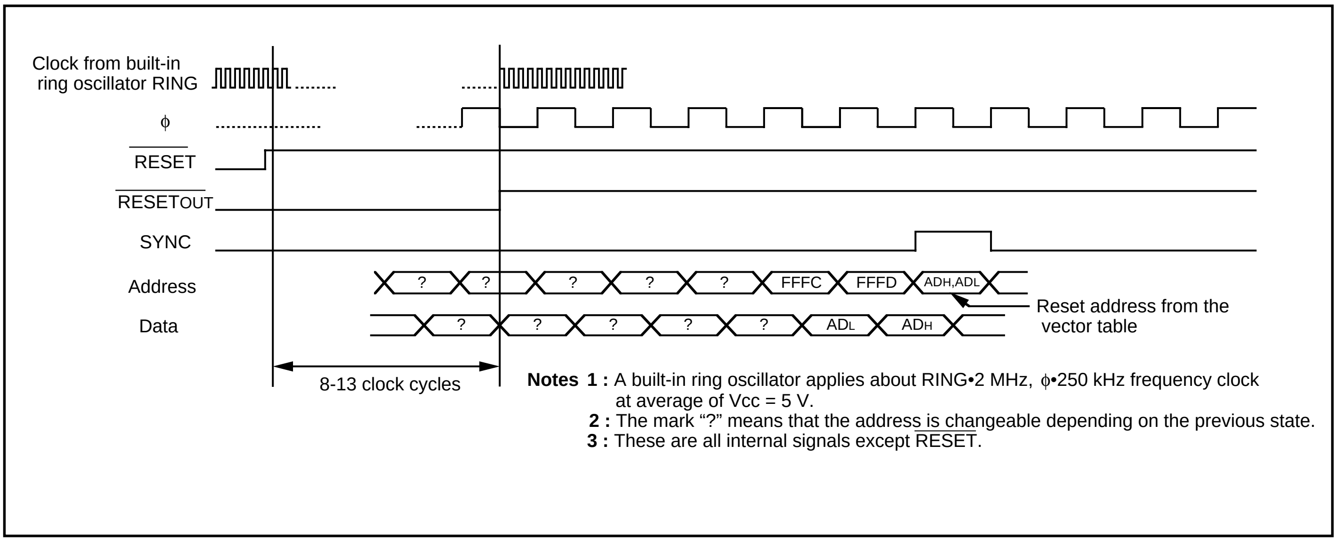


Fig. 69 Timing diagram at reset

	Register	Address	Register contents
(1)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(2)	Port P1 direction register (P1D)	0003_{16}	X X X 0 0 0 0 0
(3)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(4)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(5)	Interrupt source set register (INTSET)	$000A_{16}$	00_{16}
(6)	Interrupt source discrimination register (INTDIS)	$000B_{16}$	00_{16}
(7)	Compare register (low-order) (CMPL)	0010_{16}	00_{16}
(8)	Compare register (high-order) (CMPH)	0011_{16}	00_{16}
(9)	Capture/Compare register R/W pointer (CCRP)	0012_{16}	00_{16}
(10)	Capture software trigger register (CSTR)	0013_{16}	00_{16}
(11)	Compare register re-load register (CMPR)	0014_{16}	00_{16}
(12)	Port P0P3 drive capacity control register (DCCR)	0015_{16}	00_{16}
(13)	Pull-up control register (PULL)	0016_{16}	00_{16}
(14)	Port P1P3 control register (P1P3C)	0017_{16}	00_{16}
(15)	Serial I/O1 status register (SIO1STS)	0019_{16}	1 0 0 0 0 0 0 0
(16)	Serial I/O1 control register (SIO1CON)	$001A_{16}$	00_{16}
(17)	UART1 control register (UART1CON)	$001B_{16}$	1 1 1 0 0 0 0 0
(18)	Timer A, B mode register (TABM)	$001D_{16}$	00_{16}
(19)	Capture/Compare port register (CCPR)	$001E_{16}$	00_{16}
(20)	Timer source selection register (TMSR)	$001F_{16}$	00_{16}
(21)	Capture mode register (CAPM)	0020_{16}	00_{16}
(22)	Compare output mode register (CMOM)	0021_{16}	00_{16}
(23)	Capture/Compare status register (CCSR)	0022_{16}	00_{16}
(24)	Compare interrupt source register (CISR)	0023_{16}	00_{16}
(25)	Timer A (low-order) (TAL)	0024_{16}	FF_{16}
(26)	Timer A (high-order) (TAH)	0025_{16}	FF_{16}
(27)	Timer B (low-order) (TBL)	0026_{16}	FF_{16}
(28)	Timer B (high-order) (TBH)	0027_{16}	FF_{16}
(29)	Prescaler 1 (PRE1)	0028_{16}	FF_{16}
(30)	Timer 1 (T1)	0029_{16}	01_{16}
(31)	Timer count source set register (TCSS)	$002A_{16}$	00_{16}
(32)	Timer X mode register (TXM)	$002B_{16}$	00_{16}
(33)	Prescaler X (PREX)	$002C_{16}$	FF_{16}
(34)	Timer X (TX)	$002D_{16}$	FF_{16}
(35)	Serial I/O2 control register (SIO2STS)	$002F_{16}$	1 0 0 0 0 0 0 0
(36)	Serial I/O2 register (SIO2CON)	0030_{16}	00_{16}
(37)	UART2 control register (UART2CON)	0031_{16}	1 1 1 0 0 0 0 0
(38)	A-D control register (ADCON)	0034_{16}	0 0 0 1 0 0 0 0
(39)	Ring oscillation division ratio selection register (RODR)	0037_{16}	0 0 0 0 0 0 1 0
(40)	MISRG	0038_{16}	00_{16}
(41)	Watchdog timer control register (WDTCON)	0039_{16}	0 0 1 1 1 1 1 1
(42)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(43)	CPU mode register (CPUM)	$003B_{16}$	1 0 0 0 0 0 0 0
(44)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(45)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(46)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(47)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(48)	Flash memory control register 0 (FMCR0) (Note 3)	$0FE0_{16}$	0 0 0 0 0 0 0 1
(49)	Flash memory control register 1 (FMCR1) (Note 3)	$0FE1_{16}$	0 1 0 0 0 0 0 0
(50)	Processor status register	(PS)	X X X X X 1 X X
(51)	Program counter	(PC_H)	Contents of address $FFFD_{16}$
		(PC_L)	Contents of address $FFFC_{16}$

Notes 1: X : Undefined
2:The content of other registers is undefined when the microcomputer is reset.
The initial values must be surely set before you use it.
3:Only flash memory version has this register.

Fig. 70 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT}, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.
Use the circuit constants in accordance with the resonator manufacturer's recommended values.

(1) Ring oscillator operation
When the MCU operates by the ring oscillator for the main clock, connect X_{IN} pin to V_{CC} through a resistor and leave X_{OUT} pin open.
The clock frequency of the ring oscillator depends on the supply voltage and the operation temperature range.
Be careful that variable frequencies when designing application products.

(2) Ceramic resonator
When the ceramic resonator is used for the main clock, connect the ceramic resonator and the external circuit to pins X_{IN} and X_{OUT} at the shortest distance. A feedback resistor is built in between pins X_{IN} and X_{OUT}.

(3) RC oscillation
When the RC oscillation is used for the main clock, connect the X_{IN} pin and X_{OUT} pin to the external circuit of resistor R and the capacitor C at the shortest distance.
The frequency is affected by a capacitor, a resistor and a microcomputer.
So, set the constants within the range of the frequency limits.

(4) External clock
When the external signal clock is used for the main clock, connect the X_{IN} pin to the clock source and leave X_{OUT} pin open.
Select “0” (ceramic oscillation) to oscillation mode selection bit of CPU mode register ($003B_{16}$).

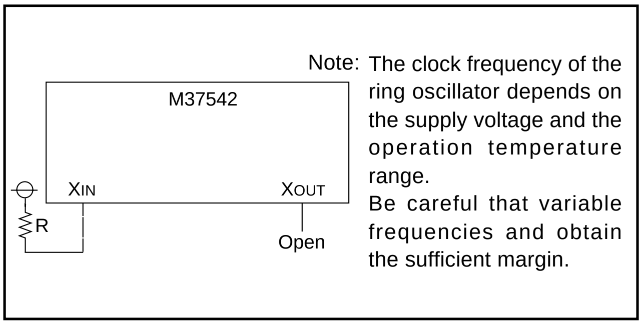


Fig. 71 Processing of X_{IN} and X_{OUT} pins at ring oscillator operation

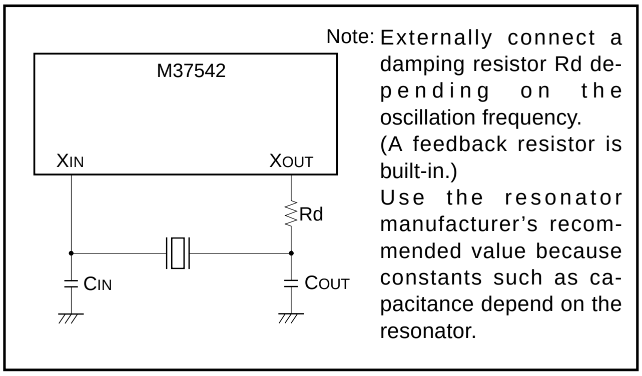


Fig. 72 External circuit of ceramic resonator

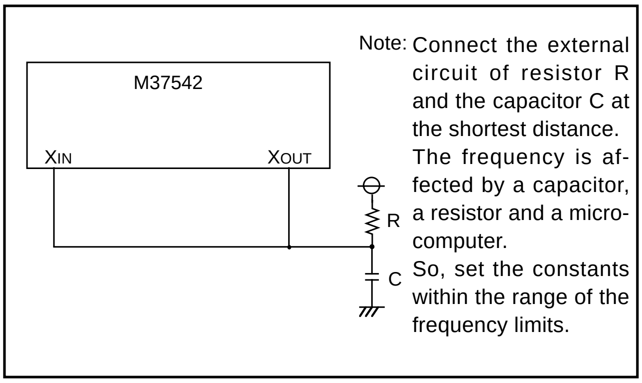


Fig. 73 External circuit of RC oscillation

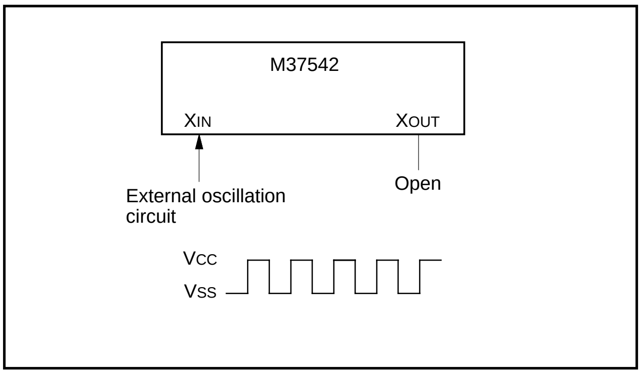


Fig. 74 External clock input circuit

(1) Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock ϕ stops at an “H” level and the XIN oscillator stops. At this time, timer 1 is set to “01_{16}” and prescaler 1 is set to “FF_{16}” when the oscillation stabilization time set bit after release of the STP instruction is “0”. On the other hand, timer 1 and prescaler 1 are not set when the above bit is “1”. Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. f(XIN)/16 is forcibly connected to the input of prescaler 1. When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at “H” until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an “L” level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable, or set the wait time by ring oscillator operation after system is released from reset until the oscillation is stabled.

With the FLASH version, the internal power supply circuit is changed to low power consumption mode for consumption current reduction at the time of STP instruction execution.

Although an internal power supply circuit is usually changed to the normal operation mode at the time of the return from an STP instruction, since a certain time is required to start the power supply to FLASH and operation of FLASH to be enabled, set wait time 100 µs or more with the FLASH version by the oscillation stabilization time set function after release of the STP instruction which used the timer 1.

• Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an “H” level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to “1” before the STP or WIT instruction is executed.

■ Notes on Clock Generating Circuit

For use with the oscillation stabilization set bit after release of the STP instruction set to “1”, set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

• Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

• Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

• CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU “M37542RSS” is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

• Clock division ratio, XIN oscillation control, ring oscillator control

The state transition shown in Fig. 79 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), ring oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 79.

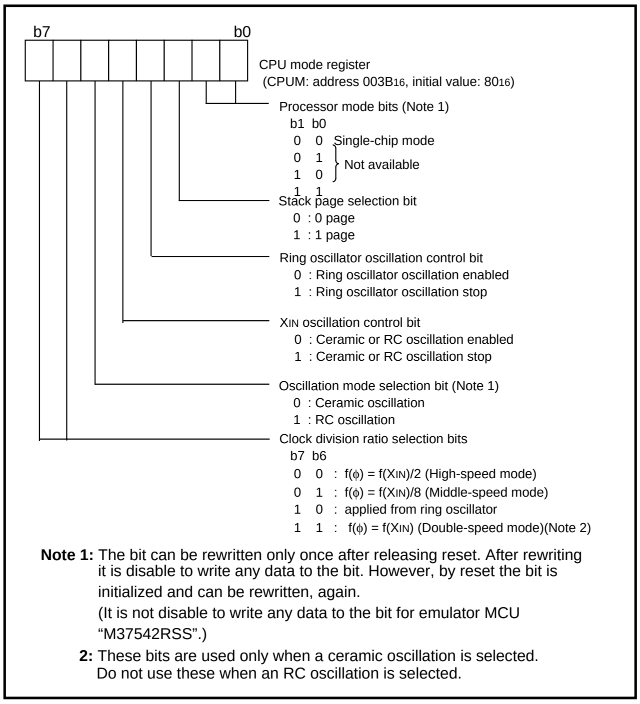


Fig. 75 Structure of CPU mode register

● Ring oscillation division ratio

At ring oscillator mode, division ratio of ring oscillator for CPU clock is selected by setting value of ring oscillation division ratio selection register. The division ratio of ring oscillation for CPU clock is selected from among 1/1, 1/2, 1/8, 1/128. The operation clock for the peripheral function block is not changed by setting value of this register.

■ Notes on Ring Oscillation Division Ratio

- When system is released from reset, ROSC/8 (ring middle-speed mode) is selected for CPU clock.
- When state transition from the ceramic or RC oscillation to ring oscillator, ROSC/8 (ring middle-speed mode) is selected for CPU clock.
- When the MCU operates by ring-oscillator for the main clock without external oscillation circuit, connect XIN pin to VCC through a resistor and leave XOUT pin open.
  Set “10010x00$_2$” (x = 0 or 1) to CPUM.

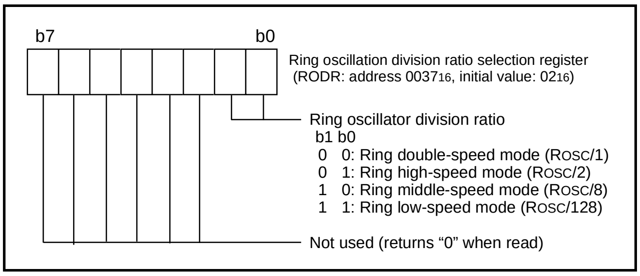


Fig. 76 Structure of ring oscillation division ratio selection register

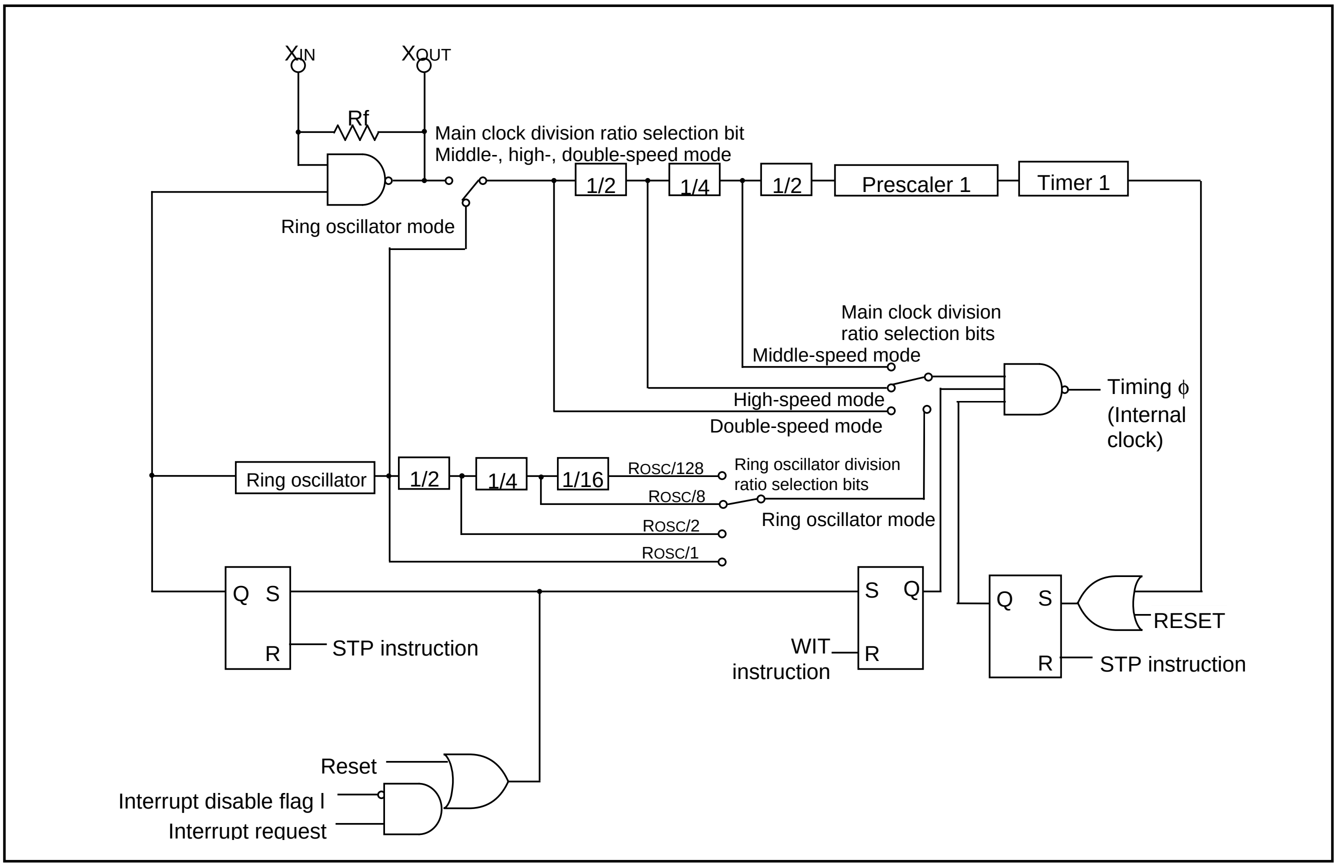


Fig. 77 Block diagram of internal clock generating circuit (for ceramic resonator)

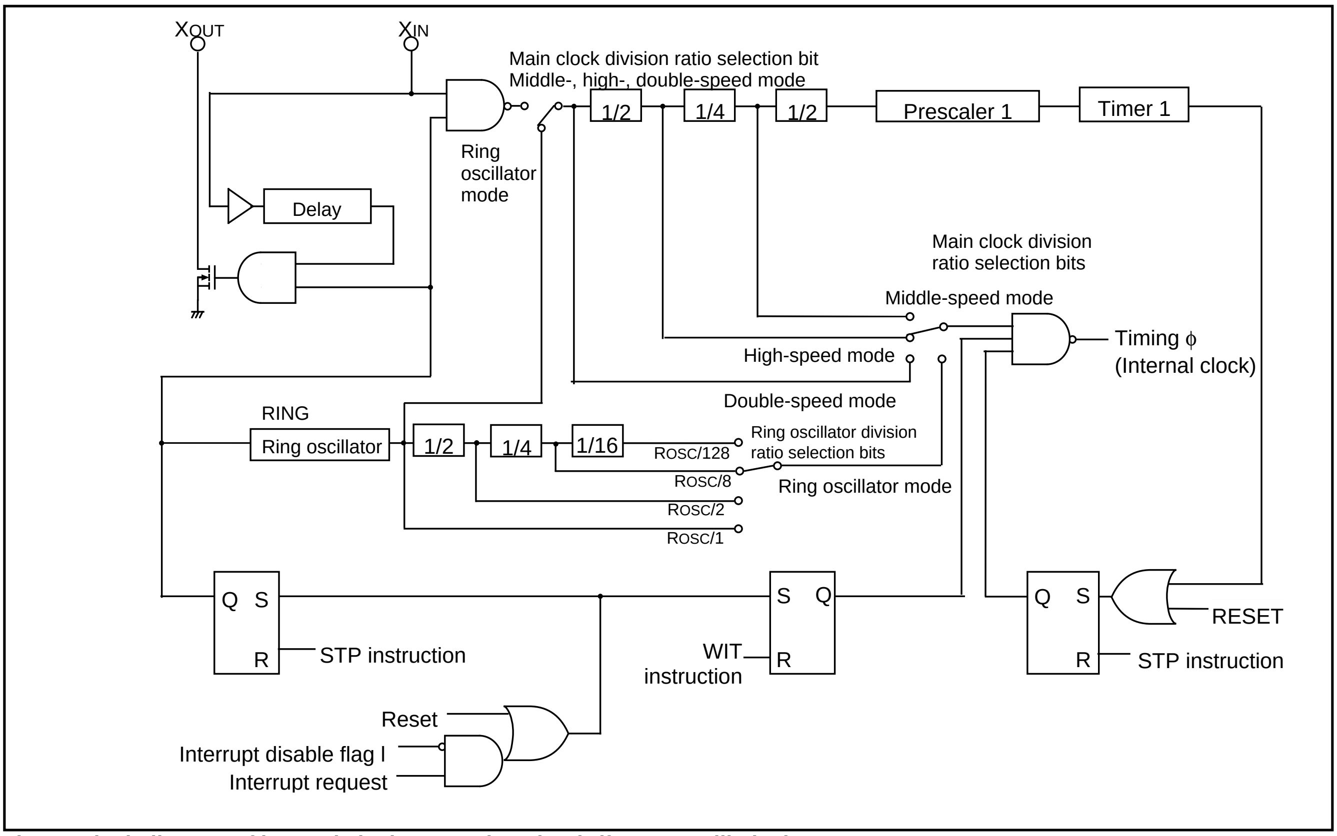
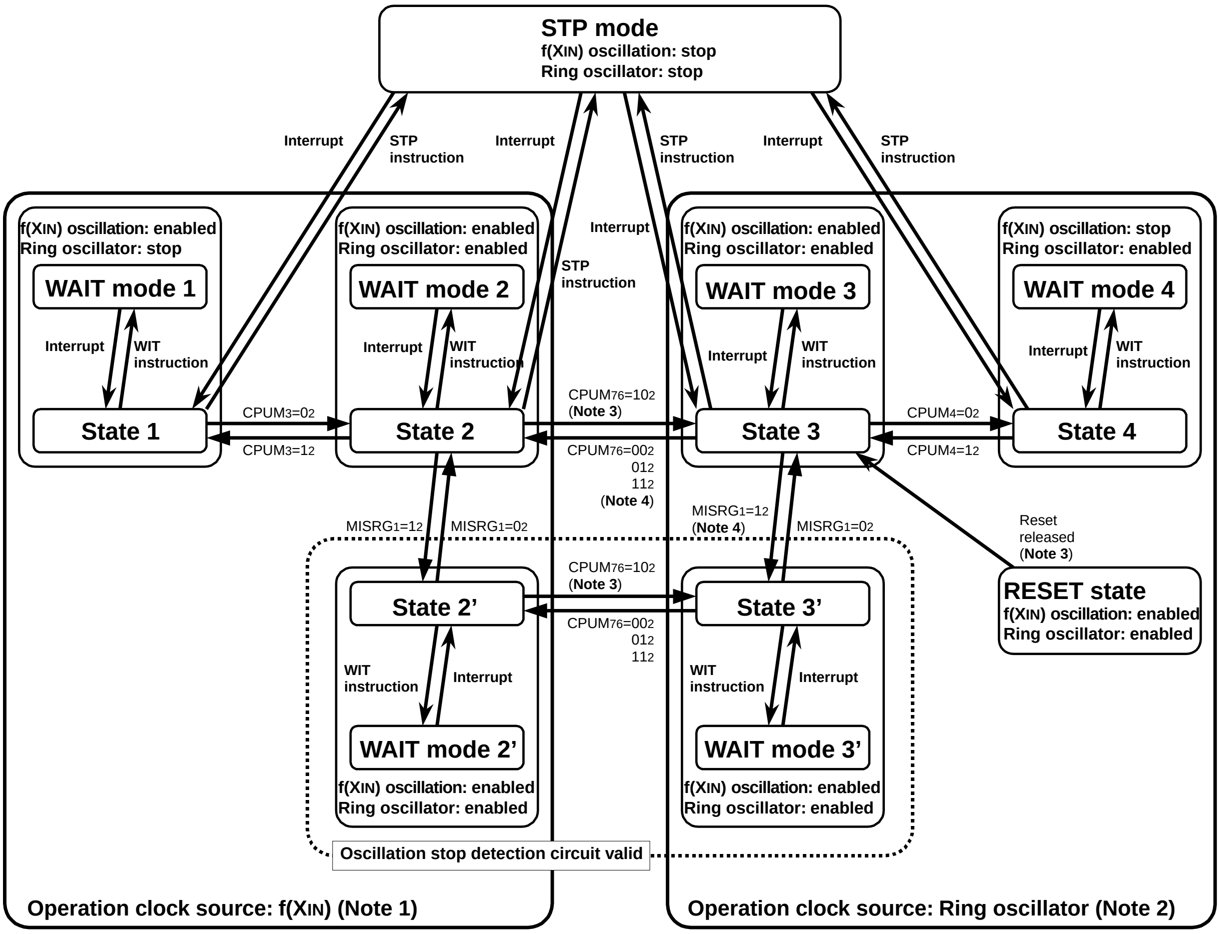


Fig. 78 Block diagram of internal clock generating circuit (for RC oscillation)



Notes on switch of clock

(1) In operation clock = f(XIN), the following can be selected for the CPU clock division ratio.
f(XIN)/2 (high-speed mode)
f(XIN)/8 (middle-speed mode)
f(XIN) (double-speed mode, only at a ceramic oscillation)

(2) In operation clock = ring oscillator, the following can be selected for the CPU clock division ratio.
ROSC/1 (ring double-speed mode)
ROSC/2 (ring high-speed mode)
ROSC/8 (ring middle-speed mode)
ROSC/128 (ring low-speed mode)

(3) After system is released from reset, and state transition of state 2 → state 3 and state transition of state 2' → state 3', ROSC/8 (ring middle-speed mode) is selected for CPU clock.

(4) Executing the state transition state 3 to 2 or state 3 to 3' after stabilizing XIN oscillation.

(5) When the state 2 → state 3 → state 4 is performed, execute the NOP instruction as shown below according to the division ratio of CPU clock.
1. $CPUM_{76} = 10_2$ (state 2 → state 3)
2. NOP instruction
   Double-speed mode: NOP × 3
   High-speed mode: NOP × 1
   Middle-speed mode: NOP × 0
3. $CPU_4 = 1_2$ (state 3 → state 4)

(6) When the state 3 → state 2 → state 1 is performed, execute the NOP instruction as shown below according to the division ratio of CPU clock.
1. $CPUM_{76} = 00_2$ or 01_2 or 11_2 (state 3 → state 2)
2. NOP instruction
   TBD
3. $CPU_3 = 1_2$ (state 2 → state 1)

Fig. 79 State transition

● Oscillation stop detection circuit

The oscillation stop detection circuit is used for reset occurrence when a ceramic resonator or RC oscillation circuit stops by disconnection. To use this circuit, set a built-in ring oscillator to be in active.

The oscillation stop detection circuit is in active to set “1” to the ceramic or RC oscillation stop detection function active bit. When the oscillation stop detection circuit is in active, ceramic or RC oscillation is watched by the built-in ring oscillator. When stop of ceramic or RC oscillation is detected, the oscillation stop detection status bit is set to “1”. While “1” is set to the oscillation stop reset bit, internal reset occurs when oscillation stop is detected.

The external reset and the oscillation stop reset can be discriminated by reading the oscillation stop detection status bit.
The oscillation stop detection status bit retains “1”, not initialized, when the oscillation stop reset occurs. The oscillation stop detection status bit is initialized to “0” when the external reset occurs. Accordingly, reset by oscillation stop can be confirmed by using this bit.

■ Notes on Oscillation Stop Detection Circuit

- Do not execute the transition to “state 2’a” shown in Figure 81 because in this “state 2’a”, MCU is stopped without reset even when X_{IN} oscillation is stopped.
- Ceramic or RC oscillation stop detection function active bit is not cleared by the oscillation stop internal reset. Accordingly, the oscillation stop detection circuit is in active when system is released from internal reset cause of oscillation stop detection.
- Oscillation stop detection status bit is initialized by the following operation.
  (1) External reset
  (2) Write “0” data to the ceramic or RC oscillation stop detection function active bit.
- The oscillation stop detection circuit is not included in the emulator MCU “M37542RSS”.

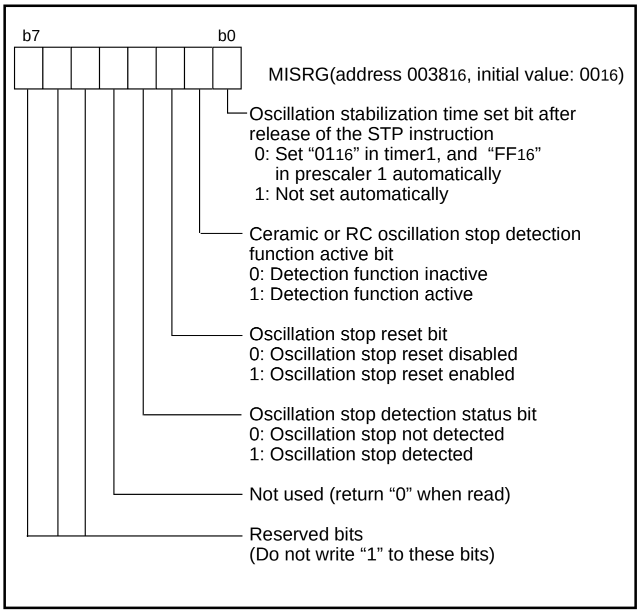
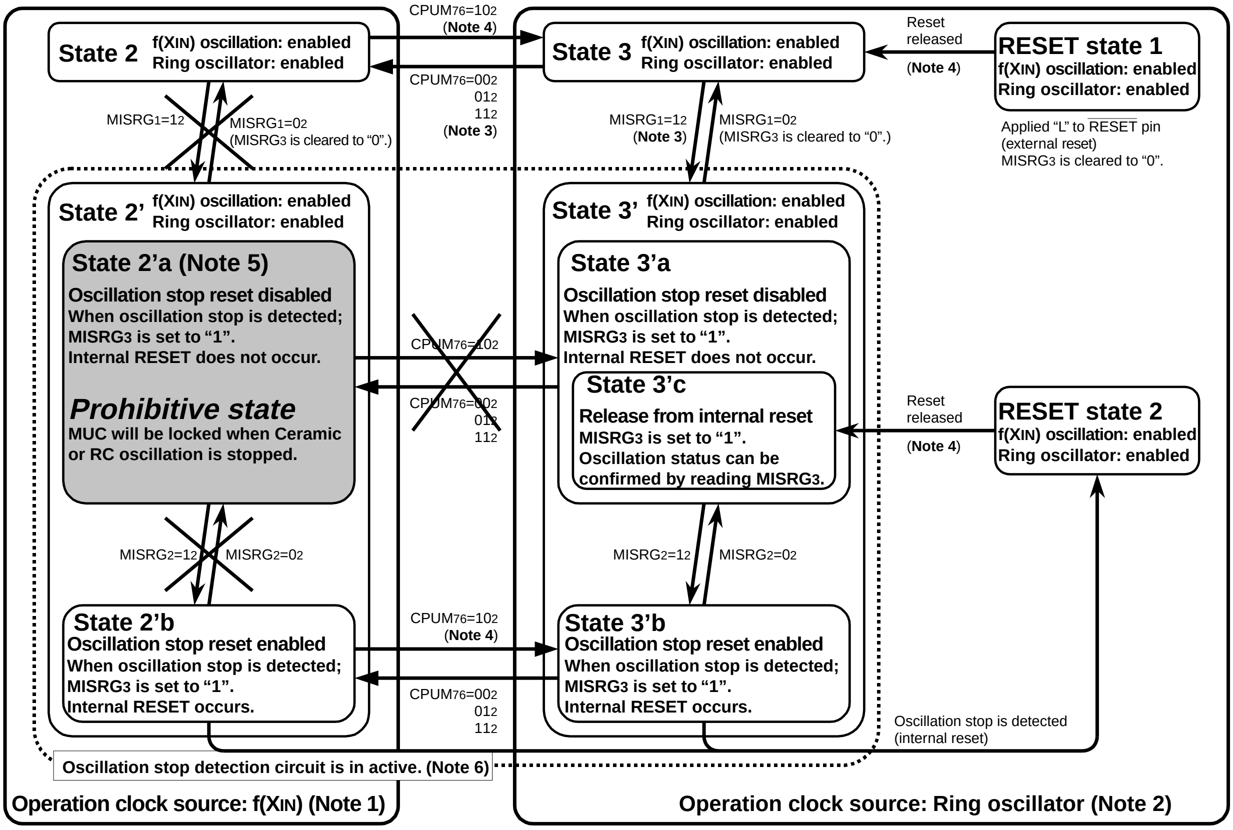


Fig. 80 Structure of MISRG



Notes on switch of clock

(1) In operation clock = f(XIN), the following can be selected for the CPU clock division ratio.
f(XIN)/2 (high-speed mode)
f(XIN)/8 (middle-speed mode)
f(XIN) (double-speed mode, only at a ceramic oscillation)

(2) In operation clock = ring oscillator, the following can be selected for the CPU clock division ratio.
ROSC/1 (ring double-speed mode)
ROSC/2 (ring high-speed mode)
ROSC/8 (ring middle-speed mode)
ROSC/128 (ring low-speed mode)

(3) Executing the state transition state 3 to 2 or state 3 to 3' after stabilizing XIN oscillation.

(4) After system is released from reset, and state transition of state 2 → state 3 and state transition of state 2' → state 3', ROSC/8 (ring middle-speed mode) is selected for CPU clock.

(5) MCU cannot be returned by ring oscillator and its operation is stopped since internal reset does not occur at oscillation stop detected. Accordingly, do not execute the transition to state 2'a.

(6) STP instruction cannot be used when oscillation stop detection circuit is in active.

Fig. 81 State transition 2

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

• For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
• In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Ports

• The values of the port direction registers cannot be read.
That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
For setting direction registers, use the LDM instruction, STA instruction, etc.

A-D Conversion

Do not execute the STP instruction during A-D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock ϕ is the same as that of the X_{IN} in double-speed mode, twice the X_{IN} cycle in high-speed mode and 8 times the X_{IN} cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit and processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)
When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

State transition

Do not stop the clock selected as the operation clock because of setting of CM3, 4.

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF to 0.1 µF is recommended.

NOTES ON PERIPHERAL FUNCTIONS

■ Interrupt

(1) When setting the followings, the interrupt request bit may be set to "1".
•When setting external interrupt active edge
Related register:
Interrupt edge selection register (address $003A_{16}$)
Timer X mode register (address $002B_{16}$)
Capture mode register (address 0020_{16})

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
① Set the corresponding interrupt enable bit to "0" (disabled).
② Set the interrupt edge select bit (active edge switch bit, trigger mode bit).
③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to "1" (enabled).

(2) Use a LDM instruction to cleare an interrupt discrimination bit.
LDM #$0n, $0Bn
Set the following values to "n"
"0": an interrupt discrimination bit to clear
"1": other interrupt discrimination bits
Ex.) When a key-on wakeup interrupt discrimination bit is cleared;
LDM #00001110B and $0B.

■ Timers

• When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
• When a count source of timer X, timer Y or timer Z is switched, stop a count of timer X.

■ Timer X

(1) $CNTR_0$ interrupt active edge selection-1
$CNTR_0$ interrupt active edge depends on the $CNTR_0$ active edge switch bit.
When this bit is "0", the $CNTR_0$ interrupt request bit is set to "1" at the falling edge of $CNTR_0$ pin input signal. When this bit is "1", the $CNTR_0$ interrupt request bit is set to "1" at the rising edge of $CNTR_0$ pin input signal.

(2) $CNTR_0$ interrupt active edge selection-2
According to the setting value of $CNTR_0$ active edge switch bit, the interrupt request bit may be set to "1".
When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
① Set the corresponding interrupt enable bit to "0" (disabled).
② Set the active edge switch bit.
③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to "1" (enabled).

■ Notes on Timer A, B

(1) Setting of timer value
When "1: Write to only latch" is set to the timer A (B) write control bit, written data to timer register is set to only latch even if timer is stopped. Accordingly, in order to set the initial value for timer when it is stopped, set "0: Write to latch and timer simultaneously" to timer A (B) write control bit.

(2) Read/write of timer A
Stop timer A to read/write its data when the system is in the following state;
• CPU operation clock source: X_{IN} oscillation
• Timer A count source: Ring oscillator output

(3) Read/write of timer B
Stop timer B to read/write its data when the system is in the following state;
• CPU operation clock source: X_{IN} oscillation
• Timer B count source: Timer A underflow
• Timer A count source: Ring oscillator output

■ Notes on Output Compare

• When the selected source timer of each compare channel is stopped, written data to compare register is loaded to the compare latch simultaneously.
• Do not write the same data to both of compare latch x0 and x1.
• When setting value of the compare latch is larger than timer setting value, compare match signal is not generated. Accordingly, the output waveform is fixed to "L" or "H" level.
However, when setting value of another compare latch is smaller than timer setting value, this compare match signal is generated. Accordingly, compare match interrupt occurs.
• When the compare x trigger enable bit is cleared to "0" (disabled), the match trigger to the waveform output circuit is disabled, and the output waveform can be fixed to "L" or "H" level.
However, in this case, the compare match signal is generated. Accordingly, compare match interrupt occurs.

■ Notes on Input Capture

• If the capture trigger is input while the capture register (low-order and high-order) is in read, captured value is changed between high-order reading and low-order reading. Accordingly, some countermeasure by software is recommended, for example comparing the values that twice of read.
• When the ring-oscillator is selected for Timer A count source, Timer A cannot be used for the capture source timer.
Timer B cannot be used for the capture source timer when the system is in the following state;
  • CPU operation clock source: X_{IN} oscillation
  • Timer B count source: Timer A underflow
  • Timer A count source: Ring oscillator output
• When writing "1" to capture latch x0 (x1) software trigger bit of capture latch x0 and x1 at the same time, or external trigger and software trigger occur simultaneously, the set value of capture x status bit is undefined.
• When setting the interrupt active edge selection bit and noise filter clock selection bit of external interrupt CAP_0, CAP_1, the interrupt request bit may be set to "1".
When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.
① Set the corresponding interrupt enable bit to "0" (disabled).
② Set the interrupt edge selection bit or noise filter clock selection bit.
③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
④ Set the corresponding interrupt enable bit to "1" (enabled).
• The capture interrupt cannot be used as the interrupt for return from stop mode. Even when the valid edge of the capture interrupt is input at stop mode, system retains the stop mode. Then, system returns from stop mode by other external interrupts, the capture interrupt is accepted.
In this case, after system returns from stop mode, the interrupt request bit of the corresponding capture interrupt is set to "1".

■ Notes on Serial I/O1

• Serial I/O interrupt

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

① Set the serial I/O transmit interrupt enable bit to “0” (disabled).
② Set the transmit enable bit to “1”.
③ Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
⑤ Set the serial I/O transmit interrupt enable bit to “1” (enabled).

• I/O pin function when serial I/O1 is enabled.

The functions of $P1_2$ and $P1_3$ are switched with the setting values of a serial I/O1 mode selection bit and a serial I/O1 synchronous clock selection bit as follows.

(1) Serial I/O1 mode selection bit → “1” :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O1 synchronous clock selection bit
“0” : $P1_2$ pin turns into an output pin of a synchronous clock.
“1” : $P1_2$ pin turns into an input pin of a synchronous clock.
Setup of a $\overline{S_{RDY1}}$ output enable bit (SRDY)
“0” : $P1_3$ pin can be used as a normal I/O pin.
“1” : $P1_3$ pin turns into a $\overline{S_{RDY1}}$ output pin.

(2) Serial I/O1 mode selection bit → “0” :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O1 synchronous clock selection bit
“0”: $P1_2$ pin can be used as a normal I/O pin.
“1”: $P1_2$ pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is $P1_3$ pin. It can be used as a normal I/O pin.

• Bus collision detection

Bus collision detection can be used when SIO1 is operating at full-duplex communication. When SIO1 is operating at half-duplex communication, set bus collision detection interrupt to be disabled.

■ Notes on Serial I/O2

• Serial I/O interrupt

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

① Set the serial I/O transmit interrupt enable bit to “0” (disabled).
② Set the transmit enable bit to “1”.
③ Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
⑤ Set the serial I/O transmit interrupt enable bit to “1” (enabled).

• I/O pin function when serial I/O2 is enabled.

The functions of $P0_6$ and $P0_7$ are switched with the setting values of a serial I/O2 mode selection bit and a serial I/O2 synchronous clock selection bit as follows.

(1) Serial I/O2 mode selection bit → “1” :
Clock synchronous type serial I/O is selected.
Setup of a serial I/O2 synchronous clock selection bit
“0” : $P0_6$ pin turns into an output pin of a synchronous clock.
“1” : $P0_6$ pin turns into an input pin of a synchronous clock.
Setup of a $\overline{S_{RDY2}}$ output enable bit (SRDY)
“0” : $P0_7$ pin can be used as a normal I/O pin.
“1” : $P0_7$ pin turns into a $\overline{S_{RDY2}}$ output pin.

(2) Serial I/O2 mode selection bit → “0” :
Clock asynchronous (UART) type serial I/O is selected.
Setup of a serial I/O2 synchronous clock selection bit
“0”: $P0_6$ pin can be used as a normal I/O pin.
“1”: $P0_6$ pin turns into an input pin of an external clock.
When clock asynchronous (UART) type serial I/O is selected, it is $P0_7$ pin. It can be used as a normal I/O pin.

■ A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that $f(X_{IN})$ is 500kHz or more during A-D conversion.

■ Notes on Clock Generating Circuit

For use with the oscillation stabilization set bit after release of the STP instruction set to “1”, set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

• Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

• Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

• CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU “M37542RSS” is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

• Clock division ratio, X_{IN} oscillation control, ring oscillator control

The state transition shown in Fig. 79 can be performed by setting the clock division ratio selection bits (bits 7 and 6), X_{IN} oscillation control bit (bit 4), ring oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 79.

■ Notes on Ring Oscillation Division Ratio

• When system is released from reset, R_{OSC}/8 (ring middle-speed mode) is selected for CPU clock.
• When state transition from the ceramic or RC oscillation to ring oscillator, R_{OSC}/8 (ring middle-speed mode) is selected for CPU clock.
• When the MCU operates by ring-oscillator for the main clock without external oscillation circuit, connect X_{IN} pin to V_{CC} through a resistor and leave X_{OUT} pin open.
  Set “10010x00$_2$” (x = 0 or 1) to CPUM.

■ Notes on Oscillation Stop Detection Circuit

• When the oscillation stop reset bit is set to “0”, internal reset does not occur. If the ceramic or RC oscillation is selected for the CPU clock, MCU will be locked when the ceramic or RC oscillation is stopped. So when the ceramic or RC oscillation is selected for the main clock, set the oscillation stop reset bit to “1”. (State 2’a of Fig. 81)
• Ceramic or RC oscillation stop detection function active bit is not cleared by the oscillation stop internal reset. Accordingly, the oscillation stop detection circuit is in active when system is released from internal reset cause of oscillation stop detection.
• Oscillation stop detection status bit is initialized by the following operation.
  (1) External reset
  (2) Write “0” data to the ceramic or RC oscillation stop detection function active bit.
• The oscillation stop detection circuit is not included in the emulator MCU “M37542RSS”.

■ Notes on CPU Rewrite Mode

Take the notes described below when rewriting the flash memory in CPU rewrite mode.

●Operation speed

During CPU rewrite mode, set the system clock ϕ to 4.0 MHz or less using the clock division ratio selection bits (bits 6 and 7 of address 003B$_{16}$).

●Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode.

●Interrupts inhibited against use

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

●Watchdog timer

If the watchdog timer has been already activated, internal reset due to an underflow will not occur because the watchdog timer is surely cleared during program or erase.

●Reset

Reset is always valid. The MCU is activated using the boot mode at release of reset in the condition of CNVss = “H”, so that the program will begin at the address which is stored in addresses FFFC$_{16}$ and FFFD$_{16}$ of the boot ROM area.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1.Mask ROM Order Confirmation Form *
2.Mark Specification Form *
3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

For the mask ROM confirmation and the mark specifications, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/en/rom).

FLASH MEMORY MODE

The 7542 group's flash memory version has the flash memory that can be rewritten with a single power source.
For this flash memory, three flash memory modes are available in which to read, program, and erase: the parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and the CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU).

● Summary

Table 7 lists the summary of the 7542 Group (flash memory version).

This flash memory version has some blocks on the flash memory as shown in Figure 82 and each block can be erased.
In addition to the ordinary User ROM area to store the MCU operation control program, the flash memory has a Boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

Table 7 Summary of 7542 group's flash memory version

Item		Specifications
Power source voltage (Vcc)		V_{CC} = 2.7 to 5.5 V
Program/Erase V_{PP} voltage (V_{PP})		V_{CC} = 2.7 to 5.5 V
Flash memory mode		3 modes; Parallel I/O mode, Standard serial I/O mode, CPU rewrite mode
Erase block division	User ROM area/Data ROM area	Refer to Fig. 82.
	Boot ROM area (Note)	Not divided (4K bytes)
Program method		In units of bytes
Erase method		Block erase
Program/Erase control method		Program/Erase control by software command
Number of commands		5 commands
Number of program/Erase times		TBD
ROM code protection		Available in parallel I/O mode and standard serial I/O mode

Note: The Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory.
This Boot ROM area can be erased and written in only parallel I/O mode.

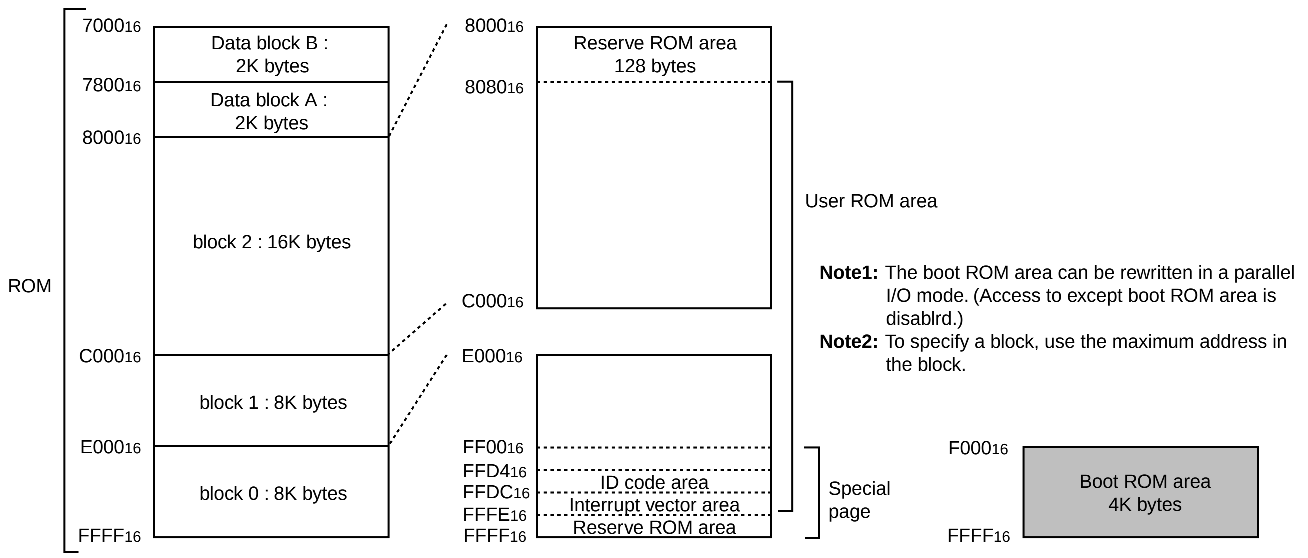


Fig. 82 Block diagram of built-in flash memory

● Boot Mode

The control program for CPU rewrite mode must be written into the User ROM or Boot ROM area in parallel I/O mode beforehand. (If the control program is written into the Boot ROM area, the standard serial I/O mode becomes unusable.)
See Figure 82 for details about the Boot ROM area.
Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVSS pin low. In this case, the CPU starts operating using the control program in the User ROM area.
When the microcomputer is reset and the CNVSS pin high after pulling the $P3_7$(RP) pin low, $P3_2$(CE) pin high, $P0_6$/SCLK pin low and $P0_5$/TxD_2 pin high, the CPU starts operating (start address of program is stored into addresses $FFFC_{16}$ and $FFFD_{16}$) using the control program in the Boot ROM area. This mode is called the "Boot mode". Also, User ROM area can be rewritten using the control program in the Boot ROM area.

● Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command.

● CPU Rewrite Mode

In CPU rewrite mode, the internal flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).
In CPU rewrite mode, only the User ROM area shown in Figure 82 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the User ROM area and each block area.
The control program for CPU rewrite mode can be stored in either User ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area before it can be executed.

• Outline Performance

CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten.
In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This rewrite control program must be transferred to internal RAM area before it can be executed.
The MCU enters CPU rewrite mode by setting “1” to the CPU rewrite mode select bit (bit 1 of address $0FE0_{16}$). Then, software commands can be accepted.
Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 83 shows the flash memory control register 0.
Bit 0 of the flash memory control register 0 is the RY/$\overline{BY}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is “0” (busy). Otherwise, it is “1” (ready).
Bit 1 of the flash memory control register 0 is the CPU rewrite mode select bit. When this bit is set to “1”, the MCU enters CPU rewrite mode. And then, software commands can be accepted. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in the internal RAM for write to bit 1. To set this bit 1 to “1”, it is necessary to write “0” and then write “1” in succession to bit 1. The bit can be set to “0” by only writing “0”.
Bit 2 of the flash memory control register 0 is the 8KB user block E/W mode disable bit. When this bit is set to “0”, CPU rewriting to block 0 and block 1 of FLASH is disabled.
Bit 3 of the flash memory control register 0 is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when exiting CPU rewrite mode and when flash memory access has failed. When the CPU rewrite mode select bit is “1”, setting “1” for this bit resets the control circuit. To release the reset, it is necessary to set this bit to “0”.
Bit 5 of the flash memory control register 0 is the User ROM area select bit and is valid only in the boot mode. Setting this bit to “1” in the boot mode switches an accessible area from the boot ROM area to the user ROM area. To use the CPU rewrite mode in the boot mode, set this bit to “1”. Note that when the microcomputer is booted up in the user ROM area, only the user ROM area is accessible and bit 5 is invalid; on the other hand, when the microcomputer is in the boot mode, bit 5 is valid independent of the CPU rewrite mode. To rewrite bit 5, execute the user-original reprogramming control software transferred to the internal RAM in advance.
Bit 6 of the flash memory control register 0 is the program status flag. This bit is set to “1” when writing to flash memory is failed. When program error occurs, the block cannot be used.
Bit 7 of the flash memory control register 0 is the erase status flag. This bit is set to “1” when erasing flash memory is failed. When erase error occurs, the block cannot be used.

Figure 84 shows the flash memory control register 1.
Bit 0 of the flash memory control register 1 is the Erase suspend enable bit. By setting this bit to “1”, the erase suspend mode to suspend erase processing temporaly when block erase command is executed can be used. In order to set this bit to “1”, writing “0” and “1” in succession to bit 0. In order to set this bit to “0”, write “0” only to bit 0.
Bit 1 of the flash memory control register 1 is the erase suspend request bit. By setting this bit to “1” when erase suspend enable bit is “1”, the erase processing is suspended.
Bit 6 of the flash memory control register 1 is the erase suspend flag. This bit is cleared to “0” at the flash erasing.

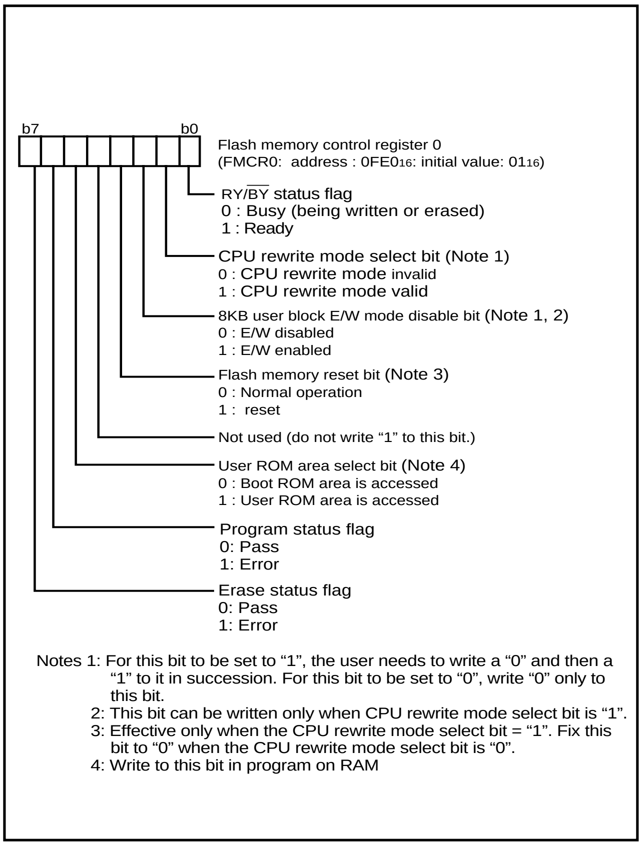


Fig. 83 Structure of flash memory control register 0

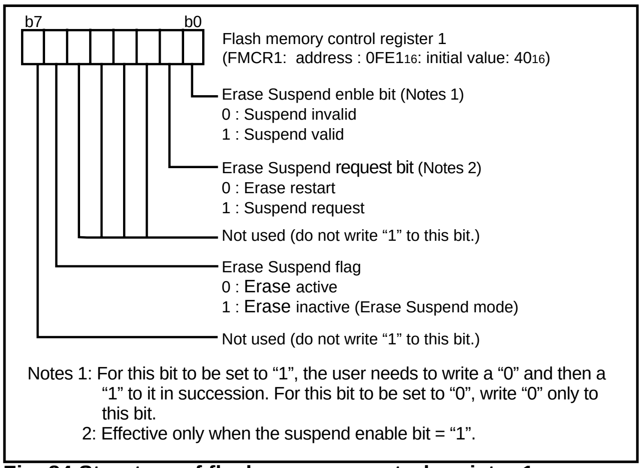
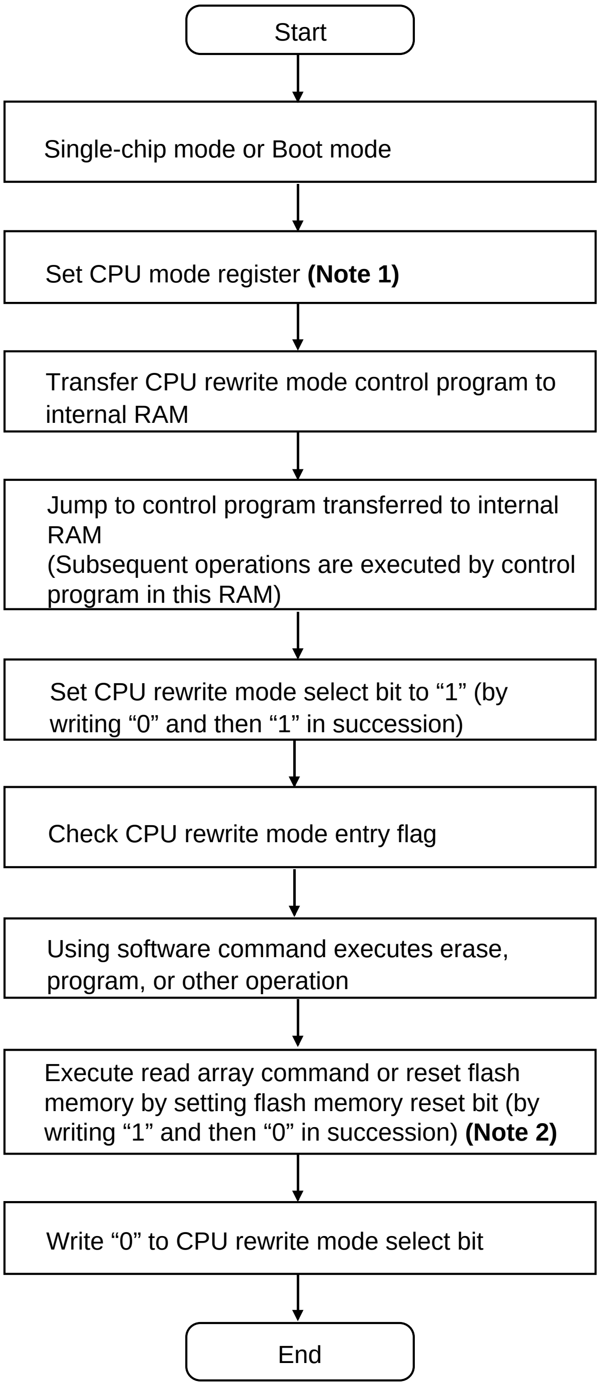


Fig. 84 Structure of flash memory control register 1

Figure 85 shows a flowchart for setting/releasing CPU rewrite mode.



Notes **1**: Set the main clock as follows depending on the clock division ratio selection bits of CPU mode register (bits 6, 7 of address $003B_{16}$).

2: Before exiting the CPU rewrite mode after completing erase or program operation, always be sure to execute the read array command or reset the flash memory.

Fig. 85 CPU rewrite mode set/release flowchart

■ Notes on CPU Rewrite Mode

Take the notes described below when rewriting the flash memory in CPU rewrite mode.

●Operation speed

During CPU rewrite mode, set the system clock ϕ to 4.0 MHz or less using the clock division ratio selection bits (bits 6 and 7 of address $003B_{16}$).

●Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode.

●Interrupts inhibited against use

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

●Watchdog timer

If the watchdog timer has been already activated, internal reset due to an underflow will not occur because the watchdog timer is surely cleared during program or erase.

●Reset

Reset is always valid. The MCU is activated using the boot mode at release of reset in the condition of CNVss = “H”, so that the program will begin at the address which is stored in addresses $FFFC_{16}$ and $FFFD_{16}$ of the boot ROM area.

● Software Commands

Table 8 lists the software commands.
After setting the CPU rewrite mode select bit to “1”, execute a software command to specify an erase or program operation.
Each software command is explained below.

• Read Array Command (FF16)
The read array mode is entered by writing the command code “FF16” in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D_0 to D_7).
The read array mode is retained until another command is written.

• Read Status Register Command (7016)
When the command code “7016” is written in the first bus cycle, the contents of the status register are read out at the data bus (D_0 to D_7) by a read in the second bus cycle.
The status register is explained in the next section.

• Clear Status Register Command (5016)
This command is used to clear the bits SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code “5016” in the first bus cycle.

• Program Command (4016)
Program operation starts when the command code “4016” is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.
Whether the write operation is completed can be confirmed by read status register or the RY/$\overline{BY}$ status flag. When the program starts, the read status register mode is entered automatically and the contents of the status register is read at the data bus (D_0 to D_7). The status register bit 7 (SR7) is set to “0” at the same time the write operation starts and is returned to “1” upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF16) is written.

The RY/$\overline{BY}$ status flag of the flash memory control register is “0” during write operation and “1” when the write operation is completed as is the status register bit 7.
At program end, program results can be checked by reading the status register.

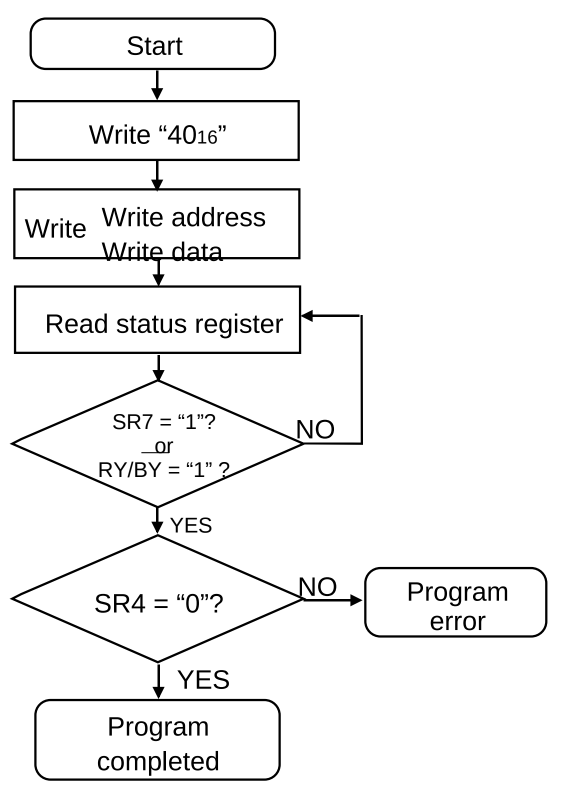


Fig. 86 Program flowchart

Table 8 List of software commands (CPU rewrite mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X **(Note 4)**	FF16			
Read status register	2	Write	X	7016	Read	X	SRD **(Note 1)**
Clear status register	1	Write	X	5016			
Program	2	Write	X	4016	Write	WA **(Note 2)**	WD **(Note 2)**
Block erase	2	Write	X	2016	Write	BA **(Note 3)**	D016

Notes 1: SRD = Status Register Data
2: WA = Write Address, WD = Write Data
3: BA = Block Address to be erased (Input the maximum address of each block.)
4: X denotes a given address in the User ROM area.

• Block Erase Command (20₁₆/D0₁₆)

By writing the command code "2016" in the first bus cycle and the confirmation command code "D016" and the block address in the second bus cycle that follows, the block erase (erase and erase verify) operation starts for the block address of the flash memory to be specified.

Whether the block erase operation is completed can be confirmed by read status register or the RY/$\overline{BY}$ status flag of flash memory control register. At the same time the block erase operation starts, the read status register mode is automatically entered, so that the contents of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF16) is written.

The RY/$\overline{BY}$ status flag is "0" during block erase operation and "1" when the block erase operation is completed as is the status register bit 7.

After the block erase ends, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

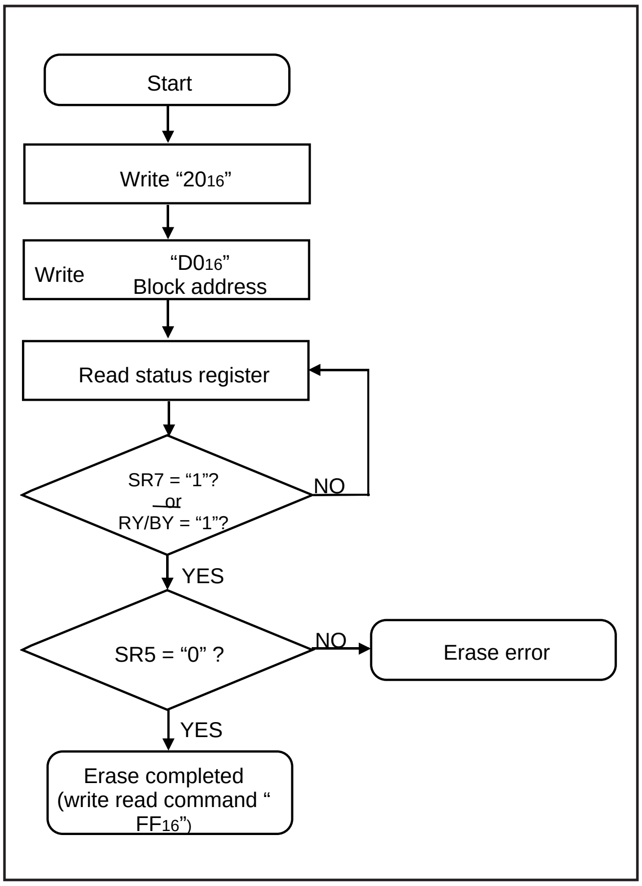


Fig. 87 Erase flowchart

● Status Register

The status register shows the operating status of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways:

(1) By reading an arbitrary address from the User ROM area after writing the read status register command (70_{16})
(2) By reading an arbitrary address from the User ROM area in the period from when the program starts or erase operation starts to when the read array command (FF_{16}) is input.

Also, the status register can be cleared by writing the clear status register command (50_{16}).
After reset, the status register is set to "80_{16}".
Table 9 shows the status register. Each bit in this register is explained below.

•Sequencer status (SR7)
The sequencer status indicates the operating status of the flash memory. This bit is set to "0" (busy) during write or erase operation and is set to "1" when these operations ends.
After power-on, the sequencer status is set to "1" (ready).

•Erase status (SR5)
The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is reset to "0".

•Program status (SR4)
The program status indicates the operating status of write operation. When a write error occurs, it is set to "1".
The program status is reset to "0" when it is cleared.

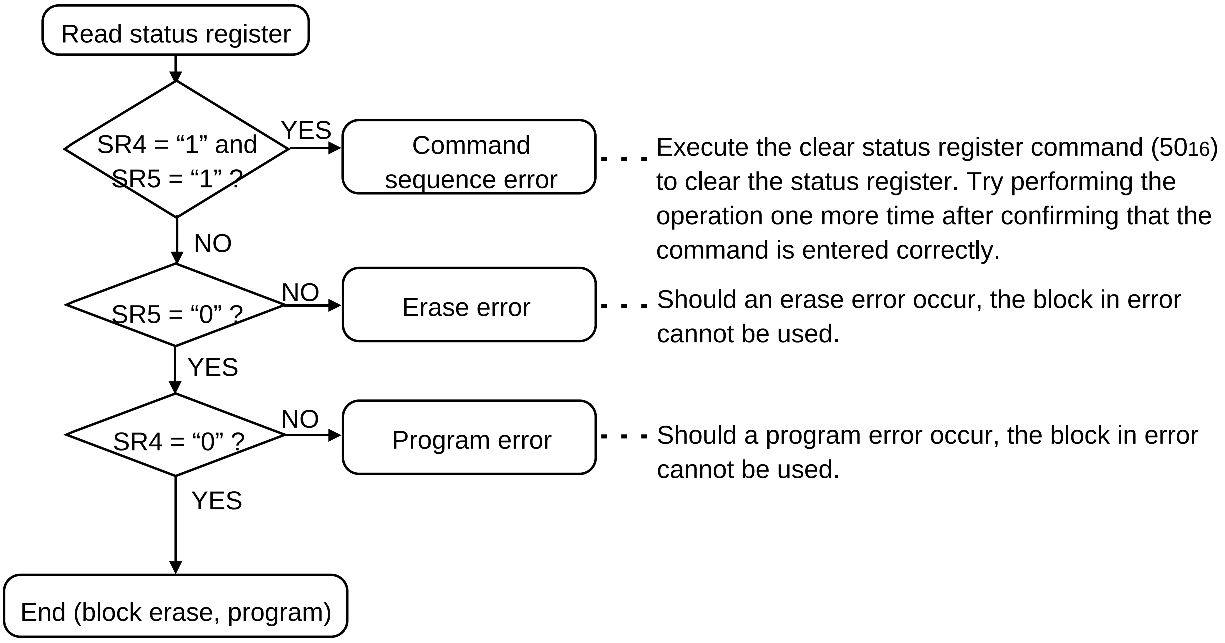
If "1" is written for any of the SR5 and SR4 bits, the read array, program, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.
Also, if any commands are not correct, both SR5 and SR4 are set to "1".

Table 9 Definition of each bit in status register

Each bit of SRD bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

● Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 88 shows a full status check flowchart and the action to be taken when each error occurs.



Note: When one of SR5 and SR4 is set to “1”, none of the read array, program, and block erase commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 88 Full status check flowchart and remedial procedure for errors

● Functions To Inhibit Rewriting Flash Memory Version

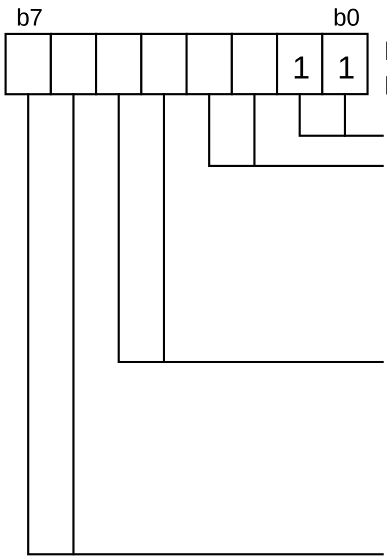
To prevent the contents of internal flash memory from being read out or rewritten easily, this MCU incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

(1) ROM Code Protect Function

The ROM code protect function is the function to inhibit reading out or modifying the contents of internal flash memory by using the ROM code protect control address (address $FFDB_{16}$) in parallel I/O mode. Figure 89 shows the ROM code protect control address (address $FFDB_{16}$). (This address exists in the User ROM area.)

If one or both of the pair of ROM code protect bits is set to “0”, the ROM code protect is turned on, so that the contents of internal flash memory are protected against readout and modification. The ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM code protect reset bits are set to “00”, the ROM code protect is turned off, so that the contents of internal flash memory can be readout or modified. Once the ROM code protect is turned on, the contents of the ROM code protect reset bits cannot be modified in parallel I/O mode. Use the serial I/O or CPU rewrite mode to rewrite the contents of the ROM code protect reset bits.



ROM code protect control address (address $FFDB_{16}$)
ROMCP (FF_{16} when shipped)

Reserved bits (“1” at read/write)

ROM code protect level 2 set bits (ROMCP2) (**Notes 1, 2**)
b3b2
0 0: Protect enabled
0 1: Protect enabled
1 0: Protect enabled
1 1: Protect disabled

ROM code protect reset bits (**Note 3**)
b5b4
0 0: Protect removed
0 1: Protect set bits effective
1 0: Protect set bits effective
1 1: Protect set bits effective

ROM code protect level 1 set bits (ROMCP1) (**Note 1**)
b7b6
0 0: Protect enabled
0 1: Protect enabled
1 0: Protect enabled
1 1: Protect disabled

Notes
1: When ROM code protect is turned on, the internal flash memory is protected against readout or modification in parallel I/O mode.
2: When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.
3: The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2. However, since these bits cannot be modified in parallel I/O mode, they need to be rewritten in serial I/O mode or CPU rewrite mode.

Fig. 89 Structure of ROM code protect control address

(2) ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the programmer is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, and its areas are $FFD4_{16}$ to $FFDA_{16}$. Write a program which has had the ID code preset at these addresses to the flash memory.

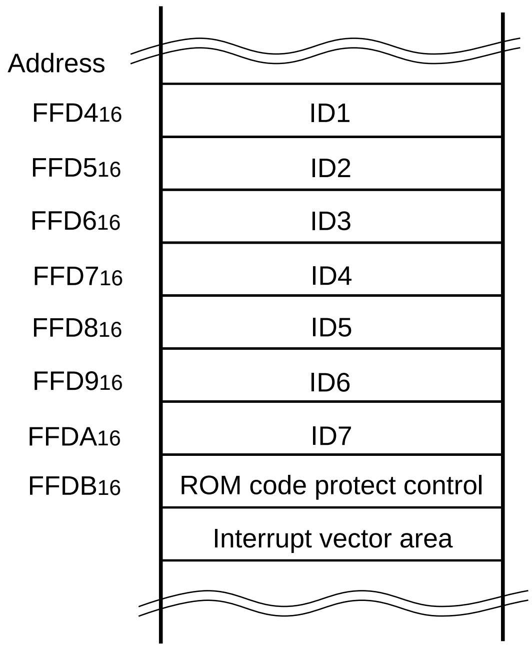


Fig. 90 ID code store addresses

● Parallel I/O Mode

The parallel I/O mode is used to input/output software commands, address and data in parallel for operation (read, program and erase) to internal flash memory.
Use the external device (writer) only for 7542 Group (flash memory version). For details, refer to the user's manual of each writer manufacturer.

• User ROM and Boot ROM Areas

In parallel I/O mode, the User ROM and Boot ROM areas shown in Figure 82 can be rewritten. Both areas of flash memory can be operated on in the same way.
The Boot ROM area is 4 Kbytes in size and located at addresses $F000_{16}$ through $FFFF_{16}$. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)
In the Boot ROM area, an erase block operation is applied to only one 4 Kbyte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. Therefore, using the MCU in standard serial I/O mode, do not rewrite to the Boot ROM area.

● Standard serial I/O Mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This mode requires a purpose-specific peripheral unit.
The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started when the microcomputer is reset and the CNVSS pin high after pulling the $P3_7$(RP) pin low, $P3_2$(CE) pin high, $P0_6$/SCLK2 pin low and $P0_5$/TxD2 pin high. (In the ordinary microcomputer mode, set CNVss pin to “L” level.)
This control program is written in the Boot ROM area when the product is shipped from Renesas. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the Boot ROM area is rewritten in parallel I/O mode. Figures 91 to 96 show the pin connections for the standard serial I/O mode.
In standard serial I/O mode, serial data I/O uses the four UART2 pins SCLK2, RxD2, TxD2 and $\overline{\text{SRDY2}}$ (BUSY). The SCLK2 pin is the transfer clock input pin through which an external transfer clock is input. The TxD2 pin is for CMOS output. The $\overline{\text{SRDY2}}$ (BUSY) pin outputs “L” level when ready for reception and “H” level when reception starts.
Serial data I/O is transferred serially in 8-bit units.
In standard serial I/O mode, only the User ROM area shown in Figure 82 can be rewritten. The Boot ROM area cannot be written.
In standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

Outline Performance (Standard Serial I/O Mode)

In standard serial I/O mode, software commands, addresses and data are input and output between the MCU and peripheral units (serial programer, etc.) using 4-wire clock-synchronized serial I/O2 (UART2).
In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the SCLK2 pin, and are then input to the MCU via the RxD2 pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxD2 pin.
The TxD2 pin is for CMOS output. Transfer is in 8-bit units with LSB first.
When busy, such as during transmission, reception, erasing or program execution, the $\overline{\text{SRDY2}}$ (BUSY) pin is “H” level. Accordingly, always start the next transfer after the $\overline{\text{SRDY2}}$ (BUSY) pin is “L” level.
Also, data and status registers in a memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register.

Table 10 Description of pin function (Flash Memory Serial I/O Mode 1)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply	I	Apply 2.7 to 5.5 V to the Vcc pin and 0 V to the Vss pin.
CNV_{SS}	CNV_{SS}	I	After input of port is set, input “H” level.
$\overline{RESET}$	Reset input	I	Reset input pin. System operates when $\overline{RESET}$ pin is set to “H” level after CNVss pin is set to “H” level.
X_{IN}	Clock input	I	Connect an oscillation circuit between the X_{IN} and X_{OUT} pins. As for the connection method, refer to the “clock generating circuit”. (When system operates only by the ring oscillator, an external circuit is not required.)
X_{OUT}	Clock output	O	
V_{REF}	Reference voltage input	I	Apply reference voltage of A-D to this pin.
$P0_0$–$P0_3$	I/O port P0	I/O	Input “L” or “H” level, or keep open.
$P0_4$	RxD input	I	Serial data input pin.
$P0_5$	TxD output	O	Serial data output pin.
$P0_6$	S_{CLK} input	I	Serial clock input pin.
$P0_7$	BUSY output	O	BUSY signal output pin.
$P1_0$–$P1_4$	I/O port P1	I/O	Input “L” or “H” level, or keep open.
$P2_0$–$P2_7$	I/O port P2	I/O	Input “L” or “H” level, or keep open.
$P3_0$, $P3_1$, $P3_3$–$P3_6$	I/O port P3	I/O	Input “L” or “H” level, or keep open.
$P3_2$	CE input	I	Input “H” level.
$P3_7$	RP input	I	Input “L” level.

Table 11 Description of pin function (Flash Memory Serial I/O Mode 2)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply	I	Apply 2.7 to 5.5 V to the Vcc pin and 0 V to the Vss pin.
CNV_{SS}	CNV_{SS}	I	After input of port is set, input “H” level.
$\overline{RESET}$	Reset input	I	Reset input pin. System operates when $\overline{RESET}$ pin is set to “H” level after CNVss pin is set to “H” level.
X_{IN}	Clock input	I	Connect an oscillation circuit between the X_{IN} and X_{OUT} pins. As for the connection method, refer to the “clock generating circuit”. (When system operates only by the ring oscillator, an external circuit is not required.)
X_{OUT}	Clock output	O	
V_{REF}	Reference voltage input	I	Apply reference voltage of A-D to this pin.
$P0_0$–$P0_3$, $P0_7$	I/O port P0	I/O	Input “L” or “H” level, or keep open.
$P0_4$	RxD input	I	Serial data input pin.
$P0_5$	TxD output	O	Serial data output pin.
$P0_6$	S_{CLK} input	I	Input “L” level.
$P1_0$–$P1_4$	I/O port P1	I/O	Input “L” or “H” level, or keep open.
$P2_0$–$P2_7$	I/O port P2	I/O	Input “L” or “H” level, or keep open.
$P3_0$, $P3_1$, $P3_3$–$P3_6$	I/O port P3	I/O	Input “L” or “H” level, or keep open.
$P3_2$	CE input	I	Input “H” level.
$P3_7$	RP input	I	Input “L” level.

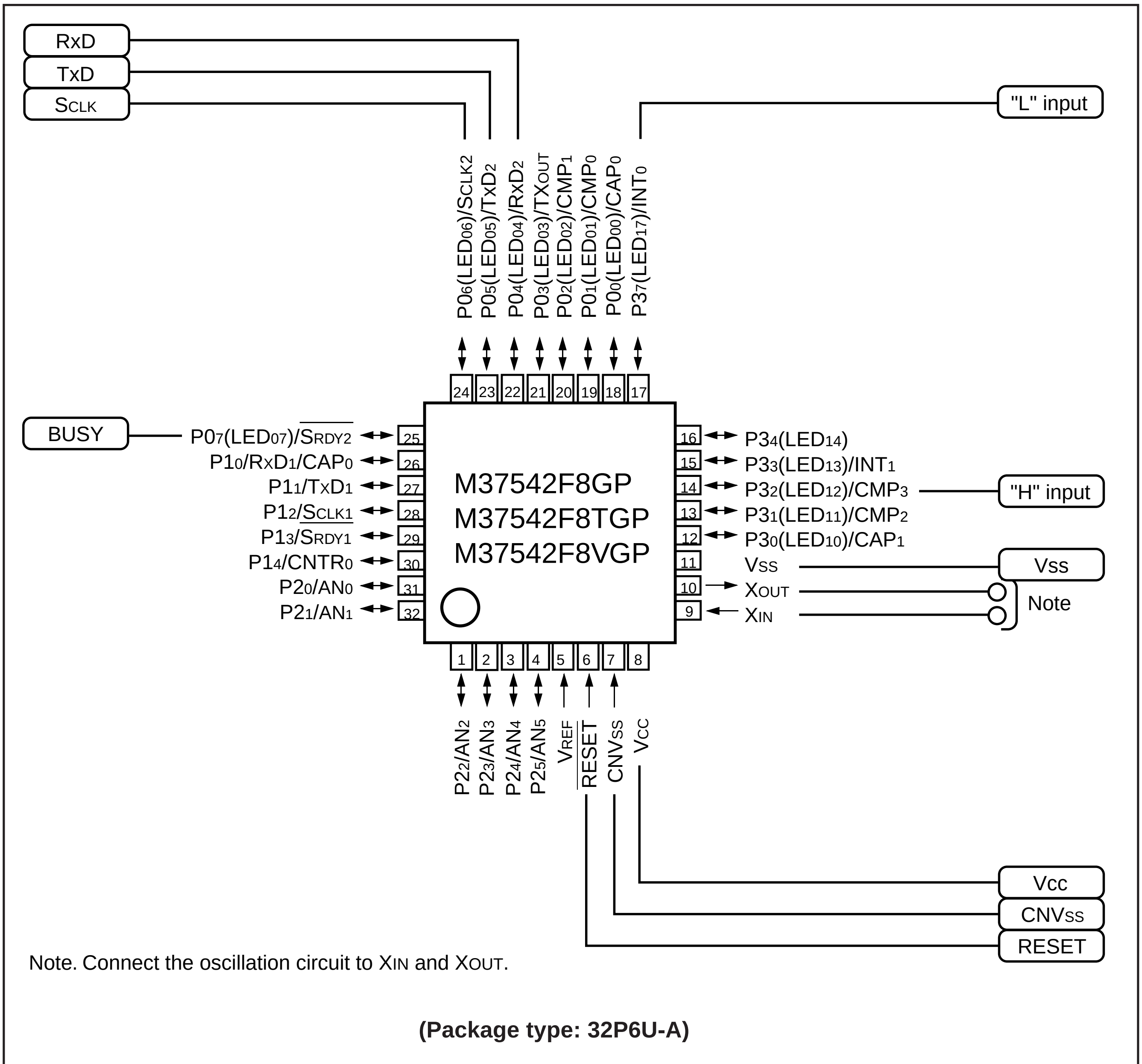
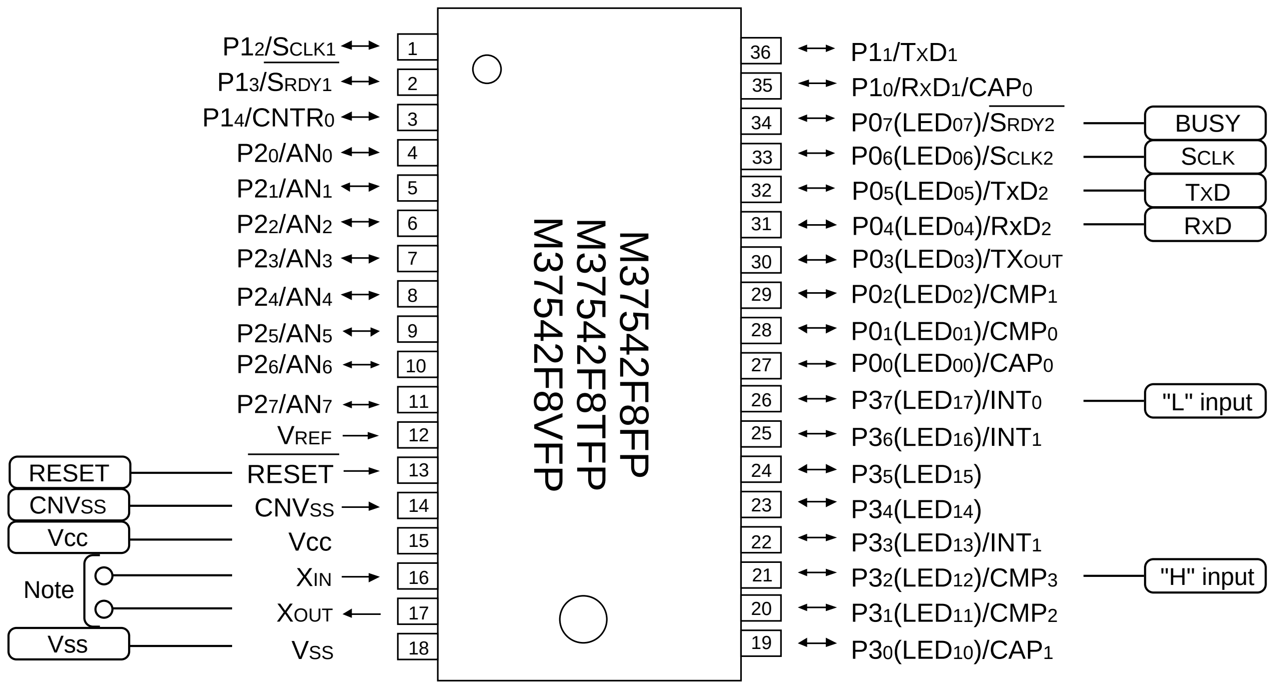


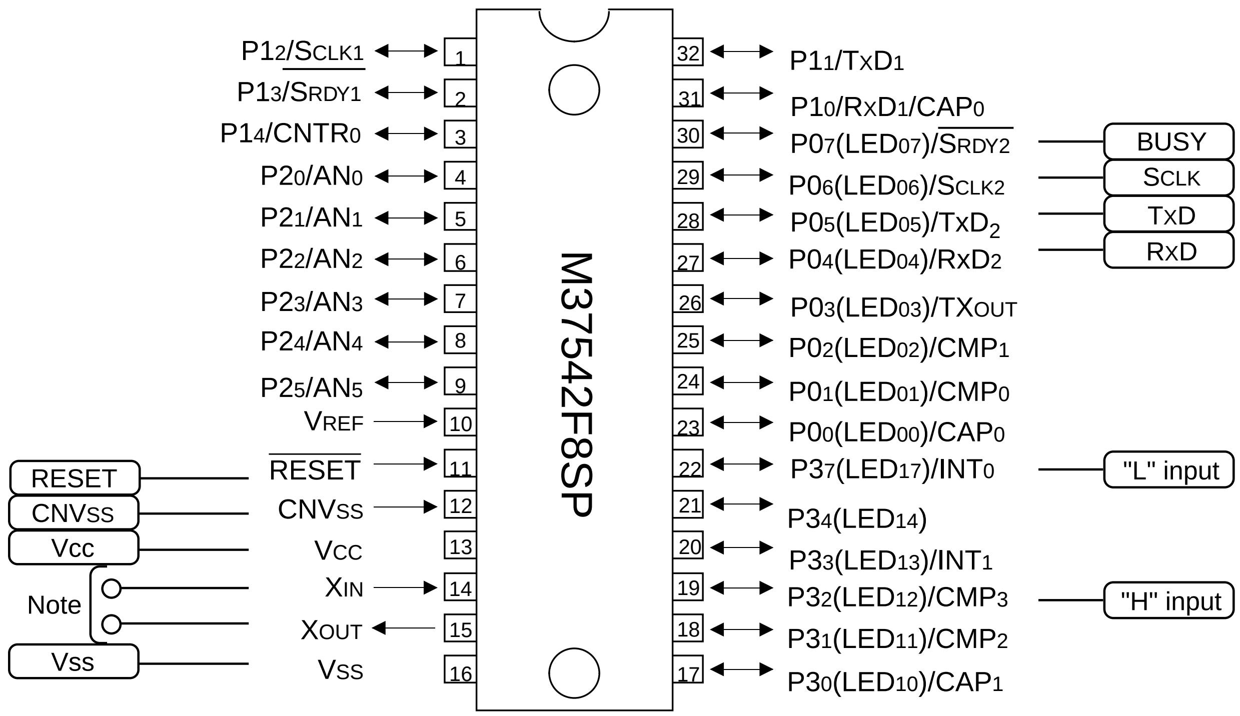
Fig. 91 Pin connection diagram in standard serial I/O mode 1 (32P6U-A package)



Note. Connect the oscillation circuit to XIN and XOUT.

(Package type: 36P2R-A)

Fig. 92 Pin connection diagram in standard serial I/O mode 1 (36P2R-A package)



Note. Connect the oscillation circuit to XIN and XOUT.

(Package type: 32P4B)

Fig. 93 Pin connection diagram in standard serial I/O mode 1 (32P4B package)

RENESAS

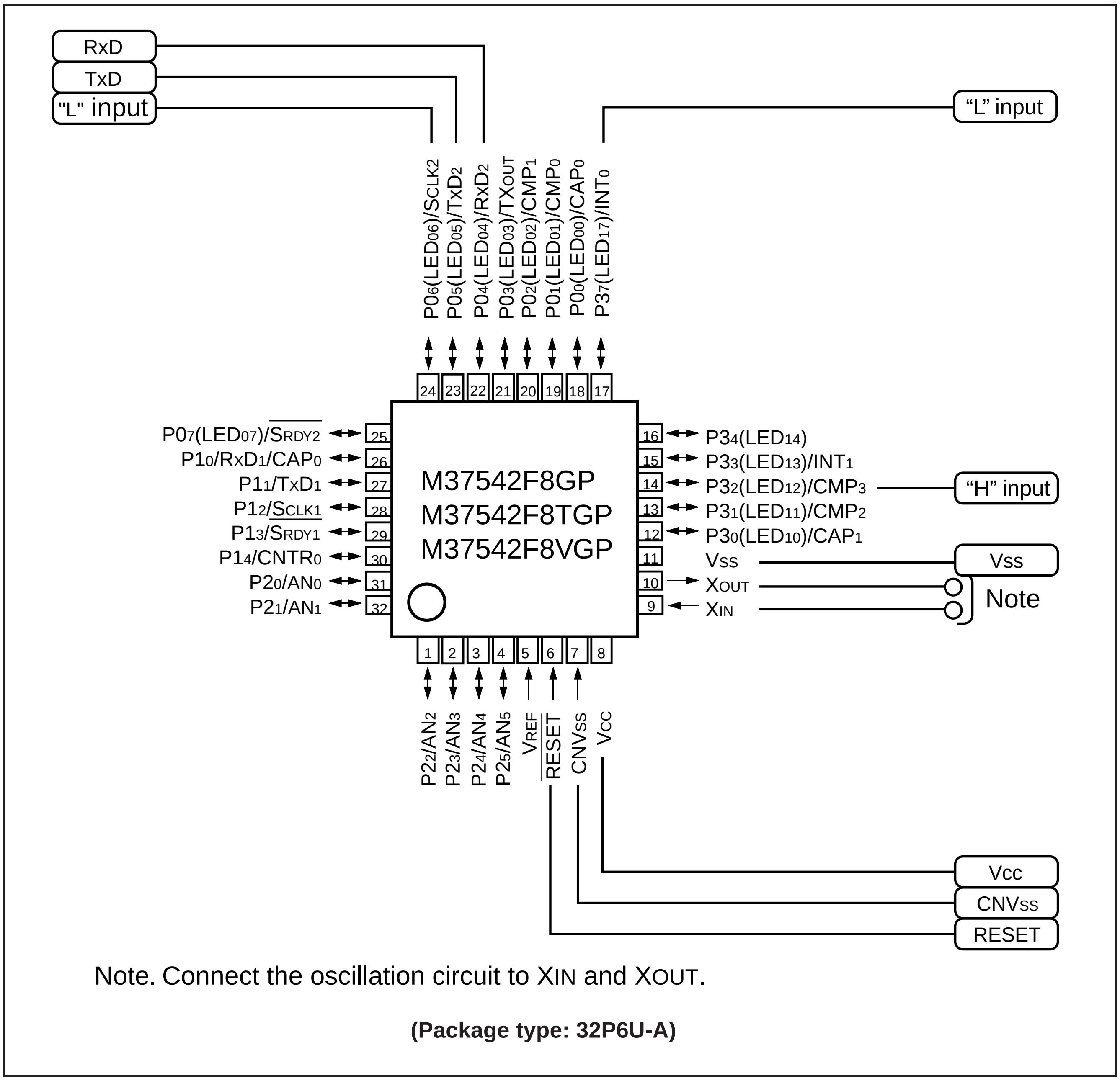
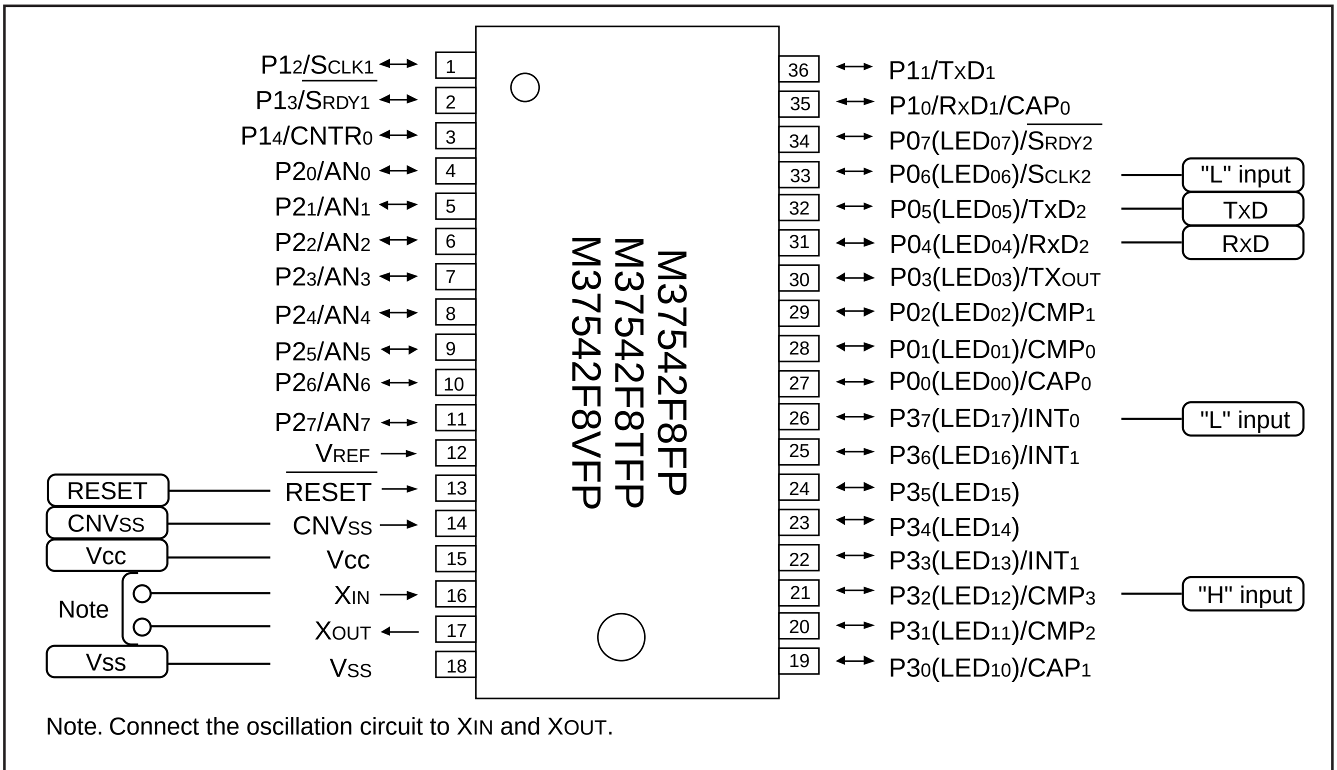
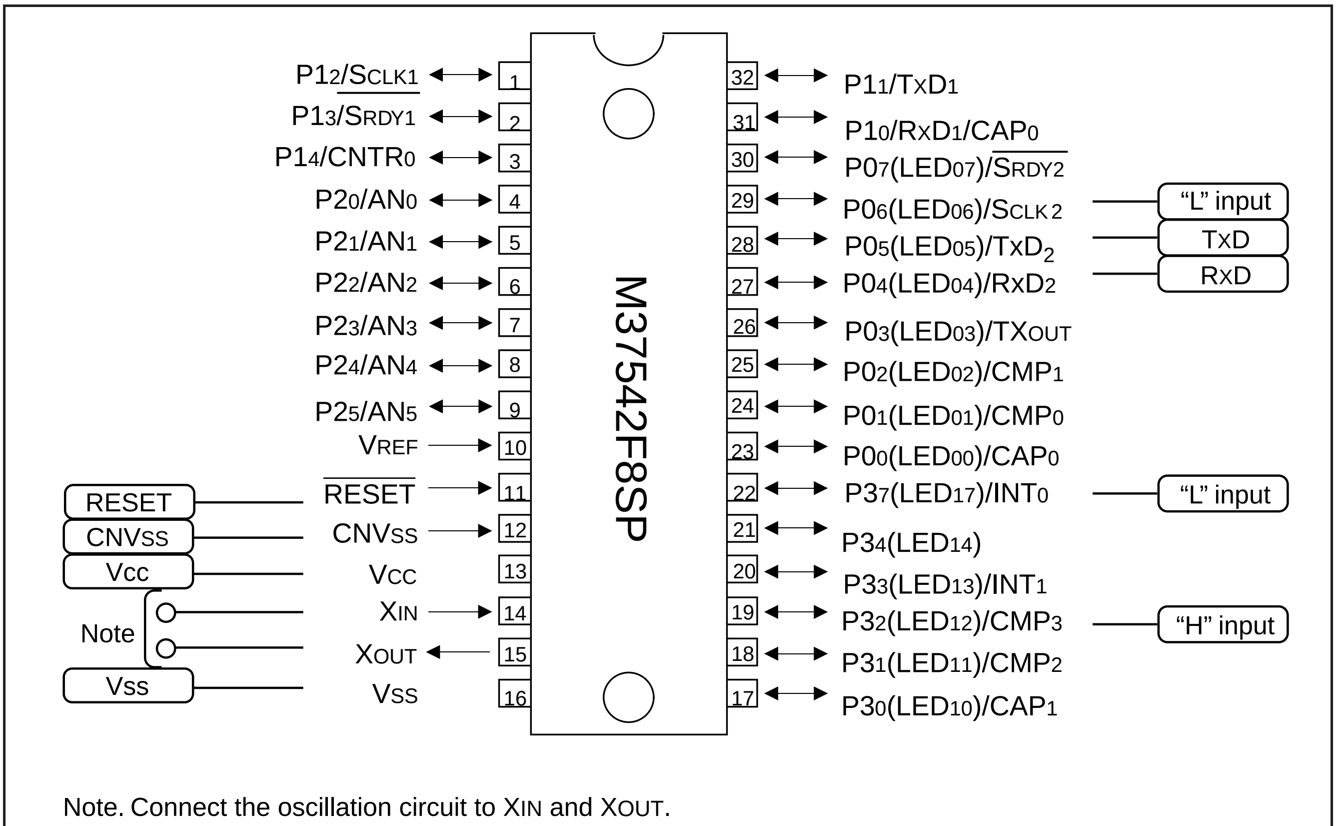


Fig. 94 Pin connection diagram in standard serial I/O mode 2 (32P6U-A package)



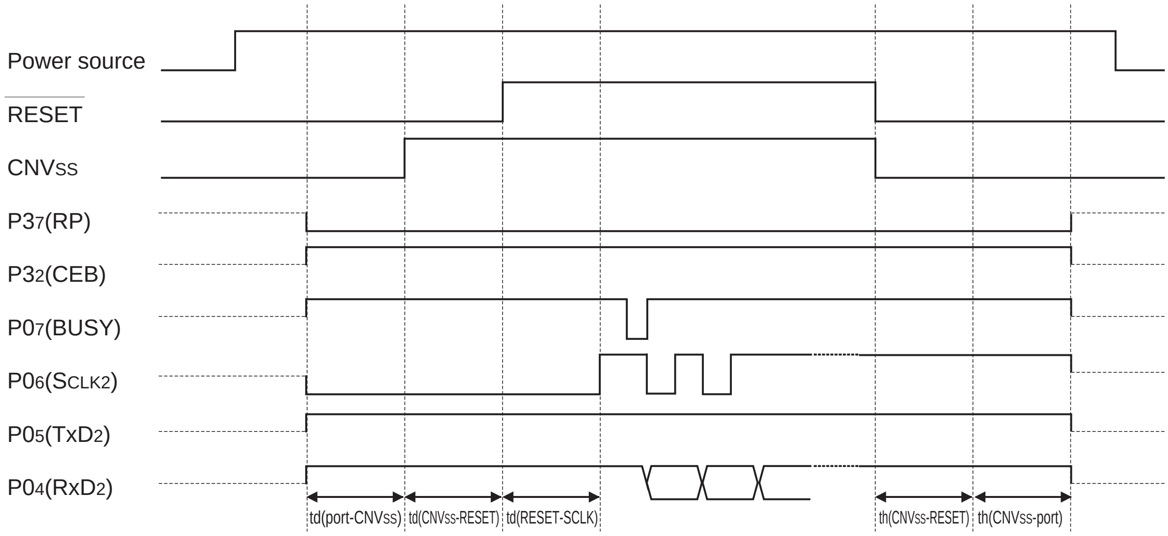
(Package type: 36P2R-A)

Fig. 95 Pin connection diagram in standard serial I/O mode 2 (36P2R-A package)



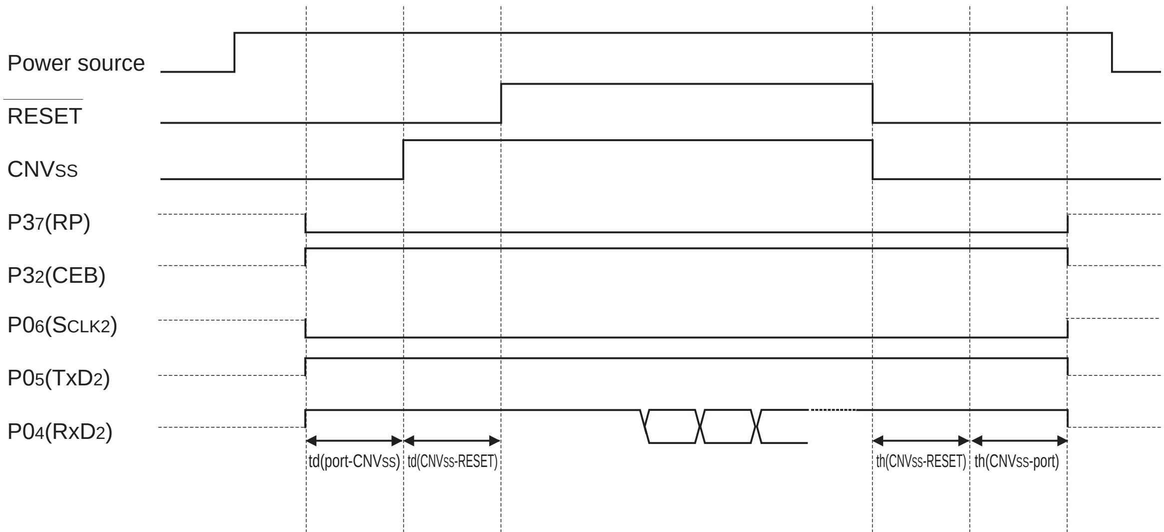
(Package type: 32P4B)

Fig. 96 Pin connection diagram in standard serial I/O mode 2 (32P4B package)



Symbol	Ratings			Unit
	Min.	Typ.	Max.	
td(port-CNVss)	1	-	-	ms
td(CNVss-RESET)	1	-	-	ms
td(RESET-SCLK)	TBD	TBD	TBD	ms
th(RESET-CNVss)	1	-	-	ms
td(CNVss-port)	1	-	-	ms

Fig. 95 Pin connection diagram in standard serial I/O mode 1



Symbol	Ratings			Unit
	Min.	Typ.	Max.	
td(port-CNVss)	1	-	-	ms
td(CNVss-RESET)	1	-	-	ms
th(RESET-CNVss)	1	-	-	ms
td(CNVss-port)	1	-	-	ms

Note: In the standard serial I/O2, set P06 and P07 as follows;
P06: input "L" level.
P07: input "L" level, "H" level or keep open.

Fig. 96 Pin connection diagram in standard serial I/O mode 2

ELECTRICAL CHARACTERISTICS

1.7542Group (General purpose)

Applied to: M37542M4/M2-XXXFP/SP/GP

Absolute Maximum Ratings (General purpose)

Table 12 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage P0₀–P0₇, P1₀–P1₄, P2₀–P2₇, P3₀–P3₇, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage P0₀–P0₇, P1₀–P1₄, P2₀–P2₇, P3₀–P3₇, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	Ta = 25°C	300 (**Note**)	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Note: 200 mW for the 32P6U-A package product.

Recommended Operating Conditions (General purpose)

Table 13 Recommended operating conditions (1) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage (ceramic)	$f(X_{IN})$ = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		$f(X_{IN})$ = 6 MHz (Double-speed mode)	4.5	5.0	5.5	V
		$f(X_{IN})$ = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
		$f(X_{IN})$ = 1 MHz (Double-speed mode)	2.2	5.0	5.5	V
	Power source voltage (RC)	$f(X_{IN})$ = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		$f(X_{IN})$ = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		$f(X_{IN})$ = 1 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage (TTL input level selected) $P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)		2.0		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}		$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$		0		$0.3V_{CC}$	V
V_{IL}	"L" input voltage (TTL input level selected) $P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)		0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$, CNV_{SS}		0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}		0		$0.16V_{CC}$	V
$\Sigma I_{OH(peak)}$	"H" total peak output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$				–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2) $P1_0$–$P1_4$, $P2_0$–$P2_7$				80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (Note 2) $P0_0$–$P0_7$, $P3_0$–$P3_7$				80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$				–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2) $P1_0$–$P1_4$, $P2_0$–$P2_7$				40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (Note 2) $P0_0$–$P0_7$, $P3_0$–$P3_7$				30	mA

Note 1: Vcc = 4.0 to 5.5V
2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended Operating Conditions (General purpose)(continued)

Table 14 Recommended operating conditions (2) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P3_0$–$P3_7$ (Drive capacity = "L") $P1_0$–$P1_4$, $P2_0$–$P2_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P3_0$–$P3_7$ (Drive capacity = "H")			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P3_0$–$P3_7$ (Drive capacity = "L") $P1_0$–$P1_4$, $P2_0$–$P2_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P3_0$–$P3_7$ (Drive capacity = "H")			15	mA
$f(X_{IN})$	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.5 to 5.5 V Double-speed mode			6	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V Double-speed mode			1	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.0 V High-, Middle-speed mode			8	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.0 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.0 V High-, Middle-speed mode			2	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.0 V High-, Middle-speed mode			2	MHz
	Oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.2 to 5.0 V High-, Middle-speed mode			1	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (General purpose)

Table 15 Electrical characteristics (1) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
		I_{OH} = –1.0 mA V_{CC} = 2.2 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P3_0$–$P3_7$ (Drive capacity = "L") $P1_0$–$P1_4$, $P2_0$–$P2_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 1.0 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P3_0$–$P3_7$ (Drive capacity = "H")	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 10 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 (Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD_1, $SCLK_1$, RxD_2, $SCLK_2$			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V
R_{OSC}	Ring oscillator oscillation frequency	V_{CC} = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
D_{OSC}	Oscillation stop detection circuit detection frequency	V_{CC} = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes 1: $P1_1$ is measured when the $P1_1$/TxD_1 P-channel output disable bit of the UART1 control register (bit 4 of address $001B_{16}$) is "0".
$P0_5$ is measured when the $P0_5$/TxD_2 P-channel output disable bit of the UART2 control register (bit 4 of address 0031_{16}) is "0".
2: RxD_1, $SCLK_1$, INT_0, and INT_1 ($P3_6$ selected) have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

Electrical Characteristics (General purpose)(continued)

Table 16 Electrical characteristics (2) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC}	Power source current	Mask ROM version	$f(X_{IN})$ = 8 MHz, Output transistors "off"	High-speed mode		TBD	TBD	mA
				Middle-speed mode		TBD	TBD	mA
			$f(X_{IN})$ = 6 MHz, Output transistors "off"	Double-speed mode		TBD	TBD	mA
			$f(X_{IN})$ = 2 MHz, V_{CC} = 2.2 V, Output transistors "off"	High-speed mode		TBD	TBD	mA
			Ring oscillator operation mode, Output transistors "off"	Frequency/1		TBD	TBD	mA
				Frequency/2		TBD	TBD	mA
				Frequency/8		TBD	TBD	mA
				Frequency/128		TBD	TBD	mA
			$f(X_{IN})$ = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors "off"			TBD	TBD	mA
			$f(X_{IN})$ = 2 MHz, V_{CC} = 2.2 V (in WIT state), functions except timer 1 disabled, Output transistors "off"			TBD	TBD	mA
			Ring oscillator operation mode, (in WIT state), functions except timer 1 disabled, Output transistors "off"			TBD	TBD	mA
			Increment when A-D conversion is executed $f(X_{IN})$ = 8 MHz, V_{CC} = 5 V			TBD	TBD	mA
			All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0	µA
				Ta = 85 °C			0.1	µA

A-D Converter Characteristics (General purpose)

Table 17 A-D Converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy	Ta = 25 °C, V_{CC} = 2.7 to 5.5 V			TBD	LSB
t_{CONV}	Conversion time				122	$t_c(X_{IN})$
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	90	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

Timing Requirements (General purpose)

Table 18 Timing requirements (1) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input "L" pulse width	2			µs
$t_C(X_{IN})$	External clock input cycle time	125			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	50			ns
$t_C(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input cycle time (Note 1)	200			ns
$t_{WH}(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input "H" pulse width (Note 1)	80			ns
$t_{WL}(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input "L" pulse width (Note 1)	80			ns
$t_C(S_{CLK1})$	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	800			ns
$t_{WH}(S_{CLK1})$	Serial I/O1, serial I/O2 clock input "H" pulse width (Note 2)	370			ns
$t_{WL}(S_{CLK1})$	Serial I/O1, serial I/O2 clock input "L" pulse width (Note 2)	370			ns
$t_{su}(RxD_1–S_{CLK1})$	Serial I/O1, serial I/O2 input set up time	220			ns
$t_h(S_{CLK1}–RxD_1)$	Serial I/O1, serial I/O2 input hold time	100			ns

Notes 1: As for CAP0, CAP1, it is the value when noise filter is not used.
2: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 0030_{16}) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Table 19 Timing requirements (2) (V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input "L" pulse width	2			µs
$t_C(X_{IN})$	External clock input cycle time	250			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	100			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	100			ns
$t_C(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input cycle time (Note 1)	500			ns
$t_{WH}(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input "H" pulse width (Note 1)	230			ns
$t_{WL}(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input "L" pulse width (Note 1)	230			ns
$t_C(S_{CLK1})$	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	2000			ns
$t_{WH}(S_{CLK1})$	Serial I/O1, serial I/O2 clock input "H" pulse width (Note 2)	950			ns
$t_{WL}(S_{CLK1})$	Serial I/O1, serial I/O2 clock input "L" pulse width (Note 2)	950			ns
$t_{su}(RxD_1–S_{CLK1})$	Serial I/O1, serial I/O2 input set up time	400			ns
$t_h(S_{CLK1}–RxD_1)$	Serial I/O1, serial I/O2 input hold time	200			ns

Notes 1: As for CAP0, CAP1, it is the value when noise filter is not used.
2: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is "0" (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 0030_{16}) is set to "1" (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is "0" (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Table 20 Timing requirements (3) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	2			µs
$t_C(X_{IN})$	External clock input cycle time	500			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	200			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	200			ns
$t_C(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input cycle time (Note 1)	1000			ns
$t_{WH}(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input “H” pulse width (Note 1)	460			ns
$t_{WL}(CNTR_0)$	$CNTR_0$, INT_0, INT_1, CAP_0, CAP_1 input “L” pulse width (Note 1)	460			ns
$t_C(S_{CLK1})$	Serial I/O1, serial I/O2 clock input cycle time (Note 2)	4000			ns
$t_{WH}(S_{CLK1})$	Serial I/O1, serial I/O2 clock input “H” pulse width (Note 2)	1900			ns
$t_{WL}(S_{CLK1})$	Serial I/O1, serial I/O2 clock input “L” pulse width (Note 2)	1900			ns
$t_{su}(RxD_1–S_{CLK1})$	Serial I/O1, serial I/O2 input set up time	800			ns
$t_h(S_{CLK1}–RxD_1)$	Serial I/O1, serial I/O2 input hold time	400			ns

Notes 1: As for CAP0, CAP1, it is the value when noise filter is not used.
2: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.
In this time, bit 6 of the serial I/O2 control register (address 0030_{16}) is set to “1” (clock synchronous serial I/O is selected).
When bit 6 of the serial I/O2 control register is “0” (clock asynchronous serial I/O is selected), the rating values are divided by 4.

Switching Characteristics (General purpose)

Table 21 Switching characteristics (1) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1, serial I/O2 clock output “H” pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1, serial I/O2 clock output “L” pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_d(S_{CLK1}–T_XD_1)$	Serial I/O1, serial I/O2 output delay time			140	ns
$t_v(S_{CLK1}–T_XD_1)$	Serial I/O1, serial I/O2 output valid time	–30			ns
$t_r(S_{CLK1})$	Serial I/O1, serial I/O2 clock output rising time			30	ns
$t_f(S_{CLK1})$	Serial I/O1, serial I/O2 clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time (Note 1)		10	30	ns
t_f(CMOS)	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin X_{OUT} is excluded.

Table 22 Switching characteristics (2) (V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

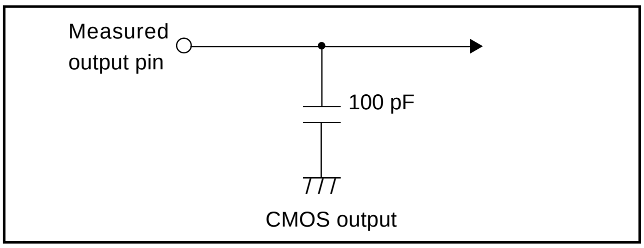
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1, serial I/O2 clock output “H” pulse width	$t_C(S_{CLK1})/2–50$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1, serial I/O2 clock output “L” pulse width	$t_C(S_{CLK1})/2–50$			ns
$t_d(S_{CLK1}–T_XD_1)$	Serial I/O1, serial I/O2 output delay time			350	ns
$t_v(S_{CLK1}–T_XD_1)$	Serial I/O1, serial I/O2 output valid time	–30			ns
$t_r(S_{CLK1})$	Serial I/O1, serial I/O2 clock output rising time			50	ns
$t_f(S_{CLK1})$	Serial I/O1, serial I/O2 clock output falling time			50	ns
t_r(CMOS)	CMOS output rising time (Note 1)		20	50	ns
t_f(CMOS)	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin X_{OUT} is excluded.

Table 23 Switching characteristics (3) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1, serial I/O2 clock output “H” pulse width	$t_C(S_{CLK1})/2–70$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1, serial I/O2 clock output “L” pulse width	$t_C(S_{CLK1})/2–70$			ns
$t_d(S_{CLK1}–T_XD_1)$	Serial I/O1, serial I/O2 output delay time			450	ns
$t_v(S_{CLK1}–T_XD_1)$	Serial I/O1, serial I/O2 output valid time	–30			ns
$t_r(S_{CLK1})$	Serial I/O1, serial I/O2 clock output rising time			70	ns
$t_f(S_{CLK1})$	Serial I/O1, serial I/O2 clock output falling time			70	ns
t_r(CMOS)	CMOS output rising time (Note 1)		25	70	ns
t_f(CMOS)	CMOS output falling time (Note 1)		25	70	ns

Note 1: Pin X_{OUT} is excluded.



Switching characteristics measurement circuit diagram (General purpose)

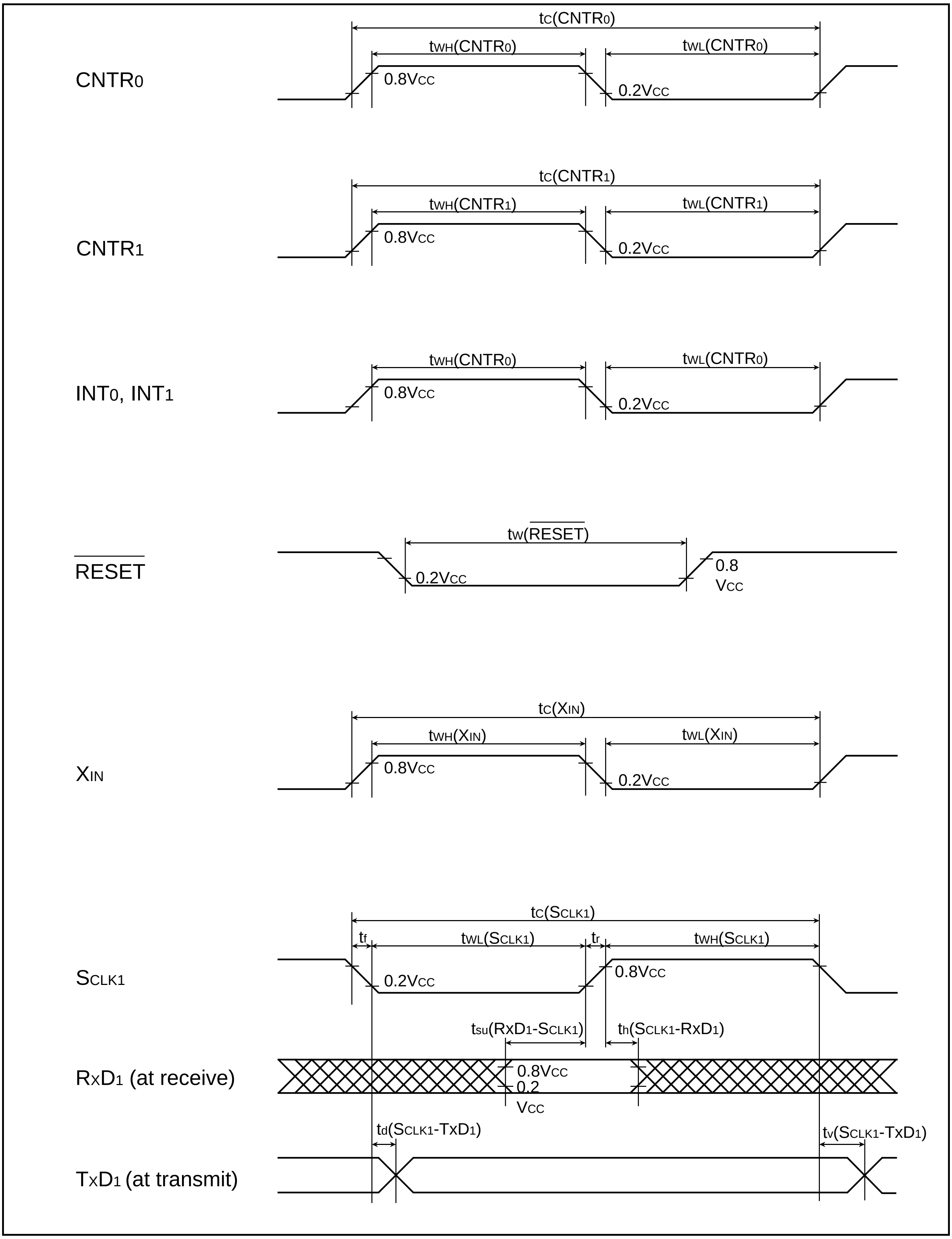


Fig. 99 Timing chart (General purpose)

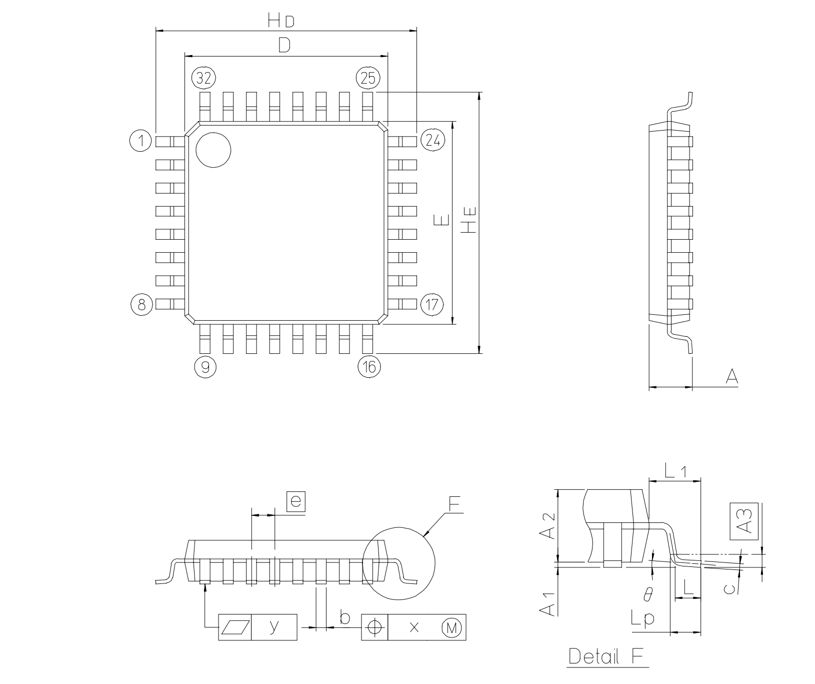
PACKAGE OUTLINE

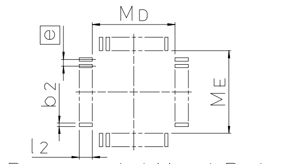
32P6U-A (MMP)

Plastic 32pin 7×7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	——		Cu Alloy

Scale: 4/1





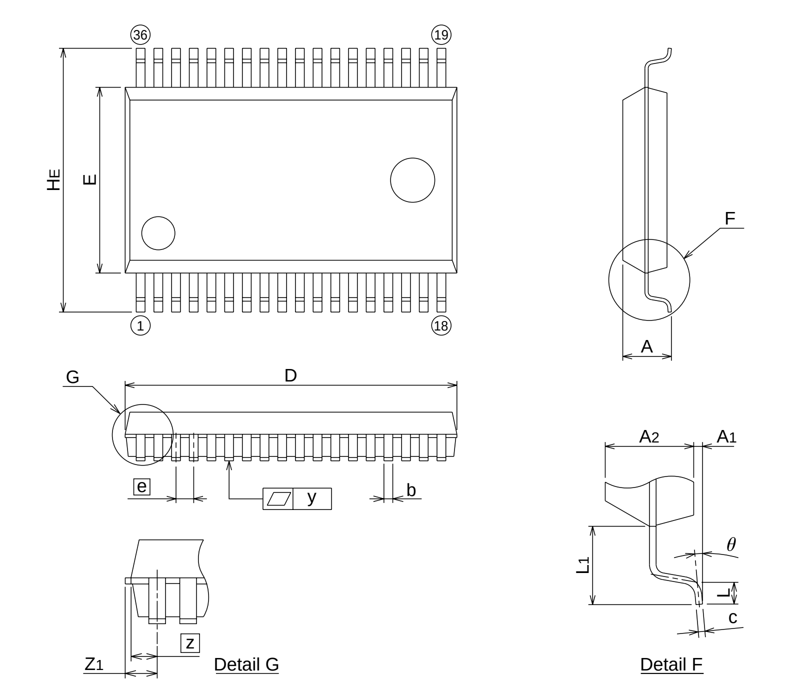
Recommended Mount Pad

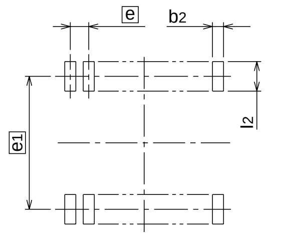
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	—	0.8	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
L	0.3	0.5	0.7
L_1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	8°
b_2	—	0.5	—
I_2	1.0	—	—
M_D	—	7.4	—
M_E	—	7.4	—

36P2R-A (MMP)

Plastic 36pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	–	0.53	Alloy 42





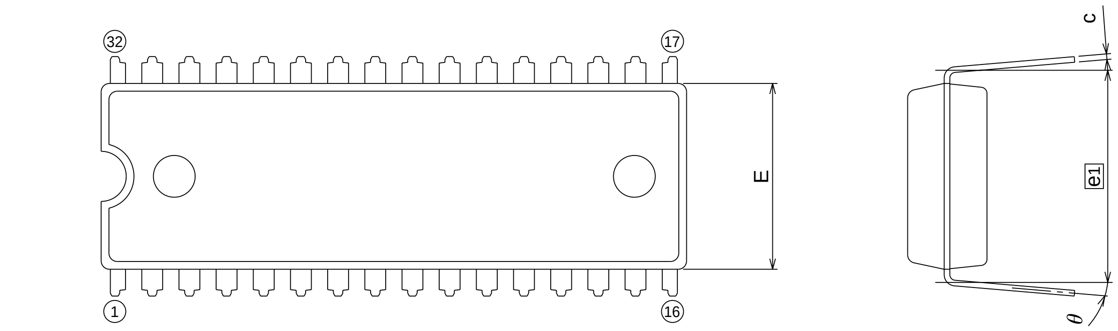
Recommended Mount Pad

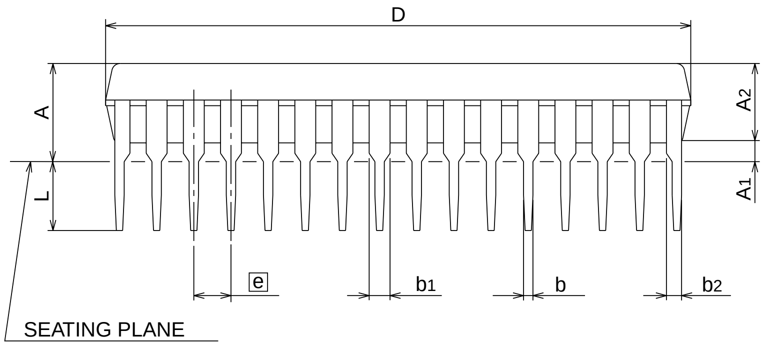
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	–	0.8	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
z	–	0.7	–
Z_1	–	–	0.85
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.5	–
e_1	–	11.43	–
I_2	1.27	–	–

32P4B (MMP)

Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	–	2.2	Alloy 42/Cu Alloy





Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	–	1.778	–
e_1	–	10.16	–
L	3.0	–	–
θ	0°	–	15°

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REVISION HISTORY	7542 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 27, 2002	–	First edition issued
2.00	Apr. 21, 2003	1	FEATURES; Memory size revised.
		8	Memory size; Flash memory size revised. Fig.8; ROM size revised.
		9	Table 2; ROM size revised.
		10	Central Processing Unit (CPU); Description revised.
		28	Fig.26; Port $P0_3$ direction register revised.
		36	Fig.42; Modulation output revised.
		37	Fig.43; Modulation output revised.
		53	Reset Circuit; Description revised.
		55	(3) RC oscillation; Description revised.
		56	(1) Oscillation control • Stop mode Description about FLASH added.
		57	Fig.77; revised.
		65 to 72	FLASH MEMORY MODE added.
		73 to 82	ELECTRICAL CHARACTERISTICS added.