DATA SHEET

74LVC543A
Octal D-type registered transceiver; 3-state

Product specification
Supersedes data of 2000 Jun 21

2003 May 16

Philips Semiconductors

PHILIPS

Octal D-type registered transceiver; 3-state 74LVC543A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low-power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-state non-inverting outputs for bus oriented applications
- High-impedance when V_{CC} = 0 V.

DESCRIPTION

The 74LVC543A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC543A is an octal registered transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable inputs ($\overline{LE}_{AB}$ and $\overline{LE}_{BA}$) and output enable inputs ($\overline{OE}_{AB}$ and $\overline{OE}_{BA}$) are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The 74LVC543A contains eight D-type latches, with separate inputs and controls for each set. For data flow from A to B, for example, the A to B enable input ($\overline{E}_{AB}$) must be LOW in order to enter data from A0 to A7 or take data from B0 to B7, as indicated in the “Function table”. With pin $\overline{E}_{AB}$ LOW, a LOW signal on the A to B latch enable input ($\overline{LE}_{AB}$) makes the A to B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LE}_{AB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With pins $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay An to Bn	C_L = 50 pF; V_{CC} = 3.3 V	3.3	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10.0	pF
C_{PD}	power dissipation capacitance per latch	V_{CC} = 3.3 V; note 1	27	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts;

   N = total load switching outputs;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUT				OUTPUT
	$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	DATA	
Disabled	H	X	X	X	Z
	X	H	X	X	Z
Disabled plus latch	L	↑	L	h	Z
	L	↑	L	l	Z
Latch plus display	L	L	↑	h	H
	L	L	↑	l	L
Transparent	L	L	L	H	H
	L	L	L	L	L
Hold (do nothing)	L	L	H	X	NC

Note

1. XX = AB for A to B direction; BA for B to A direction;
   H = HIGH voltage level;
   L = LOW voltage level;
   h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ and $\overline{E}_{BA}$;
   l = LOW state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ and $\overline{E}_{BA}$;
   X = don't care;
   ↑ = LOW-to-HIGH level transition;
   NC = no change;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC543AD	–40 to +85 °C	24	Small Outline (SO)	plastic	SOT137-1
74LVC543ADB	–40 to +85 °C	24	Shrink Small Outline (SSOP) Type II	plastic	SOT340-1
74LVC543APW	–40 to +85 °C	24	Thin Shrink Small Outline (TSSOP) Type I	plastic	SOT355-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{LE}_{BA}$	B to A latch enable input (active LOW)
2	$\overline{OE}_{BA}$	B to A output enable input (active LOW)
3, 4, 5, 6, 7, 8, 9 10	A0 to A7	A data inputs/outputs
11	$\overline{E}_{AB}$	A to B enable input (active LOW)
12	GND	ground (0 V)
22, 21, 20, 19, 18, 17, 16, 15	B0 to B7	B data inputs/outputs
13	$\overline{OE}_{AB}$	A to B output enable input (active LOW)
14	$\overline{LE}_{AB}$	A to B latch enable input (active LOW)
23	$\overline{E}_{BA}$	B to A enable input (active LOW)
24	V_{CC}	positive supply voltage

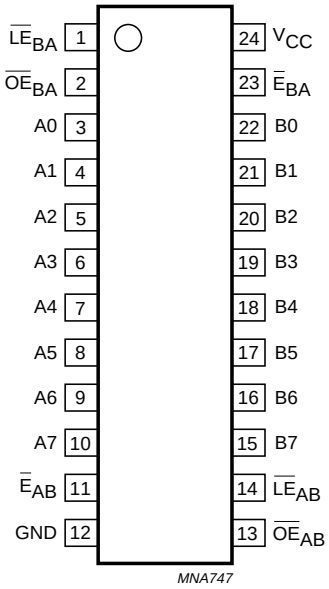


Fig.1 Pin configuration.

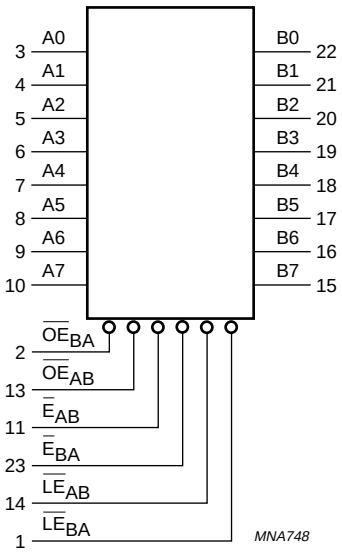


Fig.2 Logic symbol.

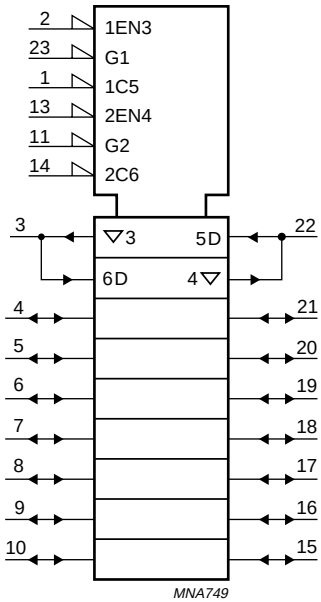


Fig.3 Logic symbol (IEEE/IEC).

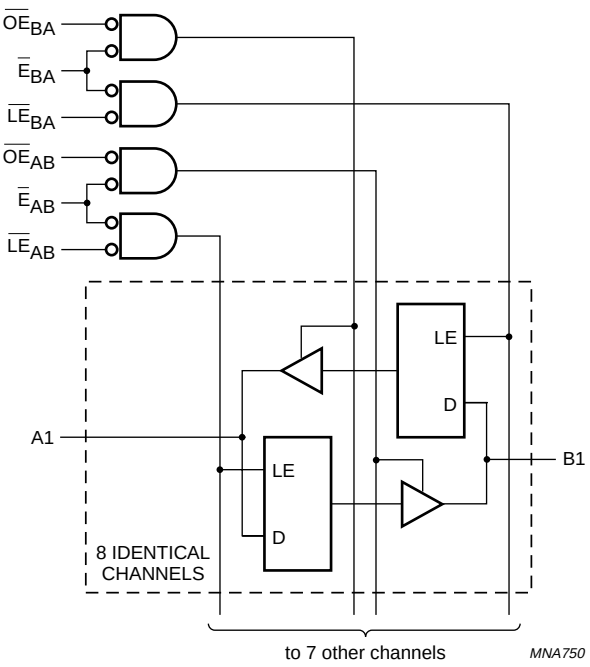


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
$V_{I/O}$	output voltage	output HIGH or LOW state	0	V_{CC}	V
$V_{I/O}$	input voltage	output 3-state	0	5.5	V
T_{amb}	operating ambient temperature	in free air	–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 2	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
$V_{I/O}$	output voltage	output HIGH or LOW state; note 2	–0.5	V_{CC} +0.5	V
$V_{I/O}$	input voltage	output 3-state; note 2	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation				
	SO package	above 70 °C derate linearly with 8 mW/K	–	500	mW
	SSOP and TSSOP packages	above 60 °C derate linearly with 5.5 mW/K	–	500	mW

Notes

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −12 mA	2.7	V_{CC} − 0.5	–	–	V
		I_O = −100 μA	3.0	V_{CC} − 0.2	V_{CC}	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.6	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 12 mA	2.7	–	–	0.40	V
		I_O = 100 μA	3.0	–	GND	0.20	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; not for I/O pins	3.6	–	±0.1	±5	μA
I_{IHZ}, I_{ILZ}	input current for common I/O pins	V_I = 5.5 V or GND	3.6	–	±0.1	±15	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	3.6	–	0.1	±10	μA
I_{off}	power off leakage supply current	V_I or V_O = 5.5 V	0.0	–	0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	3.6	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0	2.7 to 3.6	–	5	500	μA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC CHARACTERISTICS

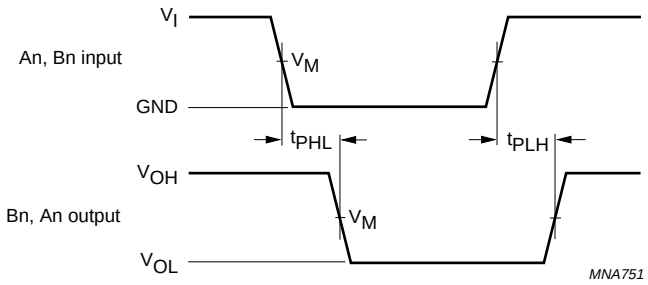
GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF.

SYMBOL	PARAMETER	WAVEFORMS	MIN.	TYP.	MAX.	UNIT
V_{CC} = 3.0 to 3.6 V; note 1						
t_{PHL}/t_{PLH}	propagation delay An to Bn; Bn to An	see Figs 5 and 9	1.5	3.3	7	ns
	propagation delay $\overline{LE}_{BA}$ to An; $\overline{LE}_{AB}$ to Bn	see Figs 6 and 9	1.5	4.1	8.5	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 7 and 9	1.5	4.2	7.7	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 7 and 9	1.5	3.4	7.0	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 7 and 9	1.5	4.4	8.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 7 and 9	1.5	3.6	7.0	ns
t_W	$\overline{LE}_{XX}$ pulse with LOW	see Fig.6	3.0	0.9	–	ns
t_{su}	set-up time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.8	+1.5	–0.5	–	ns
t_h	hold time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.8	1.5	0.6	–	ns
V_{CC} = 2.7 V						
t_{PHL}/t_{PLH}	propagation delay An to Bn; Bn to An	see Figs 5 and 9	1.5	–	8	ns
	propagation delay $\overline{LE}_{BA}$ to An; $\overline{LE}_{AB}$ to Bn	see Figs 6 and 9	1.5	–	9.5	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 7 and 9	1.5	–	9.2	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 7 and 9	1.5	–	7.5	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 7 and 9	1.5	–	9.3	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 7 and 9	1.5	–	7.5	ns
t_W	$\overline{LE}_{XX}$ pulse with LOW	see Fig.6	3.0	–	–	ns
t_{su}	set-up time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.8	1.5	–	–	ns
t_h	hold time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.8	1.5	–	–	ns
V_{CC} = 1.2 V						
t_{PHL}/t_{PLH}	propagation delay An to Bn; Bn to An	see Figs 5 and 9	–	13.0	–	ns
	propagation delay $\overline{LE}_{BA}$ to An; $\overline{LE}_{AB}$ to Bn	see Figs 6 and 9	–	16.0	–	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 7 and 9	–	15.0	–	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 7 and 9	–	8.0	–	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 7 and 9	–	15.0	–	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 7 and 9	–	8.0	–	ns
t_W	$\overline{LE}_{XX}$ pulse with LOW	see Fig.6	–	4.0	–	ns
t_{su}	set-up time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.8	–	–1.5	–	ns
t_h	hold time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.8	–	2.0	–	ns

Note

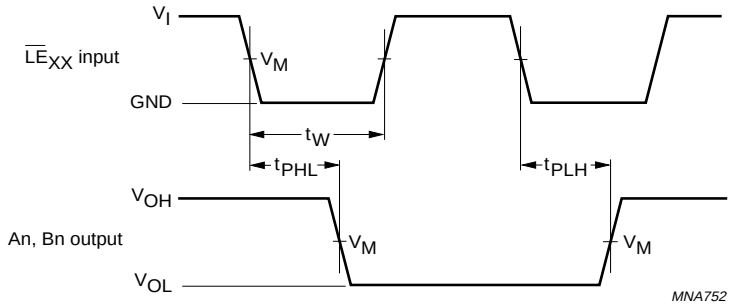
1. Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC WAVEFORMS



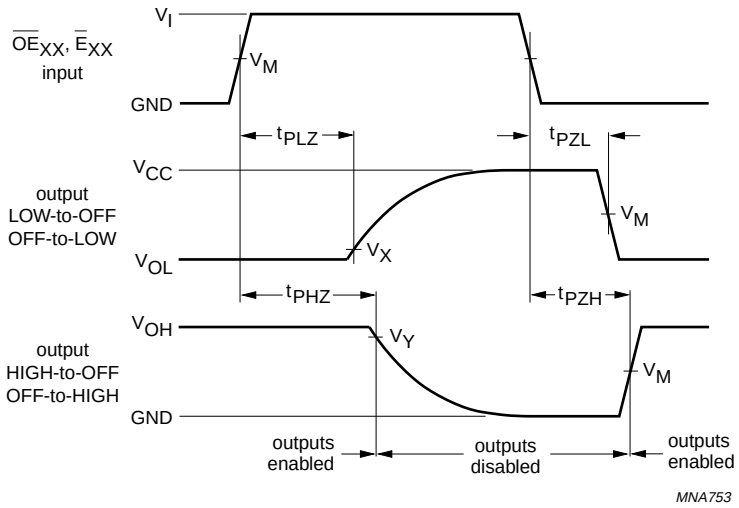
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 Input (An and Bn) to output (Bn and An) propagation delays.



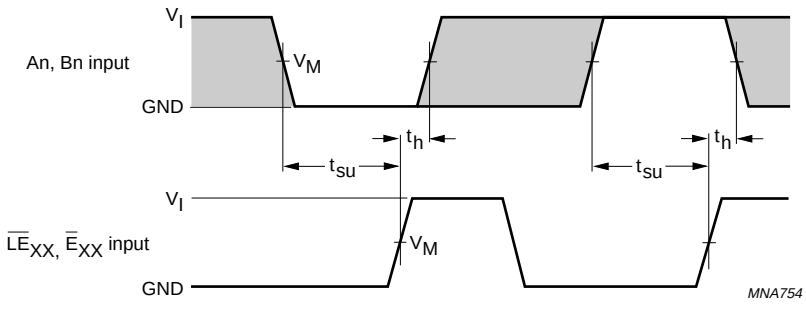
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 Latch enable input ($\overline{LE}_{XX}$) pulse width and latch enable input to output An and Bn propagation delays.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq$ 2.7 V; $V_X = V_{OL} + 0.1V_{CC}$ at V_{CC} < 2.7 V.
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq$ 2.7 V; $V_Y = V_{OH} - 0.1V_{CC}$ at V_{CC} < 2.7 V.

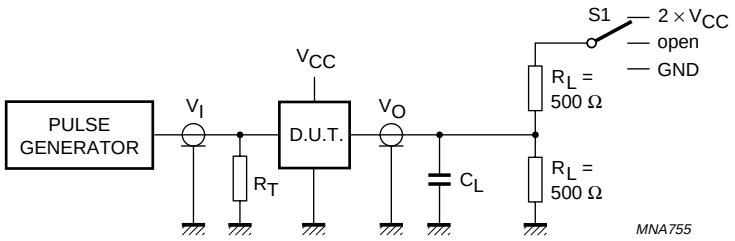
Fig.7 3-state enable and disable times.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.8 Data set-up and hold times for the inputs An and Bn to $\overline{LE}_{XX}$ and $\overline{E}_{XX}$ inputs.



SWITCH POSITION	
TEST	**SWITCH**
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
<2.7 V	V_{CC}
2.7 to 3.6 V	2.7 V

Definitions for test circuit:

R_L = Load resistor.

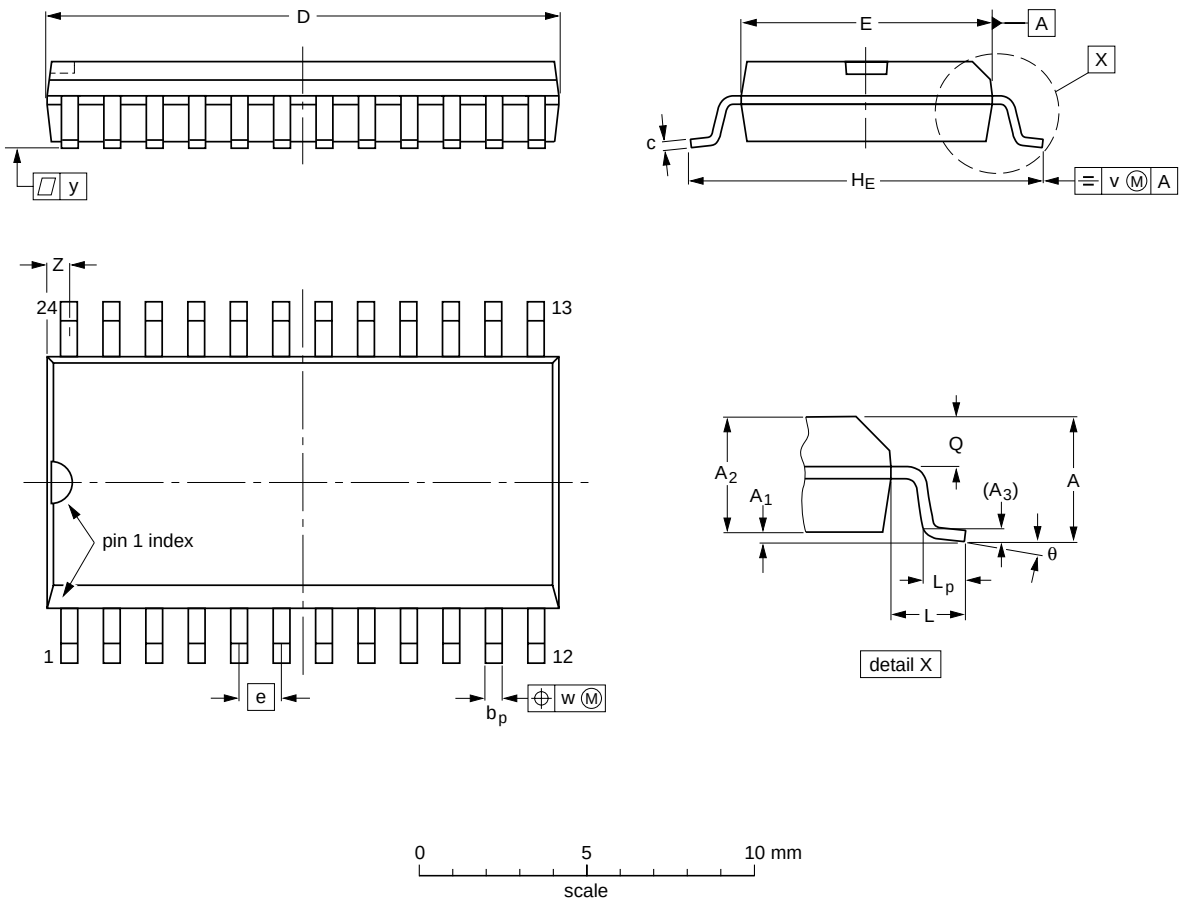
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuitry for switching times.

PACKAGE OUTLINES

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

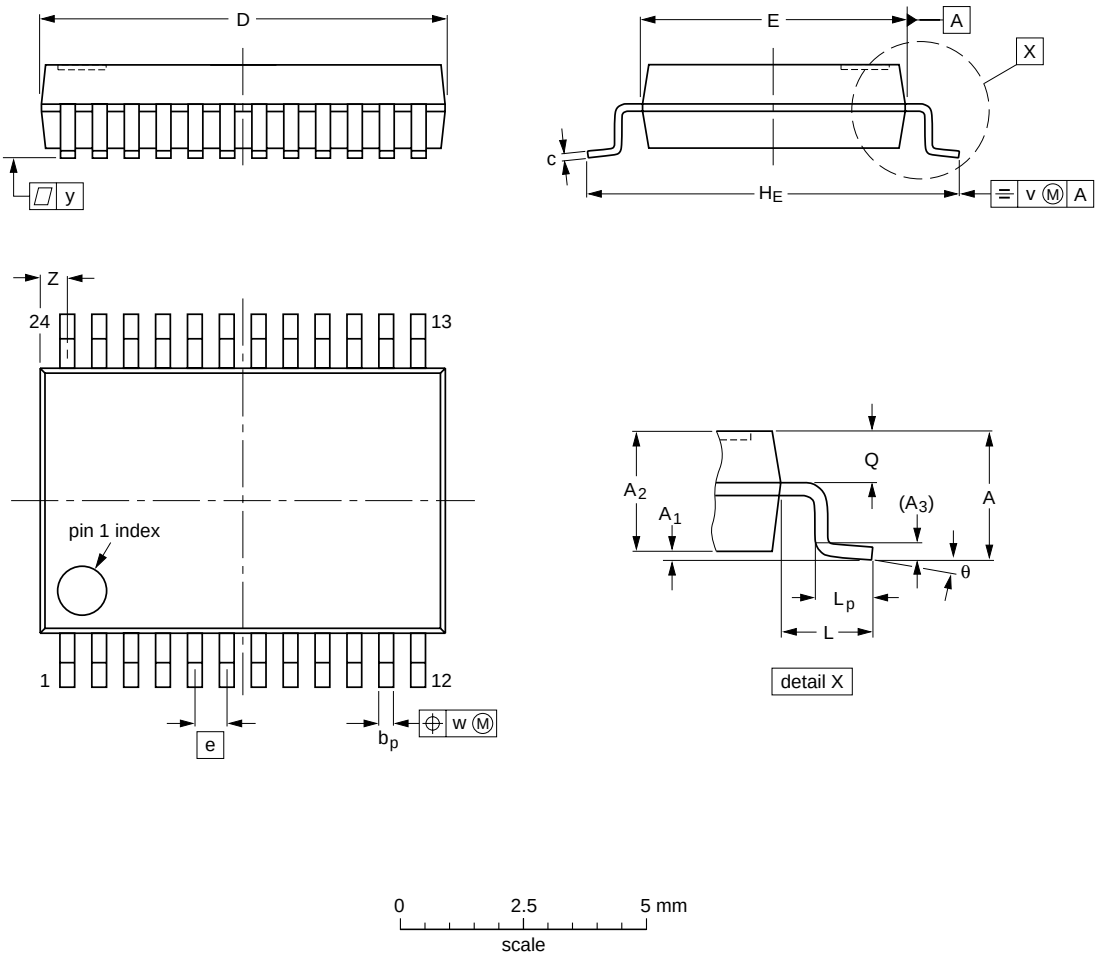
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

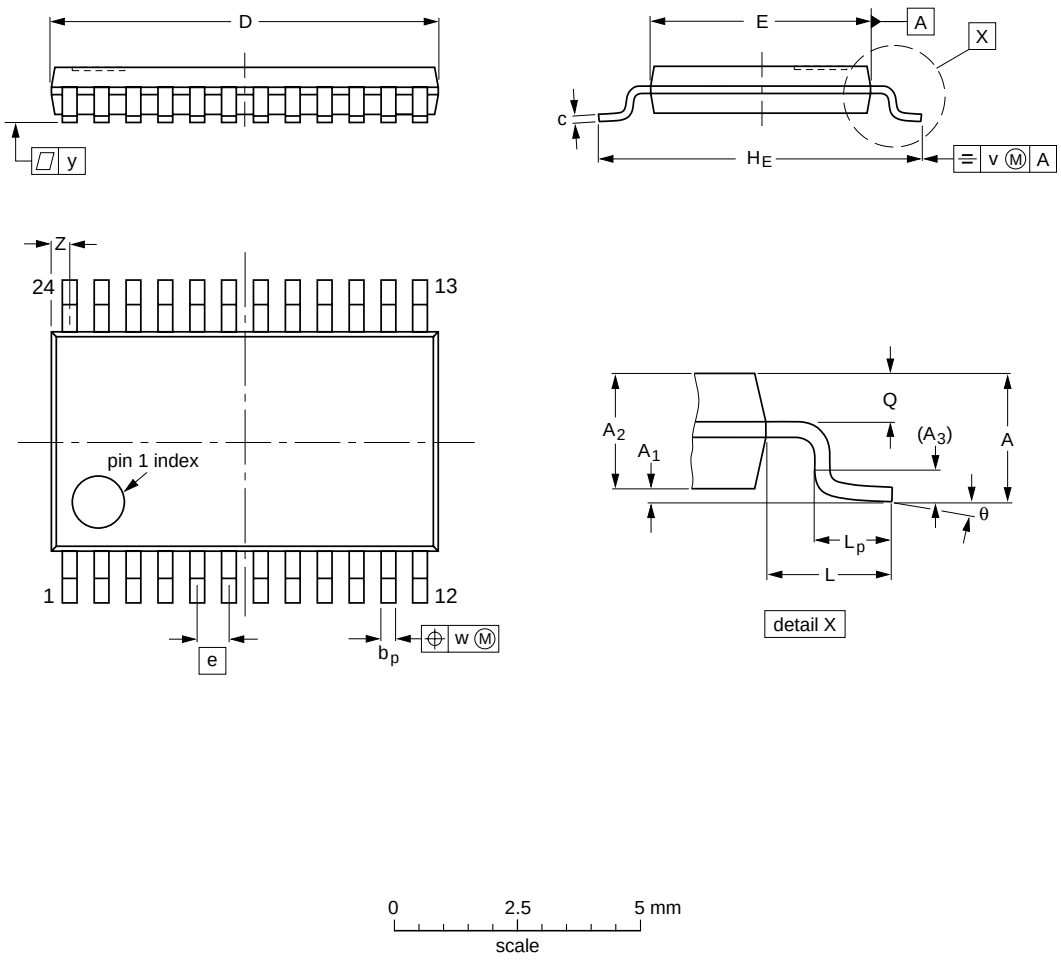
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Printed in The Netherlands 613508/04/pp20 Date of release: 2003 May 16 Document order number: 9397 750 10034

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