

- **Members of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **Parity Error Flag With Parity Generator/Checker**
- **Register for Storage of the Parity Error Flag**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

#### description

The 'ACT16833 consist of two noninverting 8-bit to 9-bit parity bus transceivers and are designed for communication between data buses. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY or 2PARITY is configured as an input and combined with the B-input data to generate an active-low error flag if odd parity is not detected.

The error ( $1\overline{ERR}$  or  $2\overline{ERR}$ ) output is configured as an open-collector output. The B-to-A parity error flag is clocked into  $1\overline{ERR}$  or  $2\overline{ERR}$  on the low-to-high transition of the clock (1CLK or 2CLK) input.  $1\overline{ERR}$  or  $2\overline{ERR}$  is cleared (set high) by taking the clear ( $1\overline{CLR}$  or  $2\overline{CLR}$ ) input low.

The output-enable ( $\overline{OEA}$  and  $\overline{OEB}$ ) inputs can be used to disable the device so that the buses are effectively isolated. When both  $\overline{OEA}$  and  $\overline{OEB}$  are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 74ACT16833 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16833 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74ACT16833 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

54ACT16833 . . . WD PACKAGE  
74ACT16833 . . . DL PACKAGE  
(TOP VIEW)

1OEB	1	56	1OEA
1CLK	2	55	1CLR
1ERR	3	54	1PARITY
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V <sub>CC</sub>	7	50	V <sub>CC</sub>
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2ERR	26	31	2PARITY
2CLK	27	30	2CLR
2OEB	28	29	2OEA



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# 54ACT16833, 74ACT16833 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
<u>OEB</u>	<u>OEA</u>	<u>CLR</u>	CLK	$\Sigma$ OF H	$\Sigma$ OF H	A	B	PARITY	<u>ERR</u> ‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error-flag register
H	H	H	No↑	X				NC		Isolation§
		L	No↑	X					H	
		H	↑	Odd	X	Z	Z	Z	H	
		H	↑	Even					L	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

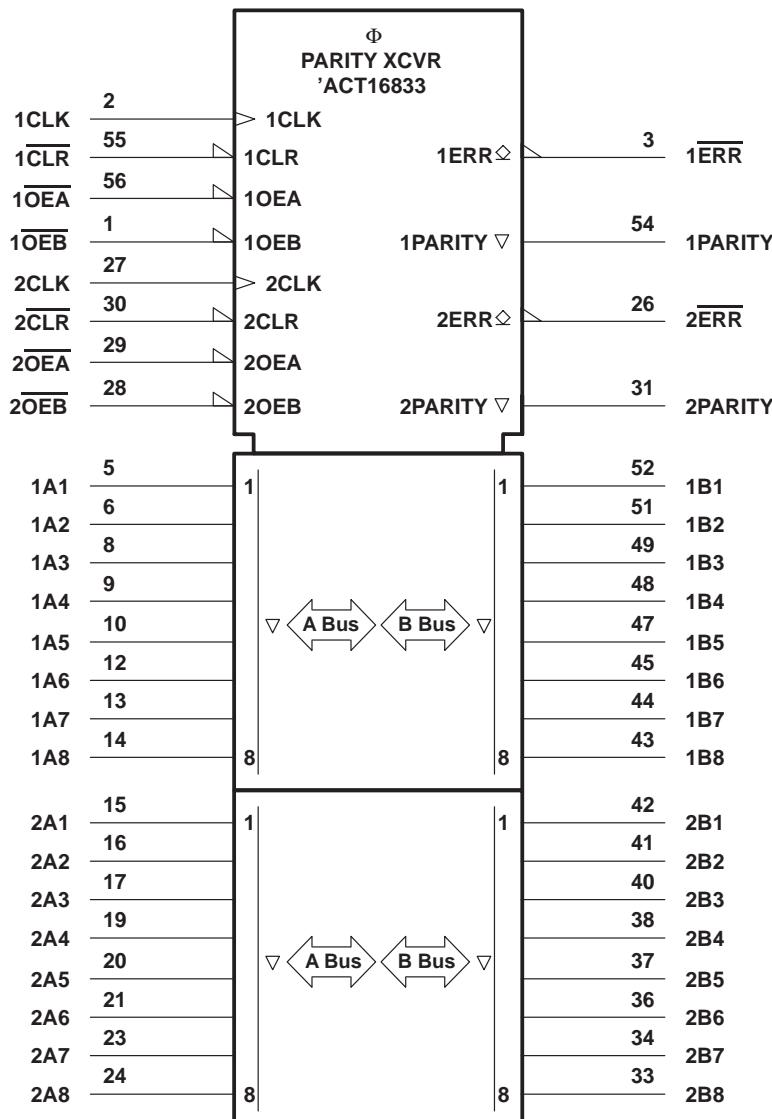
‡ Output states shown assume ERR was previously high.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.



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## logic symbol†

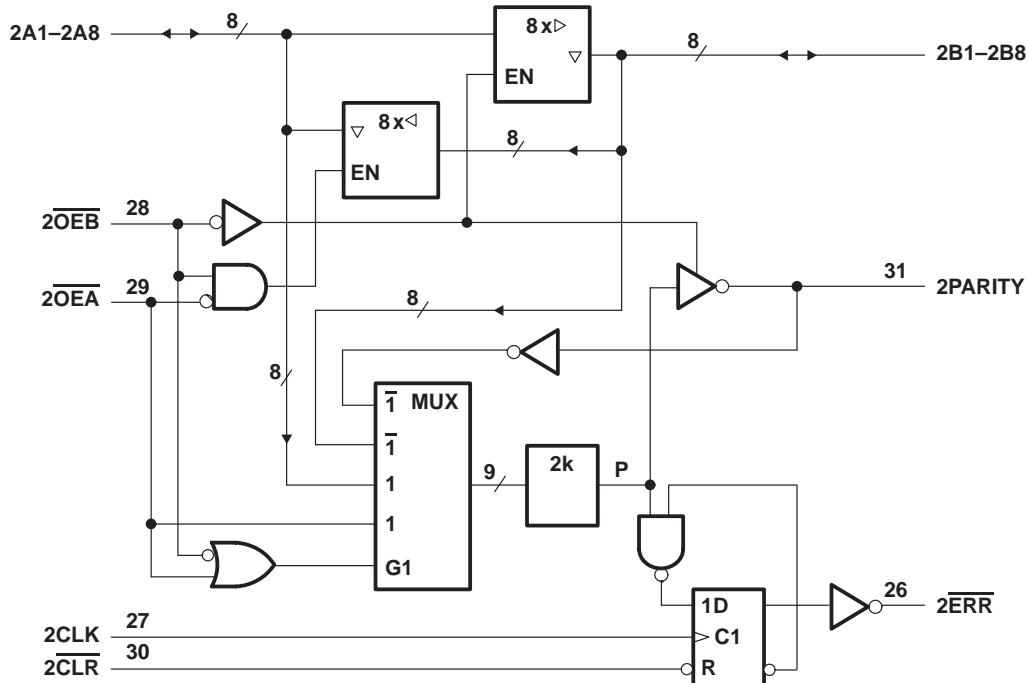
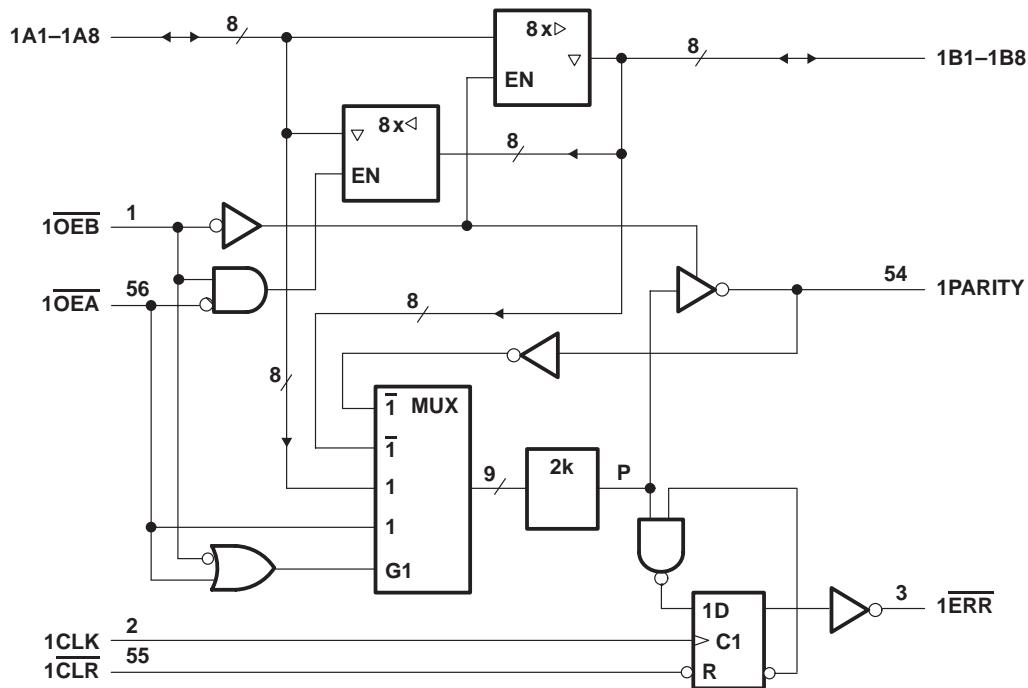


<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



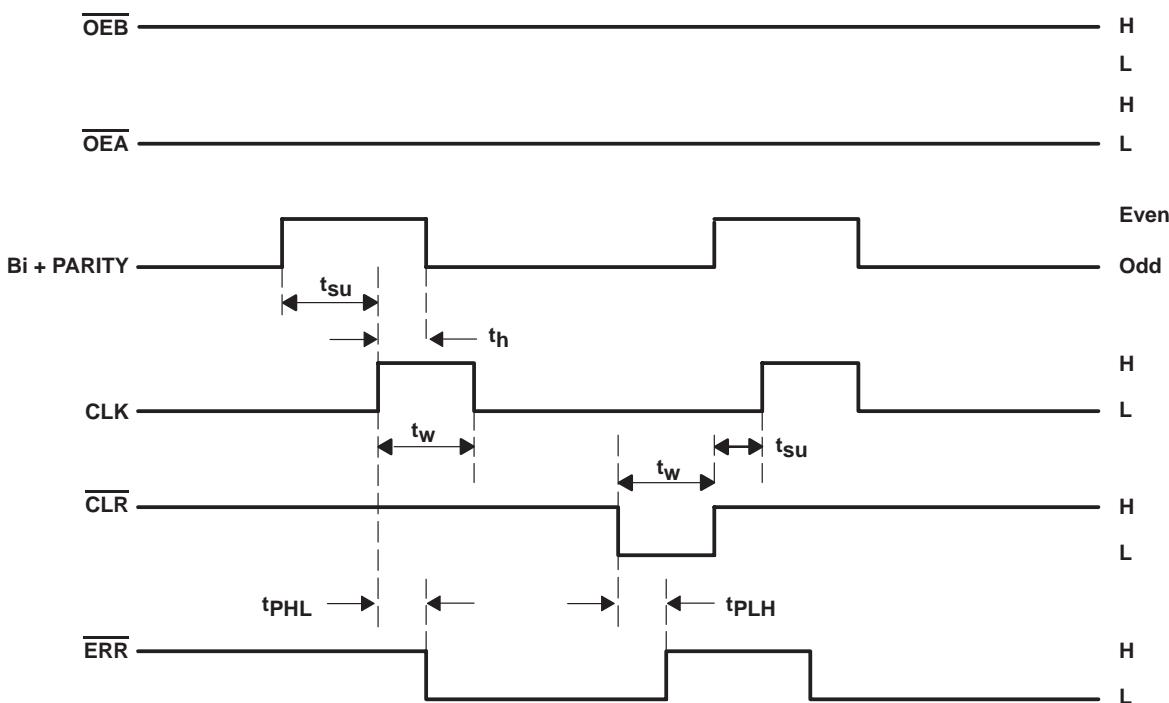
ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	CLK	POINT P‡	$\overline{ERR}_{n-1}^{\dagger}$		
H	↑	H	H	H	
H	↑	X	L	L	Sample
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of  $\overline{ERR}$  before any changes at CLR, CLK, or point P

‡ Location of point P is shown on local diagram.

### timing waveforms, error flag



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 450$ mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package .....	1.4 W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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## recommended operating conditions (see Note 3)

		54ACT16833			74ACT16833			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
I <sub>OH</sub>	High-level output current			-24			-24	mA
I <sub>OL</sub>	Low-level output current			24			24	mA
Δt/Δv	Input transition rise or fall rate	0	10		0	10		ns/V
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54ACT16833		74ACT16833		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I <sub>OH</sub>	ERR	V <sub>O</sub> = V <sub>CC</sub>	5.5 V		0.5		5		5	μA
V <sub>OH</sub>	All outputs except ERR	I <sub>OH</sub> = -50 μA	4.5 V	4.4		4.4		4.4		V
			5.5 V	5.4		5.4		5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.94		3.8		3.8			
		5.5 V	4.94		4.8		4.8			
	I <sub>OH</sub> = -75 mA†	5.5 V			3.85		3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0.1		0.1		0.1		V
		5.5 V		0.1		0.1		0.1		
		I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.44		0.44	
			5.5 V		0.36		0.44		0.44	
	I <sub>OL</sub> = 75 mA†	5.5 V				1.65		1.65		
I <sub>I</sub>	A or B ports	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		±1		±1	μA
I <sub>OZ</sub> ‡	Control inputs	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±0.5		±5		±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8		80		80	μA
ΔI <sub>CC</sub> §	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			0.9		1		1	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3.5					pF
C <sub>io</sub>	A or B ports, PARITY	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		11.5					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

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54ACT16833, 74ACT16833  
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

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**timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1 and timing waveforms)**

			$T_A = 25^\circ\text{C}$		54ACT16833		74ACT16833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration		CLK high or low	4	4	4	4	4	ns
			CLR low	4	4	4	4	4	
$t_{SU}$	Setup time before $CLK^\uparrow$		Bi + PARITY	7.5	7.5	7.5	7.5	7.5	ns
			CLR inactive	1.5	1.5	1.5	1.5	1.5	
$t_H$	Hold time, Bi + PARITY low after $CLK^\uparrow$			0	0	0	0	0	ns

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1 and timing waveforms)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT16833		74ACT16833		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	4	7.2	9.2	4	10.4	4	10.4	ns
$t_{PHL}$			3.2	6.6	9.6	3.2	10.7	3.2	10.7	
$t_{PLH}$	A	PARITY	3.9	7.9	12	3.9	13.5	3.9	13.5	ns
$t_{PHL}$			4.2	8.3	12.4	4.2	13.8	4.2	13.8	
$t_{PZH}$	$\overline{OEB}$ or $\overline{OEA}$	A or B	3.1	6.7	10.1	3.1	11.2	3.1	11.2	ns
$t_{PZL}$			3.8	7.9	11.6	3.8	13	3.8	13	
$t_{PHZ}$	$\overline{OEB}$ or $\overline{OEA}$	A or B	5.5	7.8	10	5.5	10.8	5.5	10.8	ns
$t_{PLZ}$			5	7.1	9.3	5	10.1	5	10.1	
$t_{PLH}$	$\overline{CLR}$	$\overline{ERR}$	10.7	13.1	15.4	10.7	15.8	10.7	15.8	ns
$t_{PHL}$	CLK		4.6	7.8	10.3	4.6	11.6	4.6	11.6	
$t_{PLH}$	$\overline{OEA}$	PARITY	4	8	11.8	4	13.2	4	13.2	ns
$t_{PHL}$			4.3	8.5	12.3	4.3	13.6	4.3	13.6	
$t_{PZH}$	$\overline{OEB}$	PARITY	2.6	5.7	8.5	2.6	9.5	2.6	9.5	ns
$t_{PZL}$			3.4	6.8	9.8	3.4	10.7	3.4	10.7	
$t_{PHZ}$	OEB	PARITY	5.6	7.9	9.5	5.6	10.2	5.6	10.2	ns
$t_{PLZ}$			5.1	7.2	9.1	5.1	9.7	5.1	9.7	

**operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER				TEST CONDITIONS		UNIT
	Outputs enabled	A to B	B to A	CL = 50 pF, f = 1 MHz	64	
		B to A	A to B		72	
		A to B	B to A		6	
$C_{pd}$	Power dissipation capacitance per transceiver				10.5	pF

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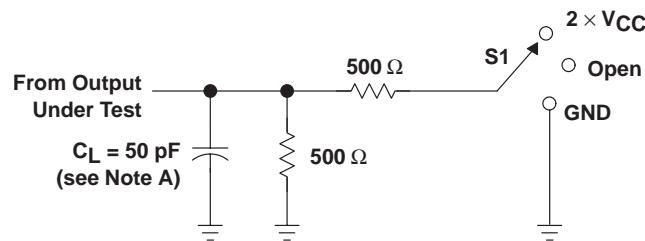


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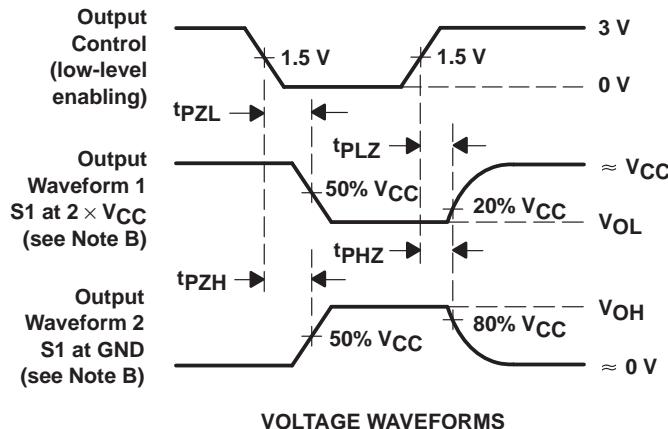
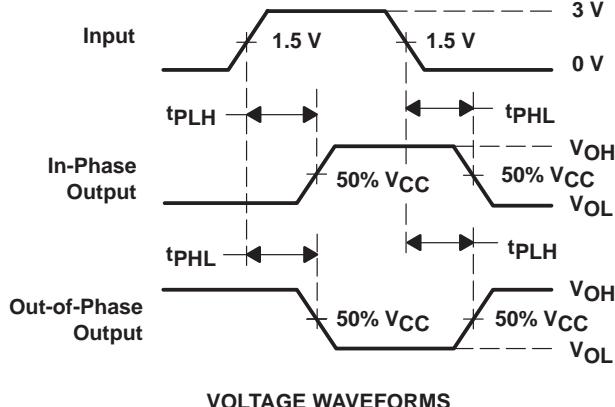
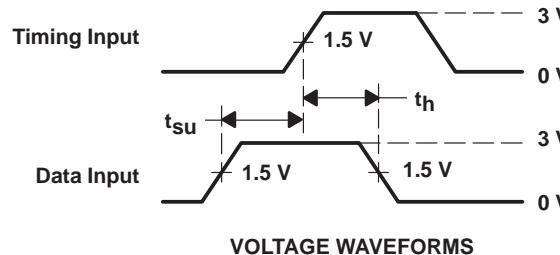
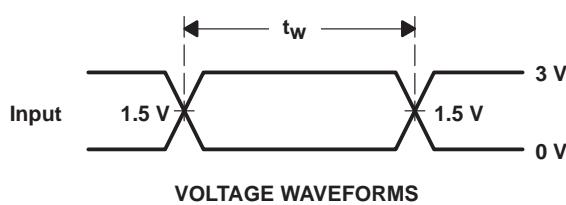
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## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.
- The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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