

# 54AC16543, 74AC16543 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS125B – MARCH 1990 – REVISED APRIL 1996

- **Members of the Texas Instruments Widebus™ Family**
- **3-State True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Pin Spacings**

## description

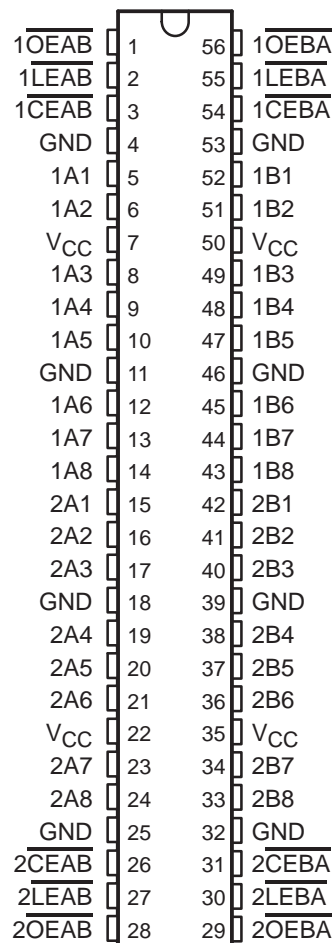
The 'AC16543 are 16-bit registered transceivers that contain two sets of D-type latches for temporary storage of data flowing in either direction. They can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ( $\overline{\text{LEAB}}$  or  $\overline{\text{LEBA}}$ ) and output-enable ( $\overline{\text{OEAB}}$  or  $\overline{\text{OEBA}}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ( $\overline{\text{CEAB}}$ ) input must be low to enter data from A or to output data to B. Having  $\overline{\text{CEAB}}$  low and  $\overline{\text{LEAB}}$  low makes the A-to-B latches transparent; a subsequent low-to-high transition at  $\overline{\text{LEAB}}$  puts the A latches in the storage mode. Data flow from B to A is similar, but requires using the  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{OEBA}}$  inputs.

The 74AC16543 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16543 is characterized for operation from –40°C to 85°C.

54AC16543 ... WD PACKAGE  
74AC16543 ... DL PACKAGE  
(TOP VIEW)



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**TEXAS  
INSTRUMENTS**

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FUNCTION TABLE†  
(each 8-bit section)

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B <sub>0</sub> ‡
L	L	L	L	L
L	L	L	H	H

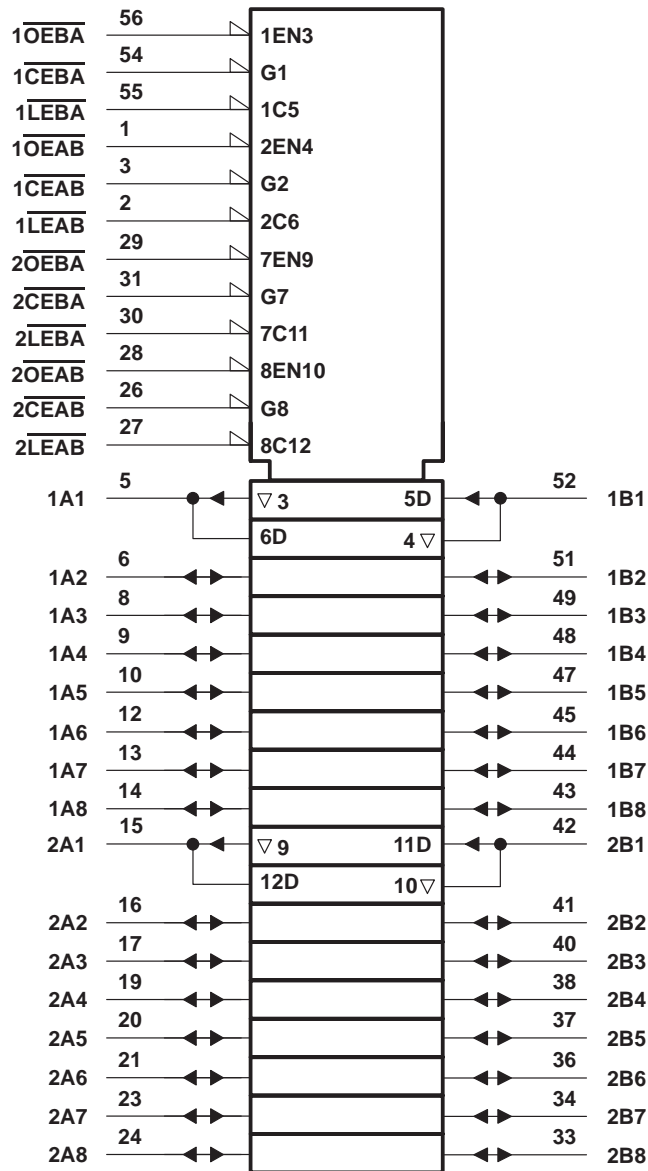
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

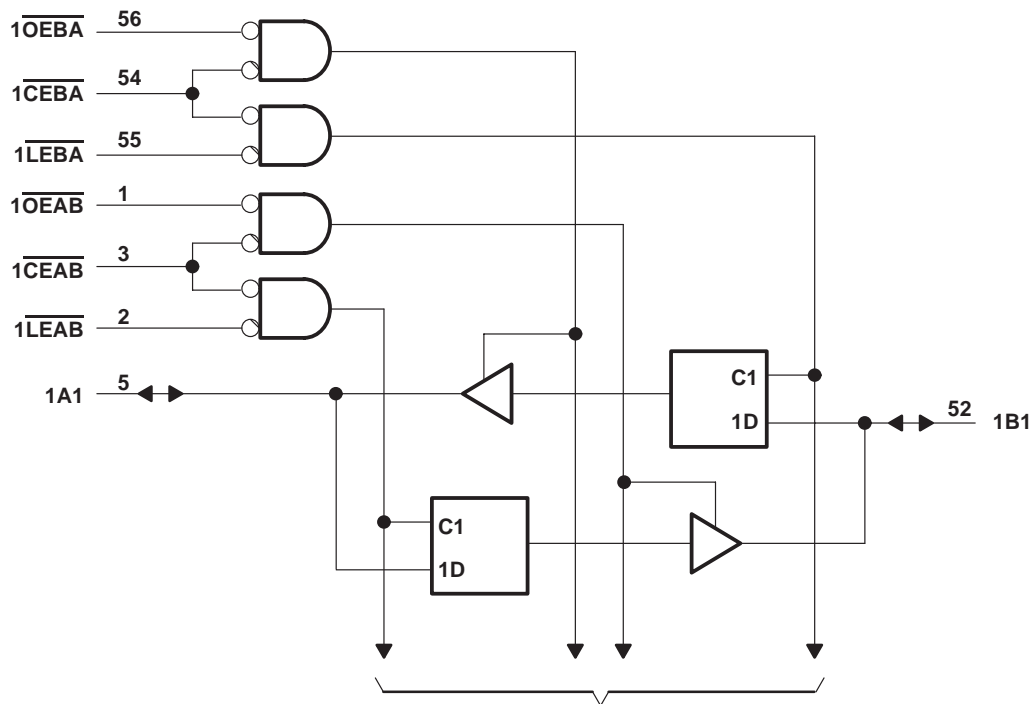
# 54AC16543, 74AC16543

## 16-BIT REGISTERED TRANSCEIVERS

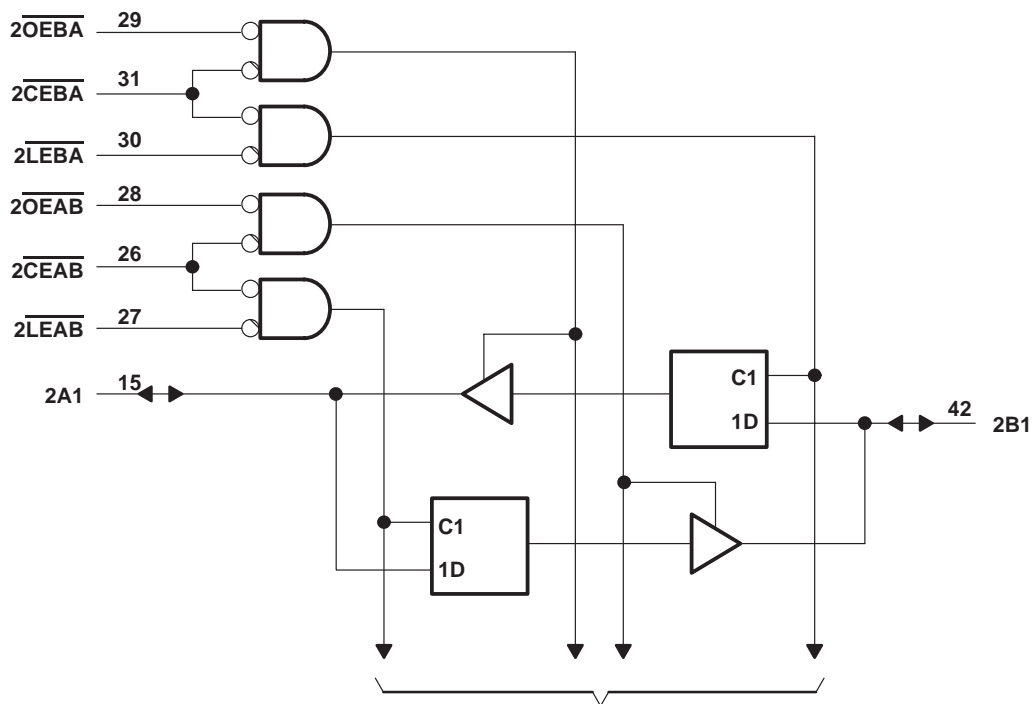
## WITH 3-STATE OUTPUTS

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**logic diagram (positive logic)**



## To Seven Other Channels



## To Seven Other Channels

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±400 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (in still air)(see Note 2): DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

**recommended operating conditions (see Note 3)**

			54AC16543			74AC16543			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage		3	5	5.5	3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3$ V	2.1			2.1			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 5.5$ V	3.85			3.85			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3$ V			0.9			0.9	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 5.5$ V			1.65			1.65	
$V_I$	Input voltage		0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage		0		$V_{CC}$	0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3$ V			–4			–4	mA
		$V_{CC} = 4.5$ V			–24			–24	
		$V_{CC} = 5.5$ V			–24			–24	
$I_{OL}$	Low-level output current	$V_{CC} = 3$ V			12			12	mA
		$V_{CC} = 4.5$ V			24			24	
		$V_{CC} = 5.5$ V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
$T_A$	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54AC16543		74AC16543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = –4 mA	3 V	2.58			2.48		2.48		
	I <sub>OL</sub> = –24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I <sub>OH</sub> = –75 mA†	5.5 V				3.85		3.85		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I <sub>OL</sub> = 12 mA	3 V			0.36		0.44		0.44	
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I <sub>OL</sub> = 75 mA†	5.5 V					1.65		1.65	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		±1		±1	µA
I <sub>OZ</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±0.5		±5		±5	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		8		80		80	µA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3					pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		11.5					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

**timing requirements over recommended operating free-air temperature range,**  
**V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		54AC16543		74AC16543		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low	5		5		5		ns
t <sub>su</sub>	Setup time, data before $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ ↑	1		1		1		ns
t <sub>h</sub>	Hold time, data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ ↑	3.5		3.5		3.5		ns

**timing requirements over recommended operating free-air temperature range,**  
**V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		54AC16543		74AC16543		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low	4		4		4		ns
t <sub>su</sub>	Setup time, data before $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ ↑	1		1		1		ns
t <sub>h</sub>	Hold time, data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ ↑	3		3		3		ns

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**switching characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC16543		74AC16543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	3.2	8.6	12.5	3.2	13.9	3.2	13.9	ns
$t_{PLH}$	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	4.6	11.8	16	4.6	18	4.6	18	ns
$t_{PHL}$			4.6	11.3	15.4	4.6	16.8	4.6	16.8	
$t_{PZH}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3.7	10	14	3.7	15.8	3.7	15.8	ns
$t_{PZL}$			4.6	12.7	17.7	4.6	19.8	4.6	19.8	
$t_{PHZ}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.7	7.8	10.1	4.7	10.8	4.7	10.8	ns
$t_{PLZ}$			4.3	7.3	9.7	4.3	10.4	4.3	10.4	
$t_{PZH}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3.5	9.7	13.9	3.5	15.7	3.5	15.7	ns
$t_{PZL}$			4.5	12.5	17.6	4.5	19.7	4.5	19.7	
$t_{PHZ}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.8	7.5	9.6	4.8	10.2	4.8	10.2	ns
$t_{PLZ}$			4.1	6.8	9.2	4.1	9.8	4.1	9.8	

**switching characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC16543		74AC16543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	2.7	5.2	7.8	2.7	8.8	2.7	8.8	ns
$t_{PHL}$			2.9	5.5	8.3	2.9	9.2	2.9	9.2	
$t_{PLH}$	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	3.9	7	10.2	3.9	11.5	3.9	11.5	ns
$t_{PHL}$			3.7	6.7	9.9	3.7	10.9	3.7	10.9	
$t_{PZH}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	3	5.8	8.7	3	9.8	3	9.8	ns
$t_{PZL}$			3.6	6.7	10.3	3.6	11.5	3.6	11.5	
$t_{PHZ}$	$\overline{CEBA}$ or $\overline{CEAB}$	A or B	4.2	6.5	8.7	4.2	9.3	4.2	9.3	ns
$t_{PLZ}$			4	5.9	8.2	4	8.8	4	8.8	
$t_{PZH}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	2.9	5.6	8.5	2.9	9.6	2.9	9.6	ns
$t_{PZL}$			3.5	6.6	10.2	3.5	11.3	3.5	11.3	
$t_{PHZ}$	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.2	6.3	8.4	4.2	8.9	4.2	8.9	ns
$t_{PLZ}$			3.7	5.6	7.9	3.7	8.4	3.7	8.4	

**operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER			TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$		53	pF
		Outputs disabled			11	

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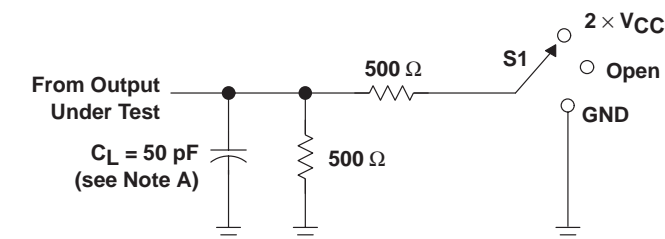
# 54AC16543, 74AC16543

## 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

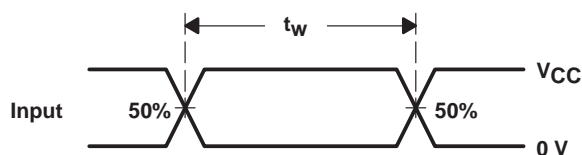
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#### PARAMETER MEASUREMENT INFORMATION

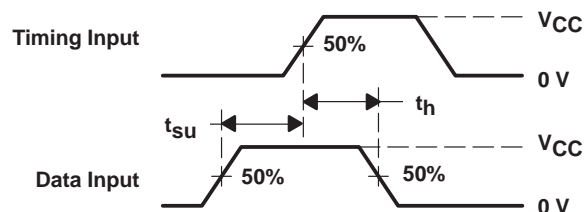


LOAD CIRCUIT

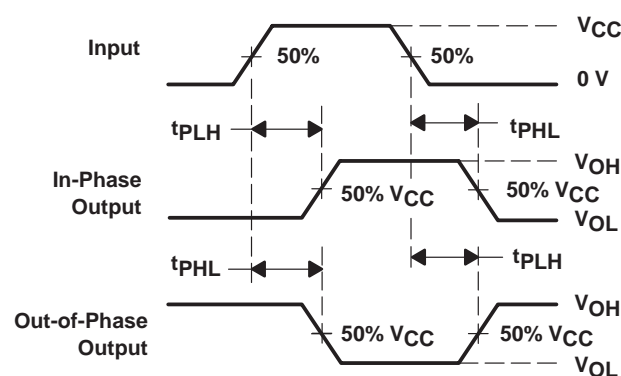
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



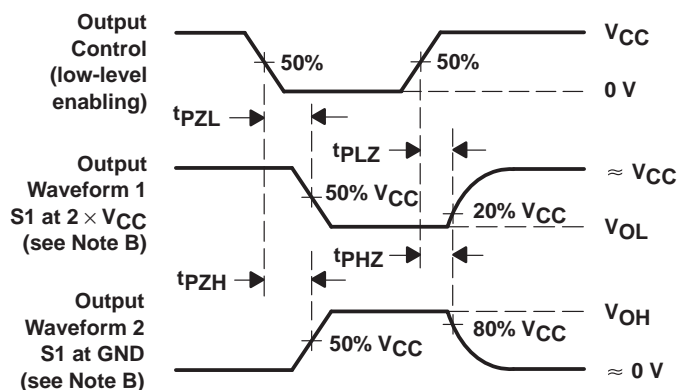
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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