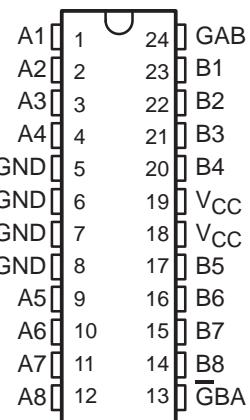


74ACT11620  
OCTAL BUS TRANSCEIVER  
WITH 3-STATE OUTPUTS

SCAS060A – D2957, JULY 1987 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- Local Bus-Latch Capability
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V<sub>CC</sub> and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE  
(TOP VIEW)



**description**

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ( $\overline{GBA}$  and  $GAB$ ).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of  $\overline{GBA}$  and  $GAB$ . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary for the 74ACT11620.

The 74ACT11620 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
GBA	GAB	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

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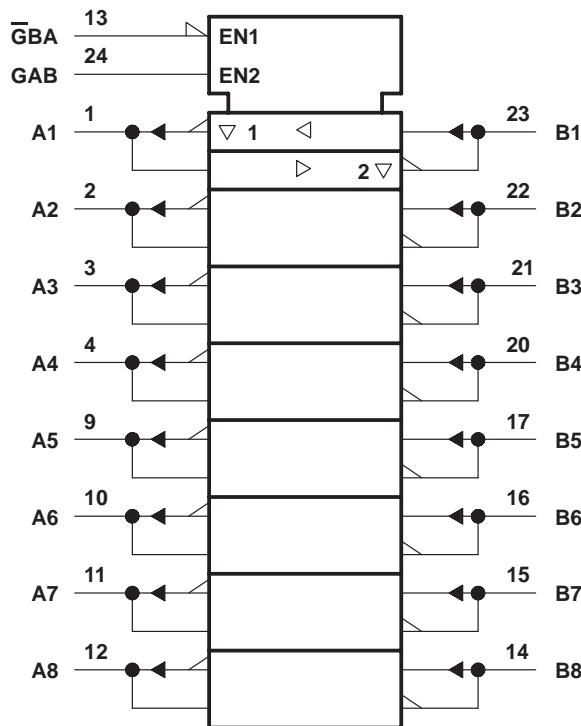


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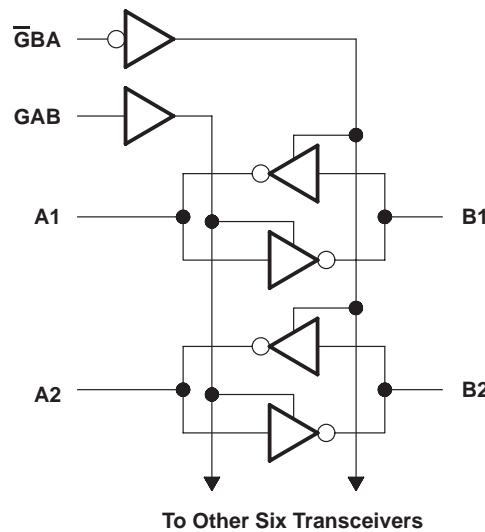
**74ACT11620**  
**OCTAL BUS TRANSCEIVER**  
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**logic symbol†**



**logic diagram (positive logic)**



† This symbol is in accordance with ANSI/IEEE Std 91-1984  
 and IEC Publication 617-12.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	± 20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	± 50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	± 50 mA
Continuous current through $V_{CC}$ or GND .....	± 200 mA
Storage temperature range .....	–65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**recommended operating conditions**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24	mA
I <sub>OL</sub>	Low-level output current		24	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

**electrical characteristics over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
			MIN	TYP	MAX				
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4		4.4	V			
		5.5 V	5.4		5.4				
	I <sub>OH</sub> = -24 mA	4.5 V	3.94		3.8				
		5.5 V	4.94		4.8				
	I <sub>OH</sub> = -75 mA†	5.5 V			3.85				
	I <sub>OL</sub> = 50 μA	4.5 V		0.1	0.1		V		
V <sub>OL</sub>		5.5 V		0.1	0.1				
		4.5 V		0.36	0.44				
		5.5 V		0.36	0.44				
		5.5 V			1.65				
I <sub>OZ</sub>	A or B ports‡	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.5	± 5	μA		
I <sub>I</sub>	GBA or GAB	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		± 0.1	± 1			
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		8	8	μA		
ΔI <sub>CC</sub> §		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.9	1			
C <sub>i</sub>	GBA or GAB	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4		pF		
C <sub>o</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		12				

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

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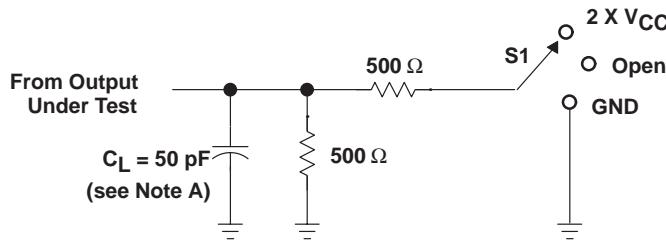
**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	1.5	5.7	8.5	1.5	9.4	ns
t <sub>PHL</sub>			1.5	5.9	7.7	1.5	8.6	
t <sub>PZH</sub>	G <sub>BA</sub>	A	1.5	7.2	9.1	1.5	10.3	ns
t <sub>PZL</sub>			1.5	7.1	9.2	1.5	10.1	
t <sub>PHZ</sub>	G <sub>BA</sub>	A	1.5	7.9	9.6	1.5	10.4	ns
t <sub>PLZ</sub>			1.5	8.3	10	1.5	10.9	
t <sub>PZH</sub>	G <sub>AB</sub>	B	1.5	7.5	10.2	1.5	11.3	ns
t <sub>PZL</sub>			1.5	7.7	9.8	1.5	11	
t <sub>PHZ</sub>	G <sub>AB</sub>	B	1.5	7.2	8.9	1.5	9.4	ns
t <sub>PLZ</sub>			1.5	7.2	8.9	1.5	9.6	

**operating characteristics, V<sub>CC</sub> = 5 V, TA = 25°C**

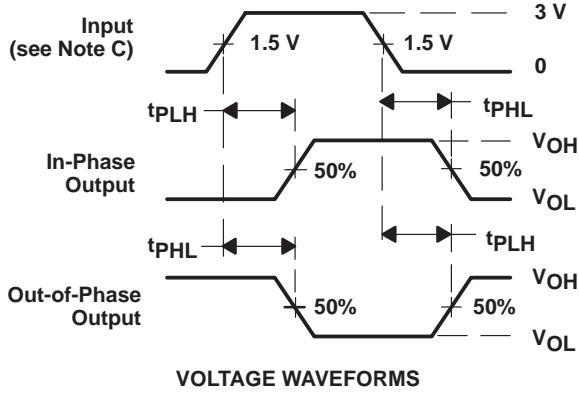
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per transceiver	Outputs enabled C <sub>L</sub> = 50 pF, f = 1 MHz	54	pF
		11	

PARAMETER MEASUREMENT INFORMATION

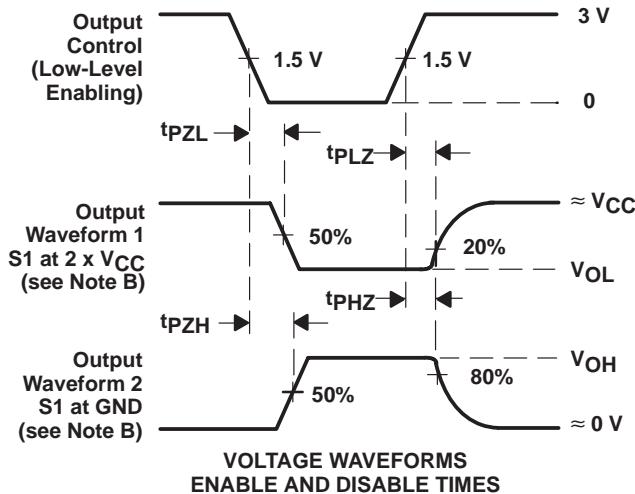


TEST	S1
$t_{PLH}/t_{PHL}$	OPEN
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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