

DATA SHEET

74ABT2240

Octal inverting buffer with 30 Ω series
termination resistors (3-State)

Product data
Supersedes data of 1998 Jan 16

2003 Apr 25

Octal inverting buffer with 30 Ω series termination resistors (3-State)

74ABT2240

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Outputs include series resistance of 30 Ω , making external termination resistors unnecessary
- Output capability: +12 mA/–32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Same part as 74ABT240-1

DESCRIPTION

The 74ABT2240 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed.

The 74ABT2240 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

The 74ABT2240 is designed with 30 Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

The 74ABT2240 is the same as the 74ABT240-1. The part number has been changed to reflect industry standards.

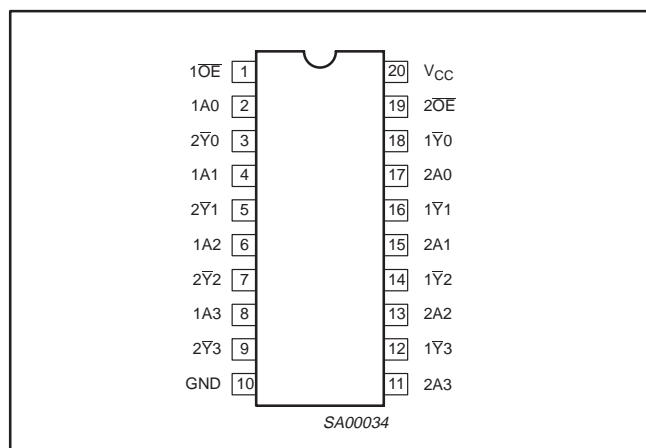
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}$; $GND = 0\text{ V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to \overline{Yn}	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$	2.8 4.3	ns
C_{IN}	Input capacitance	$V_I = 0\text{ V}$ or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{ V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{ V}$	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
20-Pin Plastic DIP	–40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABT2240N	SOT146-1
20-Pin plastic SO	–40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABT2240D	SOT163-1
20-Pin Plastic TSSOP Type I	–40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	74ABT2240PW	SOT360-1

PIN CONFIGURATION



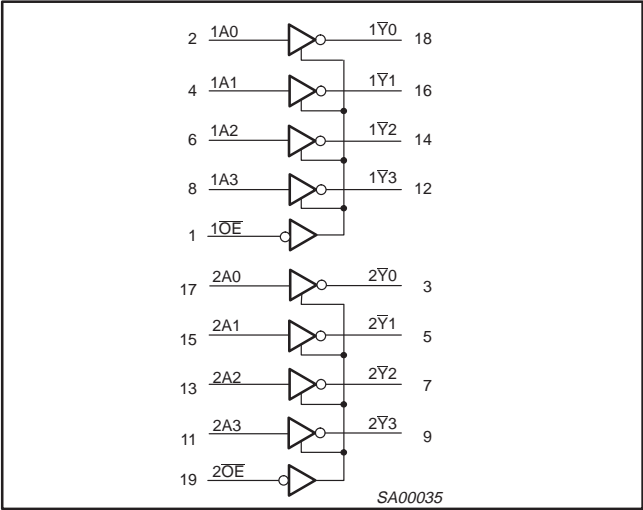
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0 V)
20	V_{CC}	Positive supply voltage

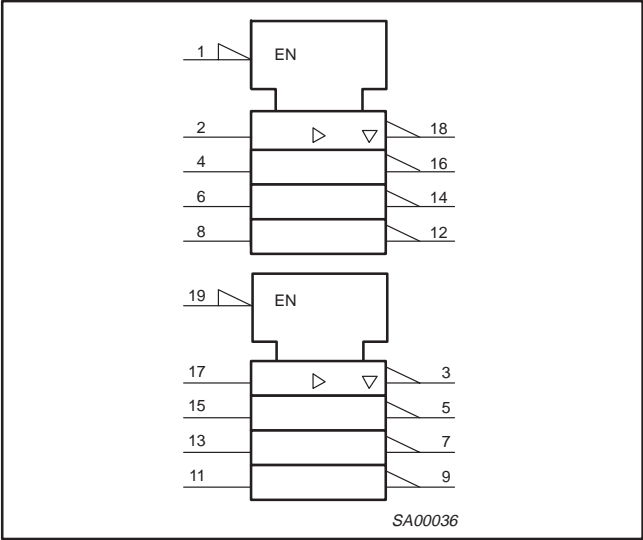
Octal inverting buffer with 30 Ω series termination resistors (3-State)

74ABT2240

LOGIC SYMBOL



LOGIC SYMBOL (IEE/IEC)

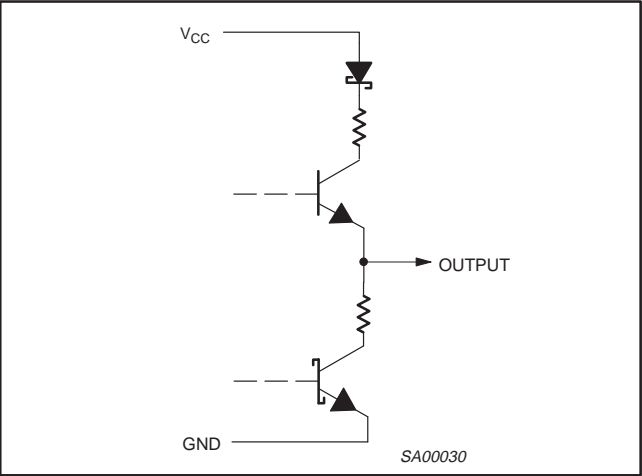


FUNCTION TABLE

INPUTS				OUTPUTS	
1OE	1An	2OE	2An	1Yn	2Yn
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

SCHEMATIC OF EACH OUTPUT



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0 V	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0 V	−50	mA
V _{OUT}	DC output voltage ³	output in Off or HIGH state	−0.5 to +5.5	V
I _{OUT}	DC output current	output in LOW state	128	mA
T _{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal inverting buffer with 30 Ω series termination resistors (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25 °C			T _{amb} = –40 °C to +85 °C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5 V; I _{IK} = –18 mA	–	–0.9	–1.2	–	–1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; I _{OH} = –3 mA; V _I = V _{IL} or V _{IH}	2.5	2.9	–	2.5	–	V
		V _{CC} = 5.0 V; I _{OH} = –3 mA; V _I = V _{IL} or V _{IH}	3.0	3.4	–	3.0	–	V
		V _{CC} = 4.5 V; I _{OH} = –32 mA; V _I = V _{IL} or V _{IH}	2.0	2.4	–	2.0	–	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 5 mA; V _I = V _{IL} or V _{IH}	–	0.32	0.55	–	0.55	V
		V _{CC} = 4.5 V; I _{OL} = 12 mA; V _I = V _{IL} or V _{IH}	–	–	0.8	–	0.8	V
I _I	Input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V	–	±0.01	±1.0	–	±1.0	µA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V	–	±5.0	±100	–	±100	µA
I _{PU/PD}	Power-up/down 3-State output current ³	V _{CC} = 2.1 V; V _O = 0.5 V; V _I = GND or V _{CC} ; V _{OE} = Don't care	–	±5.0	±50	–	±50	µA
I _{OZH}	3-State output HIGH current	V _{CC} = 5.5 V; V _O = 2.7 V; V _I = V _{IL} or V _{IH}	–	0.01	50	–	50	µA
I _{OZL}	3-State output LOW current	V _{CC} = 5.5 V; V _O = 0.5 V; V _I = V _{IL} or V _{IH}	–	–0.01	–50	–	–50	µA
I _{CEx}	Output high leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}	–	5.0	50	–	50	µA
I _O	Output current ¹	V _{CC} = 5.5 V; V _O = 2.5 V	–50	–100	–180	–50	–180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5 V; Outputs HIGH, V _I = GND or V _{CC}	–	50	250	–	250	µA
I _{CCL}		V _{CC} = 5.5 V; Outputs LOW, V _I = GND or V _{CC}	–	24	30	–	30	mA
I _{CCZ}		V _{CC} = 5.5 V; Outputs 3-State; V _I = GND or V _{CC}	–	50	250	–	250	µA
ΔI _{CC}	Additional supply current per input pin ²	Outputs enabled, one data input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V	–	0.5	1.5	–	1.5	mA
		Outputs 3-State, one data input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V	–	0.5	1.5	–	1.5	mA
		Outputs 3-State, one enable input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V	–	0.5	1.5	–	1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 msec. From $V_{CC} = 2.1\text{ V}$ to $V_{CC} = 5\text{ V} \pm 10\%$ a transition time of up to 100 μsec is permitted.

Octal inverting buffer with 30 Ω series termination resistors (3-State)

74ABT2240

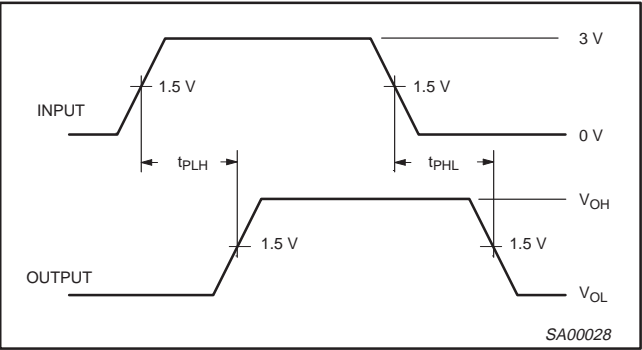
AC CHARACTERISTICS

GND = 0 V; $t_R = t_F = 2.5\text{ ns}$; $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$

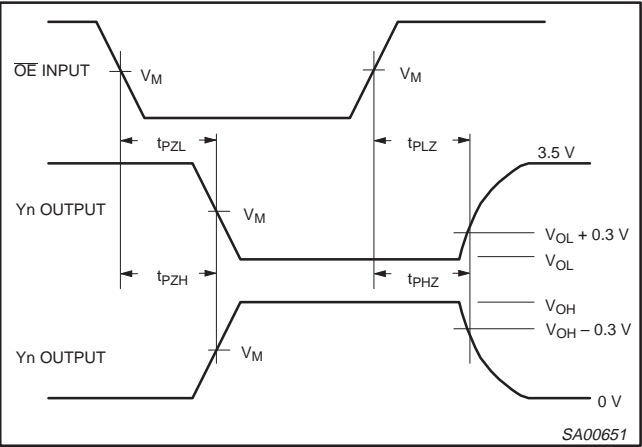
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V			T _{amb} = -40 °C to +85 °C V _{CC} = +5.0 V ±0.5 V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay An to Yn	1	1.0 3.0	2.8 4.3	4.0 5.8	1.0 3.0	4.9 6.0	ns
t _{PZH} t _{PZL}	Output enable time to HIGH and LOW level	2	1.5 4.2	3.4 5.5	4.7 7.6	1.5 4.2	5.8 8.4	ns
t _{PHZ} t _{PLZ}	Output disable time from HIGH and LOW level	2	1.9 2.5	4.1 3.4	5.0 5.8	1.9 2.5	5.6 6.4	ns

AC WAVEFORMS

$V_M = 1.5\text{ V}$, $V_{IN} = \text{GND to } 3.0\text{ V}$

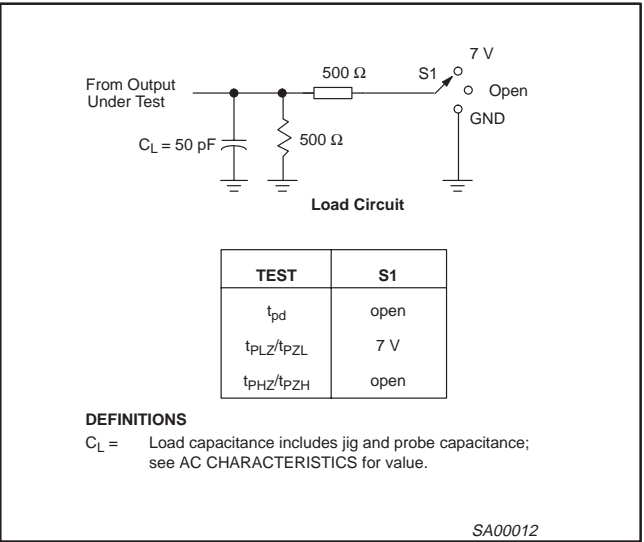


Waveform 1. Waveforms Showing the Input (An) to Output (\bar{Y}_n) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

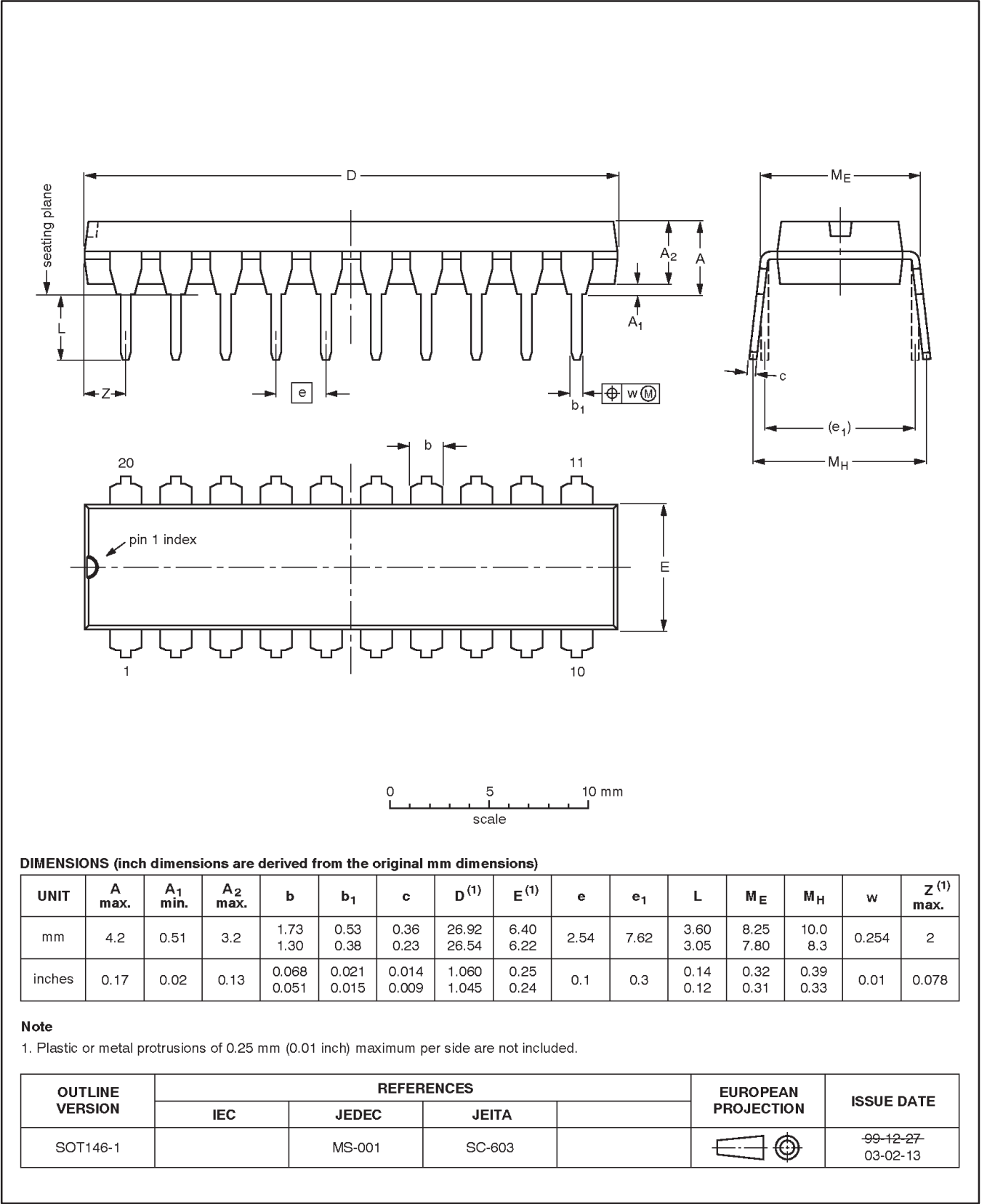


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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

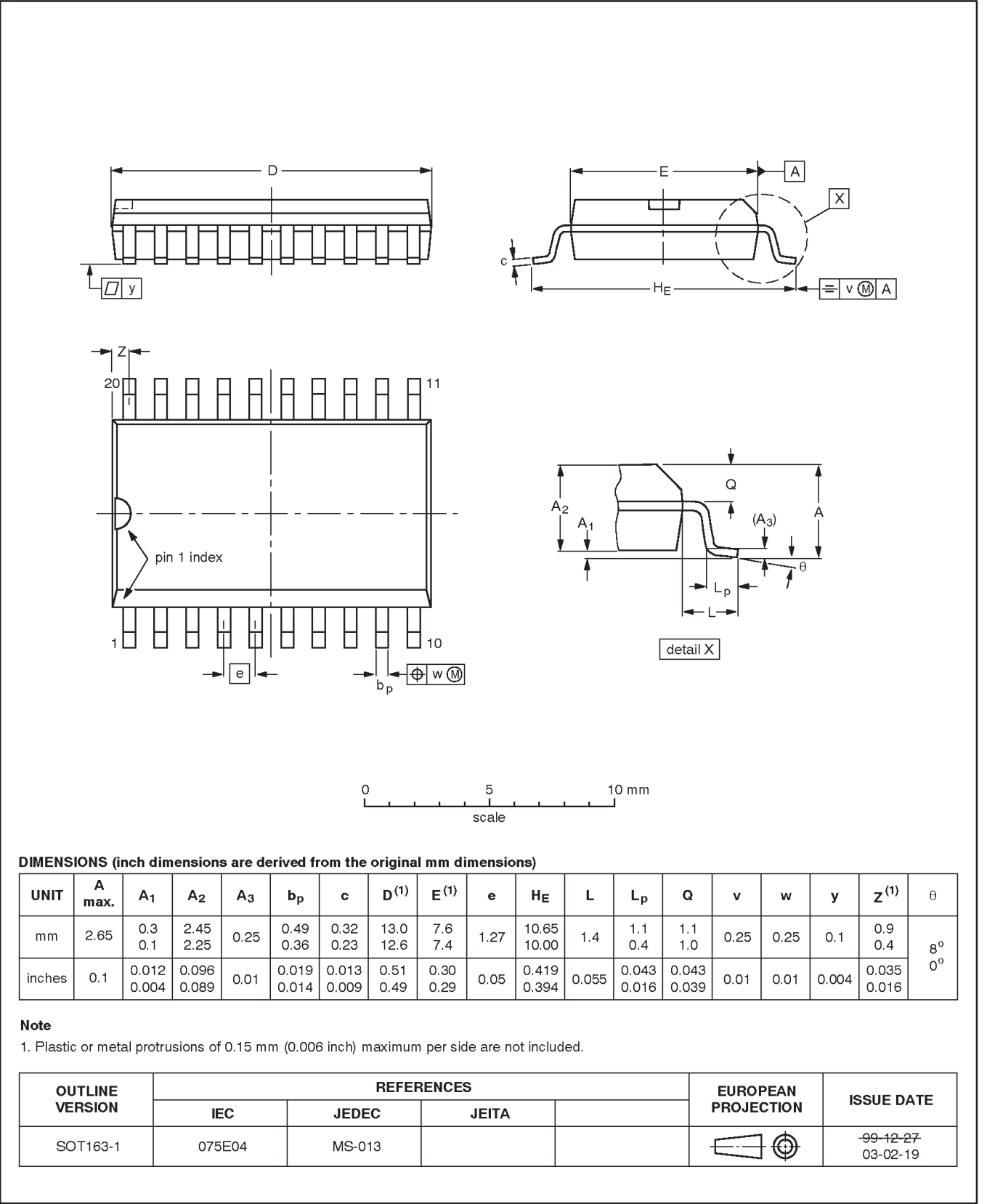


Octal inverting buffer with 30 Ω series termination resistors (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

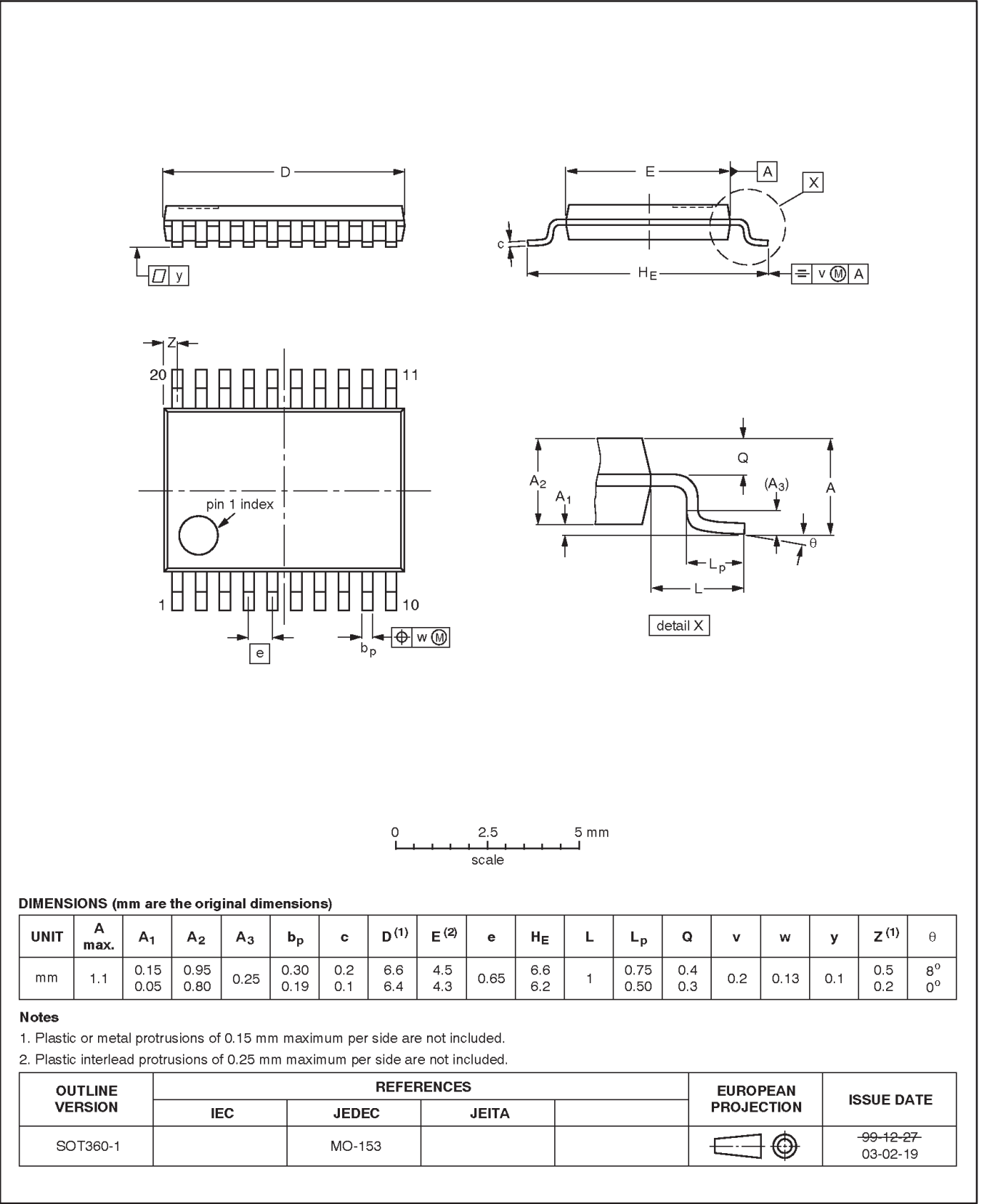


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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



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REVISION HISTORY

Rev	Date	Description
3	20030425	<p>Product data (9397 750). ECN 853-1626 29854 of 22 April 2003. Supersedes Product specification of 16 January 1998 (9397 750 03463).</p> <p>Modifications:</p> <ul style="list-style-type: none"> Ordering information table on page 2: delete "North America" column; re-name "Outside Nort America" column to "Order code"; remove 74ABT2240DB variant. DC Electrical Characteristics table on page 4, Symbol ΔI{CC}, Test Condition "Outputs 3-State, one data input at 3.4 V, other inputs at V_{CC} or GND; $V_{CC} = 5.5$ V": <ul style="list-style-type: none"> under Limit $T_{amb} = 25$ °C: change Typ. value from 50 μA to 0.5 mA; change Max. value from 250 μA to 1.5 mA. under Limit $T_{amb} = -40$ °C to +85 °C: change Max from 250 μA to 1.5 mA.
_2	19980116	<p>Product specification (9397 750 03463). ECN 853-1626 18865 of 16 January 1998. Supersedes data of 1996 Oct 08.</p>

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Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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