### INTEGRATED CIRCUITS

## DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT643 Octal bus transceiver; 3-state; true/inverting

Product specification
File under Integrated Circuits, IC06

December 1990





# Octal bus transceiver; 3-state; true/inverting

### 74HC/HCT643

#### **FEATURES**

- · Octal bidirectional bus interface
- True and inverting 3-state outputs
- · Output capability: bus driver
- I<sub>CC</sub> category: MSI

#### **GENERAL DESCRIPTION**

The 74HC/HCT643 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT643 are octal transceivers featuring true and inverting 3-state bus compatible outputs in both send and receive directions.

The "643" features an output enable  $(\overline{OE})$  input for easy cascading and a send/receive (DIR) for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated.

#### **QUICK REFERENCE DATA**

GND = 0 V;  $T_{amb} = 25 \, ^{\circ}C$ ;  $t_r = t_f = 6 \, \text{ns}$ 

CVMDOL	DADAMETED	CONDITIONS	TYI	LINIT		
SYMBOL	PARAMETER	CONDITIONS	НС	нст	UNIT	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$				
	A <sub>n</sub> to B <sub>n</sub> ; inverting		7	8	ns	
	B <sub>n</sub> to A <sub>n</sub> ; true		8	11	ns	
C <sub>I</sub>	input capacitance		3.5	3.5	pF	
C <sub>I/O</sub>	input/output capacitance		10	10	pF	
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	42	44	pF	

#### **Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz

 $f_o$  = output frequency in MHz

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$ 

For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$ 

#### **ORDERING INFORMATION**

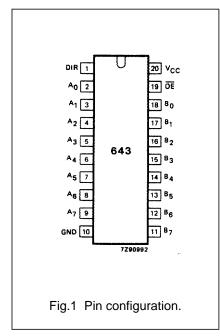
See "74HC/HCT/HCU/HCMOS Logic Package Information".

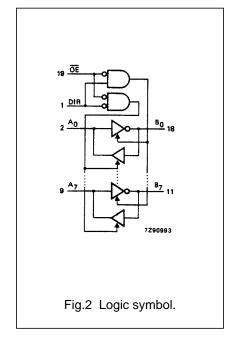
# Octal bus transceiver; 3-state; true/inverting

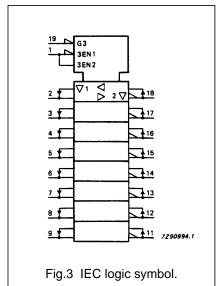
### 74HC/HCT643

#### **PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>7</sub>	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B <sub>0</sub> to B <sub>7</sub>	data inputs/outputs
19	ŌĒ	output enable input (active LOW)
20	V <sub>CC</sub>	positive supply voltage







### **FUNCTION TABLE**

INP	UTS	INPUTS/OUTPUTS					
ŌĒ	DIR	A <sub>n</sub>	B <sub>n</sub>				
L	L	A = B	inputs				
L	Н	inputs	$B = \overline{A}$				
Н	Х	Z	Z				

#### **Notes**

1. H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

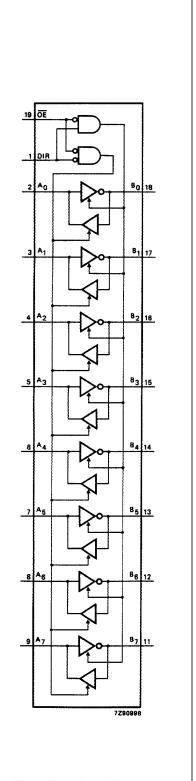


Fig.4 Functional diagram.

Philips Semiconductors Product specification

# Octal bus transceiver; 3-state; true/inverting

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#### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

### **AC CHARACTERISTICS FOR 74HC**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
SYMBOL		74HC									
STWIBOL		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay  A <sub>n</sub> to B <sub>n</sub> ;  inverting		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay  B <sub>n</sub> to A <sub>n</sub> ;  non-inverting (true)		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>			39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>PHZ</sub> / t <sub>PLZ</sub>			44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5 and Fig.6

Philips Semiconductors Product specification

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#### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

#### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT						
A <sub>n</sub>	1.50						
B <sub>n</sub>	0.40						
ŌE	1.50						
DIR	0.90						

#### **AC CHARACTERISTICS FOR 74HCT**

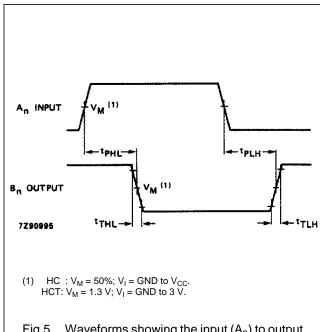
 $GND = 0 \text{ V; } t_r = t_f = 6 \text{ ns; } C_L = 50 \text{ pF}$ 

	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS		
SYMBOL		74HCT										
		+25		-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.		(		
t <sub>PHL</sub> / t <sub>PLH</sub>	$\begin{array}{c} \text{propagation delay} \\ A_n \text{ to } B_n; \\ \text{inverting} \end{array}$		10	20		25		30	ns	4.5	Fig.5	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay  B <sub>n</sub> to A <sub>n</sub> ;  non-inverting (true)		13	23		29		35	ns	4.5	Fig.6	
t <sub>PZH</sub> / t <sub>PZL</sub>			16	30		38		45	ns	4.5	Fig.7	
t <sub>PHZ</sub> / t <sub>PLZ</sub>			17	30		38		45	ns	4.5	Fig.7	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.5 and Fig.6	

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#### **AC WAVEFORMS**



B<sub>n</sub> INPUT

V<sub>M</sub>

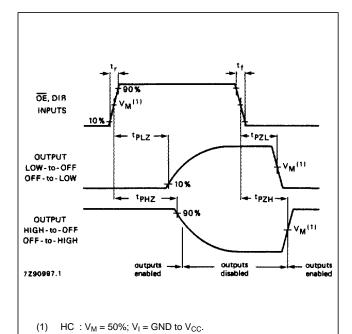
(1)

HC: V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.

HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

Fig.6 Waveforms showing the input (B<sub>n</sub>) to output (A<sub>n</sub>) propagation delays and the output transition times.

Fig.5 Waveforms showing the input  $(A_n)$  to output  $(B_n)$  propagation delays and the output transition times.



HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

Fig.7 Waveforms showing the 3-state enable and disable times for OE and DIR inputs.

### **PACKAGE OUTLINES**

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".