TEXAS INSTRUMENTS

CY74FCT16827T
CY74FCT162827T

20-Bit Buffers/Line Drivers

SCCS064B - August 1994 - Revised September 2001

Features

- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16827T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162827T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25˚C**

Functional Description

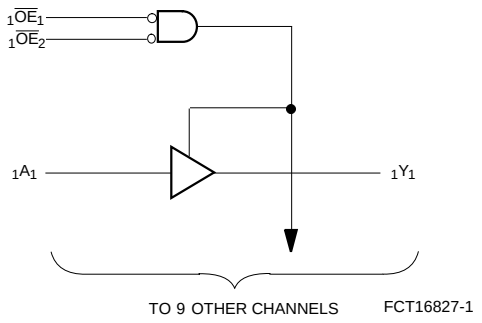
The CY74FCT16827T 20-bit buffer/line driver and the CY74FCT162827T 20-bit buffer/line driver provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. These parts can be used as a single 20-bit buffer or two 10-bit buffers. Each 10-bit buffer has a pair of NANDed $\overline{OE}$ for increased flexibility.

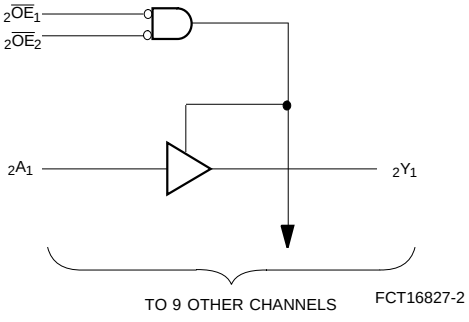
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16827T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162827T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162827T is ideal for driving transmission lines.

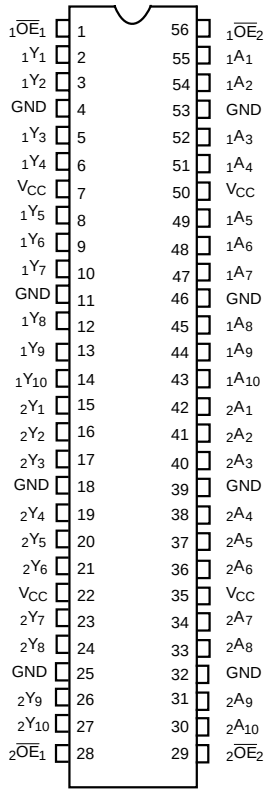
Logic Block Diagrams





Pin Configuration

SSOP/TSSOP
Top View



FCT16827-3

Pin Description

Name	Description
$\overline{OE}$	Output Enable Inputs (Active LOW)
A	Data Inputs
Y	Three-State Outputs

Function Table[1]

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

DC Input Voltage ..... –0.5V to +7.0V

DC Output Voltage ..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... –60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	–80	–140	–200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	–50		–180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[7]			±1	µA

Output Drive Characteristics for CY74FCT16827T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=–32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.Z = HIGH Impedance.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Tested at +25°C.

Output Drive Characteristics for CY74FCT162827T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Min.	Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V, V_{IN}≥V_{CC}–0.2V	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[8]	—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1$=$\overline{OE}_2$=GND,	V_{IN}=V_{CC} or V_{IN}=GND	—	60	100	µA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}_1$=$\overline{OE}_2$=GND	V_{IN}=V_{CC} or V_{IN}=GND	—	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	—	0.9	2.3	
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Twenty Bits Toggling, $\overline{OE}_1$=$\overline{OE}_2$=GND	V_{IN}=V_{CC} or V_{IN}=GND	—	3.0	5.5[11]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.0	20.5[11]	

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = I_{CC}+$\Delta I_{CC} D_H N_T$+$I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	Condition[13]	CY74FCT16827AT CY74FCT162827AT		CY74FCT162827BT		Unit	Fig. No.[13]
			Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to Y	C_L=50 pF R_L=500Ω	1.5	8.0	1.5	5.0	ns	1, 3
		C_L=300 pF R_L=500Ω	1.5	15.0	1.5	13.0		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	12.0	1.5	8.0	ns	1, 7, 8
		C_L=300 pF R_L=500Ω	1.5	23.0	1.5	15.0		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y	C_L=5 pF R_L=500Ω	1.5	9.0	1.5	6.0	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	10.0	1.5	7.0		
$t_{SK(O)}$	Output Skew[14]		—	0.5	—	0.5	ns	—

Parameter	Description	Condition[12]	CY74FCT16827CT CY74FCT162827CT		Unit	Fig. No.[13]
			Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay A to Y	C_L=50 pF R_L=500Ω	1.5	4.2	ns	1, 3
		C_L=300 pF R_L=500Ω	1.5	10.0		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y	C_L=50 pF R_L=500Ω	1.5	5.6	ns	1, 7, 8
		C_L=300 pF R_L=500Ω	1.5	14.0		
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y	C_L=5 pF R_L=500Ω	1.5	5.7	ns	1, 7, 8
		C_L=50 pF R_L=500Ω	1.5	6.0		
$t_{SK(O)}$	Output Skew[14]		—	0.5	ns	—

Notes:
12. Minimum limits are specified but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.
14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16827CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16827CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT16827ATPVC/PVCT	Z56	56-Lead (240-Mil) SSOP	Industrial

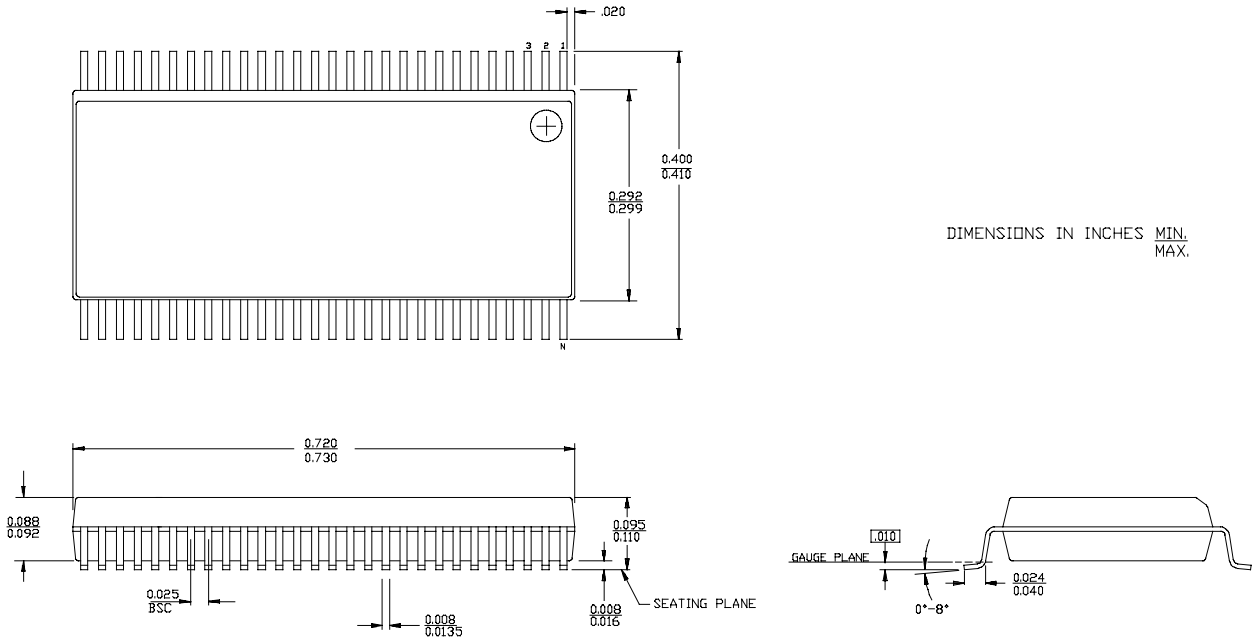
Document #: 38–00393–C

Ordering Information CY74FCT162827

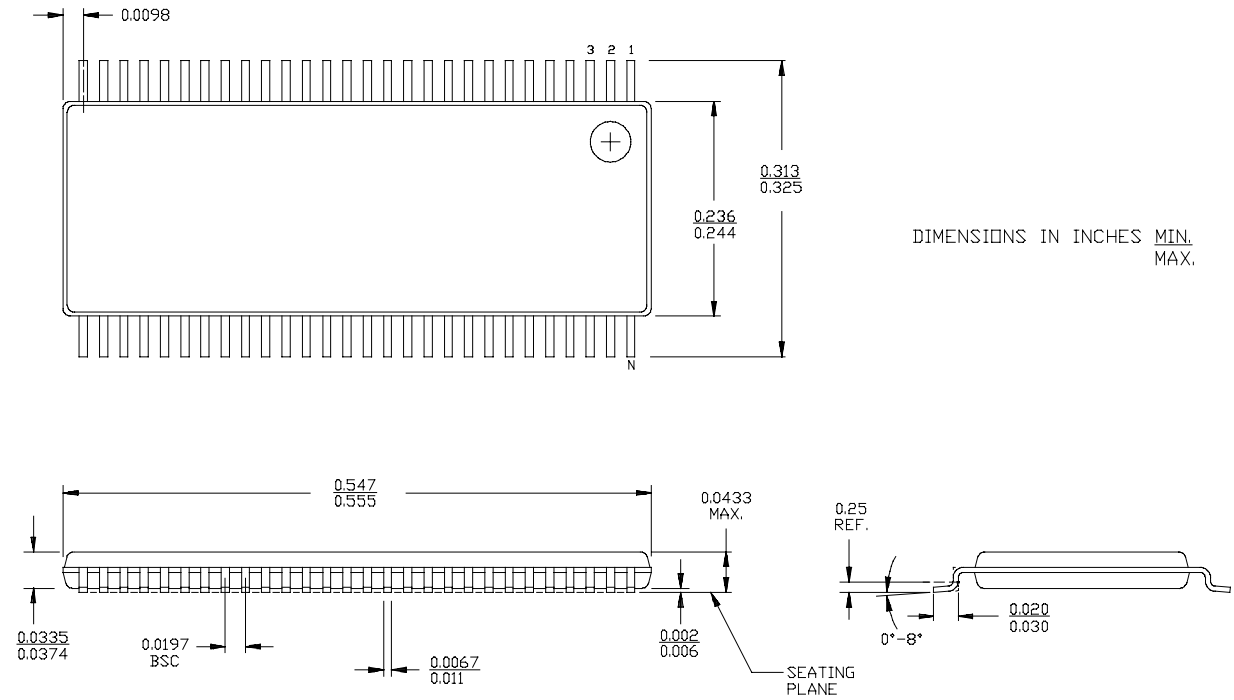
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	74FCT162827CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162827CTPVC	Z56	56-Lead (240-Mil) SSOP	
	74FCT162827CTPVCT	Z56	56-Lead (240-Mil) SSOP	
5.0	CY74FCT162827BTPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162827BTPVCT	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT162827ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162827ATPVCT	O56	56-Lead (300-Mil) SSOP	

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



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