



SCCS056A - August 1994 - Revised October 2001

CY74FCT16500T CY74FCT162500T

18-Bit Registered Transceivers

Features

- FCT-C speed at 4.6 ns
- I_{off} supports partial-power- mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5V \pm 10\%$

CY74FCT16500T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) <1.0V at $V_{CC} = 5V$, $T_A = 25^{\circ}\text{C}$

CY74FCT162500T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) <0.6V at $V_{CC} = 5V$, $T_A = 25^{\circ}\text{C}$

Functional Description

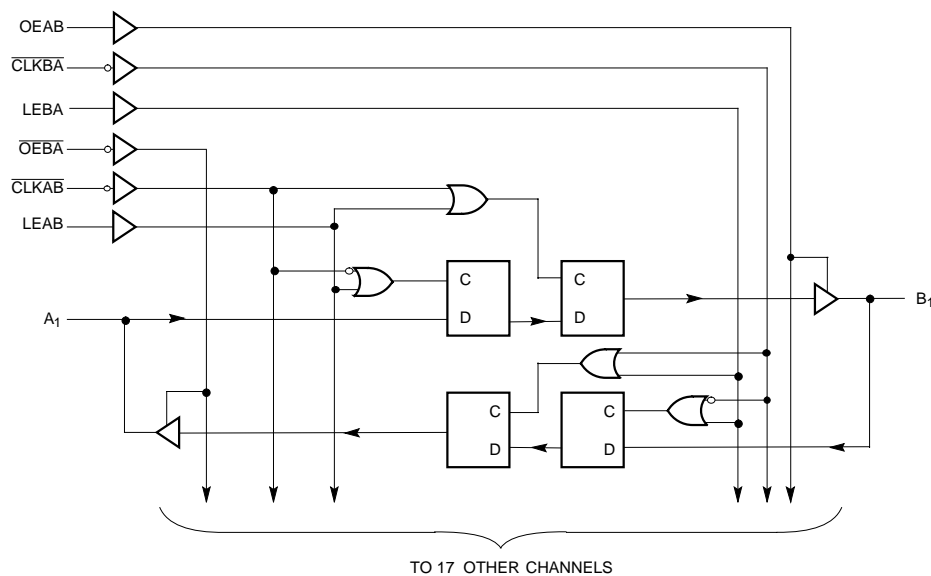
These 18-bit universal bus transceivers can be operated in transparent, latched, or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch enable (\overline{LEAB} and \overline{LEBA}), and clock inputs (\overline{CLKAB} and \overline{CLKBA}) inputs. For A-to-B data flow, the device operates in transparent mode when \overline{LEAB} is HIGH. When \overline{LEAB} is LOW, the A data is latched if \overline{CLKAB} is held at a HIGH or LOW logic level. If \overline{LEAB} is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of \overline{CLKAB} . \overline{OEAB} performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by \overline{OEBA} , \overline{LEBA} , and \overline{CLKBA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

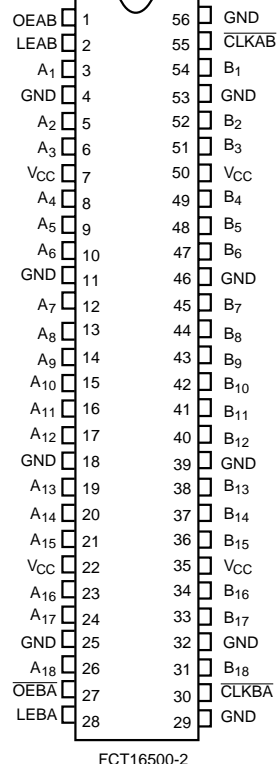
The CY74FCT16500T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162500T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162500T is ideal for driving transmission lines.

Logic Block Diagram



SSOP/TSSOP Top View



Pin Summary

Name	Description
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input (Active LOW)
CLKBA	B-to-A Clock Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

Function Table^[1, 2]

Inputs				Outputs
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↯	L	L
H	L	↯	H	H
H	L	H	X	B ^[3]
H	L	L	X	B ^[4]

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[8]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND.			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μA
I _{OS}	Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[9]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[10]			±1	μA

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. ↯ = HIGH-to-LOW Transition.
- A-to-B data flow is shown, B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Tested at +25°C.

Maximum Ratings^[5, 6]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature Com'l -55°C to +125°C

Ambient Temperature with
Power Applied..... Com'l -55°C to +125°C

DC Input Voltage-0.5V to +7.0V

DC Output Voltage-0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin)-60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	5V ± 10%

Output Drive Characteristics for CY74FCT16500T

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162500T

Parameter	Description	Test Conditions	Min.	Typ. ^[7]	Max.	Unit
I _{ODL}	Output LOW Current ^[9]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[9]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[8] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[7]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max. V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	5	500	μA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max. V _{IN} =3.4V ^[11]	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ^[12]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OEAB=OEBA=V _{CC} or GND V _{IN} =V _{CC} or V _{IN} =GND	75	120	μA/MHz
I _C	Total Power Supply Current ^[13]	V _{CC} =Max., f ₀ =10 MHz (CLKAB), f ₁ =5 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OEAB=OEBA=V _{CC} LEAB=GND V _{IN} =V _{CC} or V _{IN} =GND	0.8	1.7	mA
		V _{IN} =3.4V or V _{IN} =GND	1.3	3.2	mA
		V _{CC} =Max., f ₀ =10 MHz, f ₁ =2.5 MHz, 50% Duty Cycle, Outputs Open, Eighteen Bits Toggling, OEAB=OEBA=V _{CC} LEAB=GND V _{IN} =V _{CC} or V _{IN} =GND	3.8	6.5 ^[14]	mA
		V _{IN} =3.4V or V _{IN} =GND	8.5	20.8 ^[14]	mA

Notes:

11. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f₁
 All currents are in milliamps and all frequencies are in megahertz.
14. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[15]

Parameter	Description	CY74FCT162500AT		CY74FCT16500CT/ CY74FCT162500CT		Unit	Fig. No. ^[16]
		Min.	Max.	Min.	Max.		
f_{MAX}	CLKAB or CLKBA frequency		150		150	MHz	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	1.5	5.1	1.5	4.6	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LEBA to A, LEAB to B	1.5	5.6	1.5	5.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CLKBA to A, CLKAB to B	1.5	5.6	1.5	5.3	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time OEBA to A, OEAB to B	1.5	6.0	1.5	5.4	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time OEBA to A, OEAB to B	1.5	5.6	1.5	5.2	ns	1, 7, 8
t_{SU}	Set-Up Time, HIGH or LOW A to CLKAB, B to CLKBA	3.0		3.0		ns	9
t_H	Hold Time, HIGH or LOW A to CLKAB, B to CLKBA	0		0		ns	9
t_{SU}	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock HIGH	3.0		3.0	ns	4
		Clock LOW	1.5		1.5	ns	4
t_H	Hold Time, HIGH or LOW A to LEAB, B to LEBA	1.5		1.5		ns	4
t_W	LEAB or LEBA Pulse Width HIGH	3.0		2.5		ns	5
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW	3.0		3.0		ns	5
$t_{SK(O)}$	Output Skew ^[17]		0.5		0.5	ns	

Ordering Information CY74FCT16500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT16500CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16500CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162500T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162500CTPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162500CTPVCT	O56	56-Lead (300-Mil) SSOP	
5.1	CT74FCT162500ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162500ATPVCT	O56	56-Lead (300-Mil) SSOP	

Notes:

15. Minimum limits are specified but not tested on Propagation Delays.

16. See "Parameter Measurement Information" in the General Information section.

17. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

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