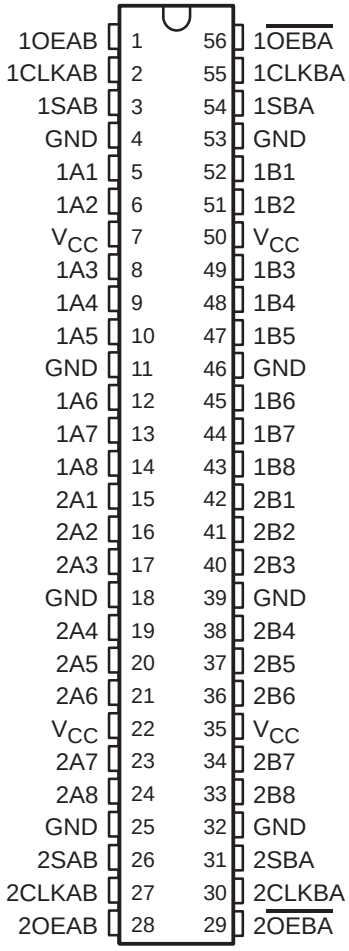
- **Members of the Texas Instruments *Widebus*™ Family**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed $V_{CC}$ and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

**54AC16652 . . . WD PACKAGE**
**74AC16652 . . . DL PACKAGE**
**(TOP VIEW)**




## description

The ’AC16652 are 16-bit bus transceivers that consist of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. They can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ’AC16652.

## description (continued)

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The 74AC16652 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

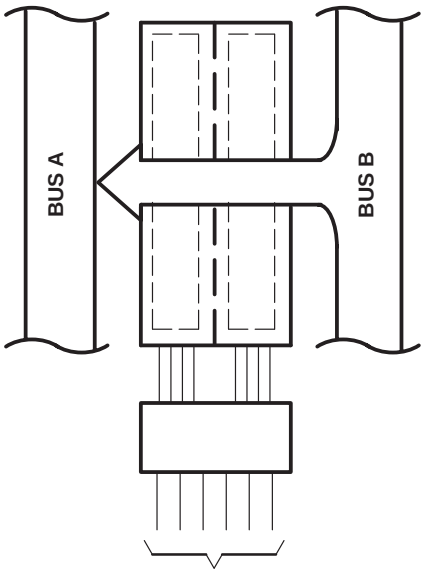
The 54AC16652 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16652 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| L | H | L | L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | L | X | X | Input | Unspecified‡ | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | L | ↑ | X | X | Unspecified‡ | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | L | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | L | X | H | X | Input | Output | Stored A data to B bus |
| H | L | L | L | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

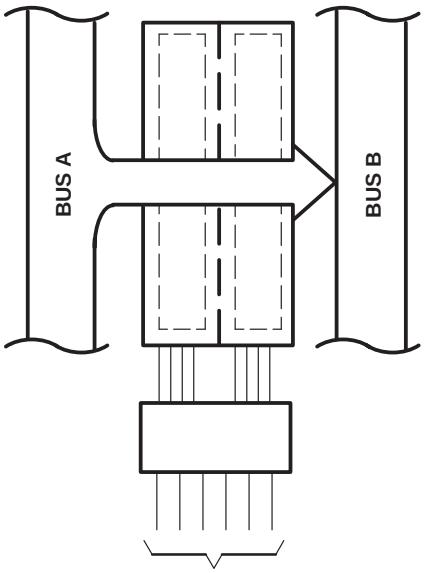
† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered in order to load both registers.



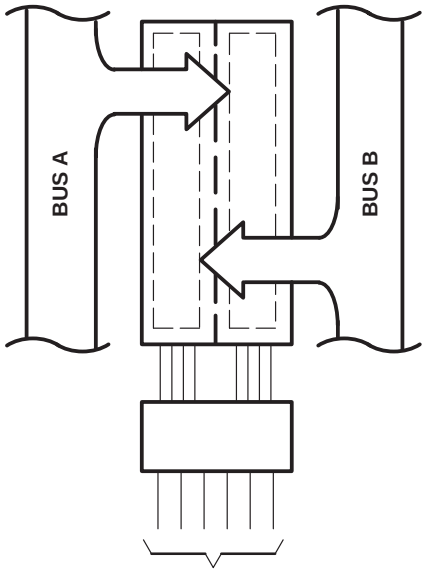

| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



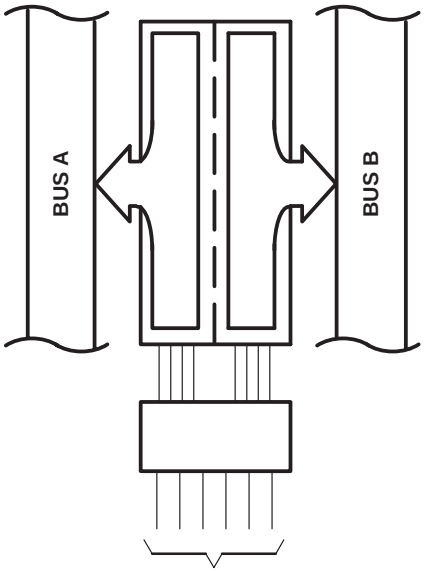

| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

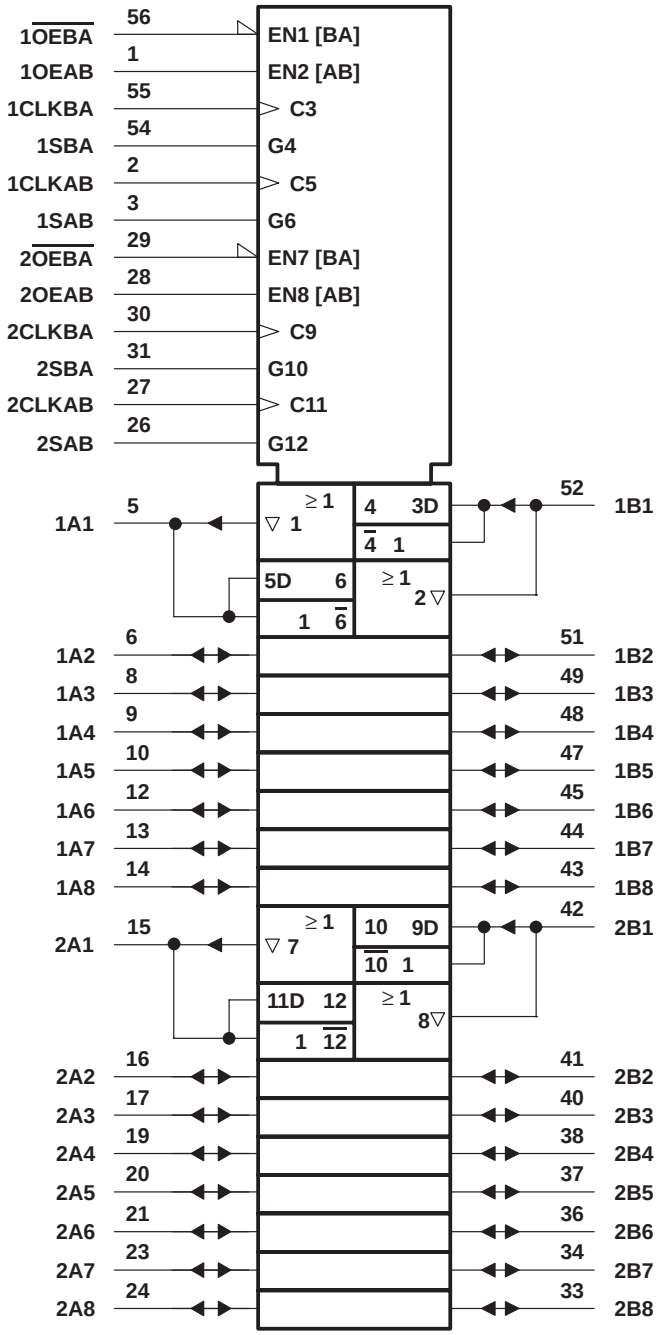



| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| H | L | L | L | H | H |

**TRANSFER STORED DATA**
**TO A AND/OR B**

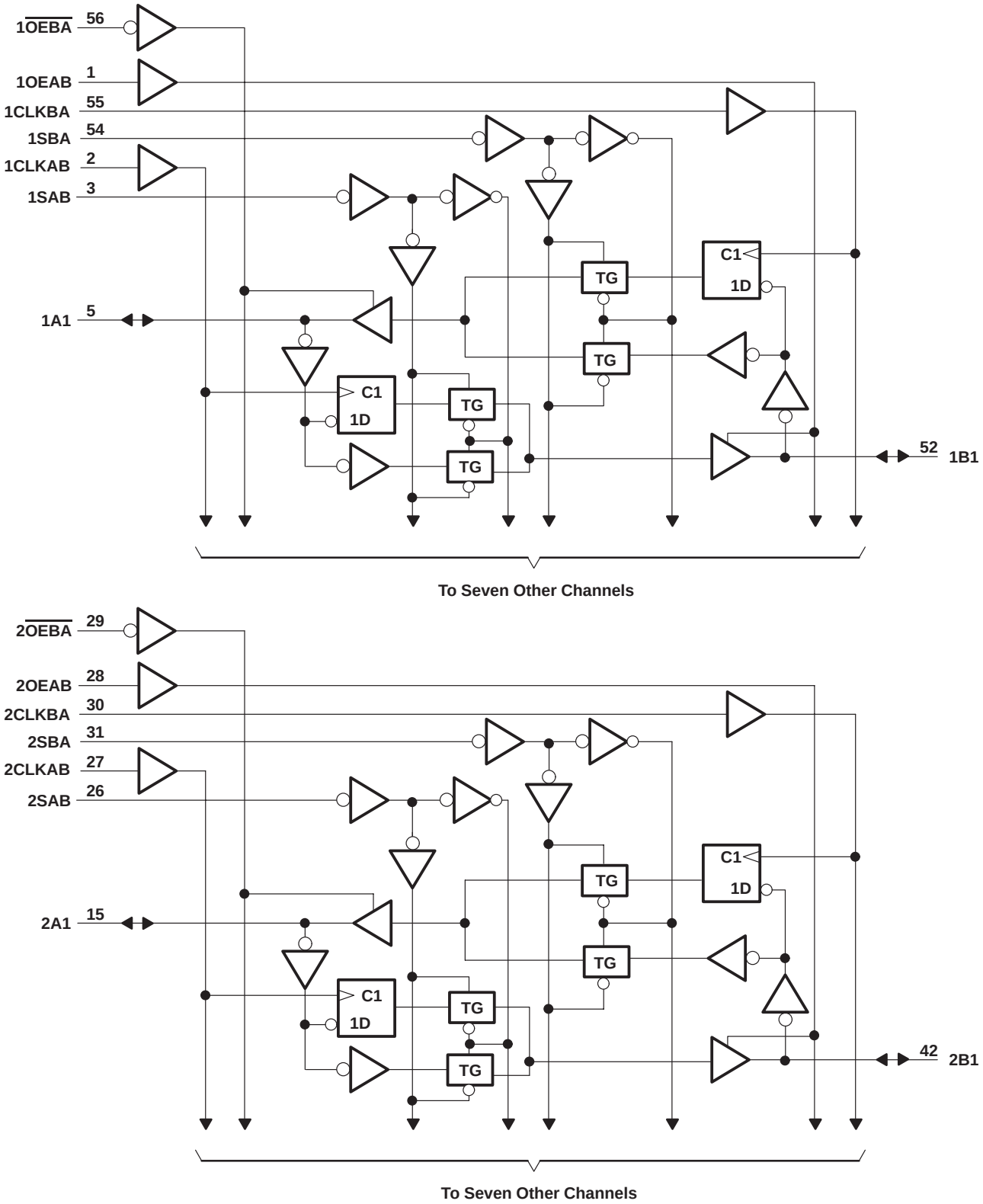
**Figure 1. Bus-Management Functions**

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±400 mA
Maximum package power dissipation at $T_A$ = 55°C (in still air) (see Note 2): DL package . . . . . 1.4 W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

### recommended operating conditions (see Note 3)

| | | | 54AC16652 | | | 74AC16652 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage (see Note 4) | | 3 | 5 | 5.5 | 3 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 2.1 | | | 2.1 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | 3.15 | | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | | 3.85 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | | | 0.9 | | | 0.9 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | | | 1.35 | |
| | | $V_{CC}$ = 5.5 V | | | 1.65 | | | 1.65 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3 V | | | –4 | | | –4 | mA |
| | | $V_{CC}$ = 4.5 V | | | –24 | | | –24 | |
| | | $V_{CC}$ = 5.5 V | | | –24 | | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3 V | | | 12 | | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | | 24 | | | 24 | |
| | | $V_{CC}$ = 5.5 V | | | 24 | | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | | 10 | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |



NOTES: 3. Unused inputs must be held high or low to prevent them from floating.
4. All $V_{CC}$ and GND pins must be connected to the proper voltage power supply.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | 54AC16652 | | 74AC16652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 µA | 3 V | 2.9 | | | 2.9 | | 2.9 | | V |
| | | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.4 | | 2.48 | | |
| | | $I_{OH}$ = –24 mA | 4.5 V | 3.94 | | | 3.7 | | 3.8 | | |
| | | | 5.5 V | 4.94 | | | 4.7 | | 4.8 | | |
| | | $I_{OH}$ = –50 mA† | 5.5 V | | | | 3.85 | | | | |
| | | $I_{OH}$ = –75 mA† | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | | $I_{OL}$ = 50 µA | 3 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | 5.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 12 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | | 1.65 | |
| $I_I$ | Control inputs | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{OZ}$ | A or B ports‡ | $V_O = V_{CC}$ or GND | 5.5 V | | | ±0.5 | | ±10 | | ±5 | µA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 8 | | 160 | | 80 | µA |
| $C_i$ | Control inputs | $V_I = V_{CC}$ or GND | 5 V | | 4 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O = V_{CC}$ or GND | 5 V | | 12 | | | | | | pF |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

| | | $T_A$ = 25°C | | 54AC16652 | | 74AC16652 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | 0 | 55 | 0 | 55 | 0 | 55 | MHz |
| $t_w$ | Pulse duration, CLKAB or CLKBA high or low | 9 | | 9 | | 9 | | ns |
| $t_{su}$ | Setup time, A before CLKAB↑ or B before CLKBA↑ | 7 | | 7 | | 7 | | ns |
| $t_h$ | Hold time, A after CLKAB↑ or B after CLKBA↑ | 0 | | 0 | | 0 | | ns |

## timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

| | | $T_A$ = 25°C | | 54AC16652 | | 74AC16652 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | 0 | 95 | 0 | 95 | 0 | 95 | MHz |
| $t_w$ | Pulse duration, CLKAB or CLKBA high or low | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, A before CLKAB↑ or B before CLKBA↑ | 4.5 | | 4.5 | | 4.5 | | ns |
| $t_h$ | Hold time, A after CLKAB↑ or B after CLKBA↑ | 0 | | 0 | | 0 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | 54AC16652 | | 74AC16652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 55 | | | 55 | | 55 | | MHz |
| $t_{PLH}$ | A or B | B or A | 3.6 | 10.4 | 13.7 | 3.6 | 17.1 | 3.6 | 15.6 | ns |
| $t_{PHL}$ | | | 4.1 | 10.9 | 14.3 | 4.1 | 16.3 | 4.1 | 15.4 | |
| $t_{PLH}$ | CLKBA or CLKAB | A or B | 5.1 | 13.6 | 17.3 | 5.1 | 21.2 | 5.1 | 19.5 | ns |
| $t_{PHL}$ | | | 5.4 | 13.5 | 17.2 | 5.4 | 19.9 | 5.4 | 18.8 | |
| $t_{PLH}$ | SBA or SAB (with A or B high) | A or B | 5.8 | 15.0 | 18.7 | 5.8 | 23.3 | 5.8 | 21.4 | ns |
| $t_{PHL}$ | | | 5.4 | 13.1 | 16.7 | 5.4 | 19.1 | 5.4 | 18.1 | |
| $t_{PLH}$ | SBA or SAB (with A or B low) | A or B | 4.2 | 11.8 | 15.2 | 4.2 | 18.9 | 4.2 | 17.4 | ns |
| $t_{PHL}$ | | | 5.9 | 14.4 | 18.3 | 5.9 | 21.7 | 5.9 | 20.3 | |
| $t_{PZH}$ | $\overline{OEBA}$ | A | 4.2 | 11.8 | 15.1 | 4.2 | 18.8 | 4.2 | 17.2 | ns |
| $t_{PZL}$ | | | 6 | 16.2 | 20.6 | 6 | 25.3 | 6 | 23.5 | |
| $t_{PHZ}$ | $\overline{OEBA}$ | A | 4.6 | 8.1 | 10 | 4.6 | 10.9 | 4.6 | 10.6 | ns |
| $t_{PLZ}$ | | | 4.4 | 7.6 | 9.6 | 4.4 | 10.6 | 4.4 | 10.3 | |
| $t_{PZH}$ | OEAB | B | 4.1 | 11.5 | 14.6 | 4.1 | 18.1 | 4.1 | 16.6 | ns |
| $t_{PZL}$ | | | 6 | 16.0 | 20 | 6 | 24.6 | 6 | 22.7 | |
| $t_{PHZ}$ | OEAB | B | 4.3 | 7.2 | 9 | 4.3 | 9.7 | 4.3 | 9.5 | ns |
| $t_{PLZ}$ | | | 3.9 | 6.7 | 8.6 | 3.9 | 9.2 | 3.9 | 9.1 | |



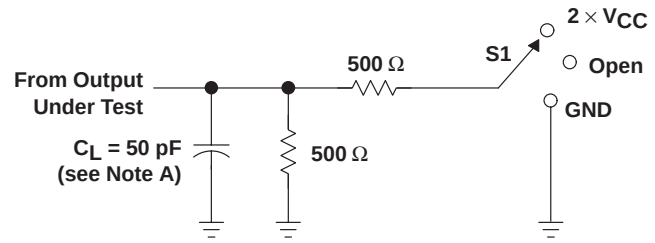
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | 54AC16652 | | 74AC16652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 95 | | | 95 | | 95 | | MHz |
| $t_{PLH}$ | A or B | B or A | 2.7 | 6.1 | 8.8 | 2.7 | 10.7 | 2.7 | 9.9 | ns |
| $t_{PHL}$ | | | 3 | 6.3 | 9.2 | 3 | 10.8 | 3 | 10.2 | |
| $t_{PLH}$ | CLKBA or CLKAB | A or B | 3.9 | 7.8 | 10.9 | 3.9 | 13.3 | 3.9 | 12.2 | ns |
| $t_{PHL}$ | | | 4.2 | 7.8 | 11.1 | 4.2 | 13.2 | 4.2 | 12.3 | |
| $t_{PLH}$ | SBA or SAB (with A or B high) | A or B | 4.5 | 8.8 | 12.1 | 4.5 | 15 | 4.5 | 13.8 | ns |
| $t_{PHL}$ | | | 4.1 | 7.7 | 11 | 4.1 | 12.9 | 4.1 | 12.1 | |
| $t_{PLH}$ | SBA or SAB (with A or B low) | A or B | 3.1 | 6.7 | 9.7 | 3.1 | 11.9 | 3.1 | 11 | ns |
| $t_{PHL}$ | | | 4.6 | 8.8 | 12.2 | 4.6 | 14.9 | 4.6 | 13.8 | |
| $t_{PZH}$ | $\overline{OEBA}$ | A | 3.1 | 6.7 | 9.5 | 3.1 | 11.6 | 3.1 | 10.7 | ns |
| $t_{PZL}$ | | | 4.5 | 8.3 | 11.8 | 4.5 | 14.4 | 4.5 | 13.2 | |
| $t_{PHZ}$ | $\overline{OEBA}$ | A | 4.6 | 6.5 | 8.3 | 4.6 | 9 | 4.6 | 8.8 | ns |
| $t_{PLZ}$ | | | 4.1 | 6.1 | 8.1 | 4.1 | 9.1 | 4.1 | 8.7 | |
| $t_{PZH}$ | OEAB | B | 3.1 | 6.6 | 9.3 | 3.1 | 11.3 | 3.1 | 10.5 | ns |
| $t_{PZL}$ | | | 4.6 | 8.2 | 11.6 | 4.6 | 14.1 | 4.6 | 13 | |
| $t_{PHZ}$ | OEAB | B | 4.2 | 5.9 | 7.7 | 4.2 | 8.3 | 4.2 | 8 | ns |
| $t_{PLZ}$ | | | 3.7 | 5.5 | 7.4 | 3.7 | 8.3 | 3.7 | 7.8 | |

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

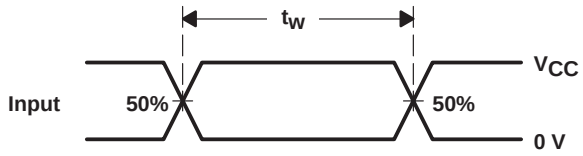
| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per transceiver | Outputs enabled | $C_L$ = 50 pF, | f = 1 MHz | 57 | pF |
| | | Outputs disabled | | | 13 | |

## PARAMETER MEASUREMENT INFORMATION

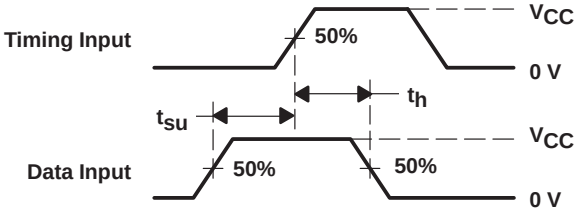



LOAD CIRCUIT

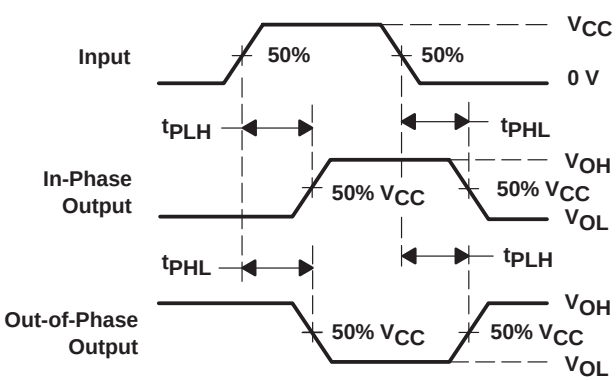
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



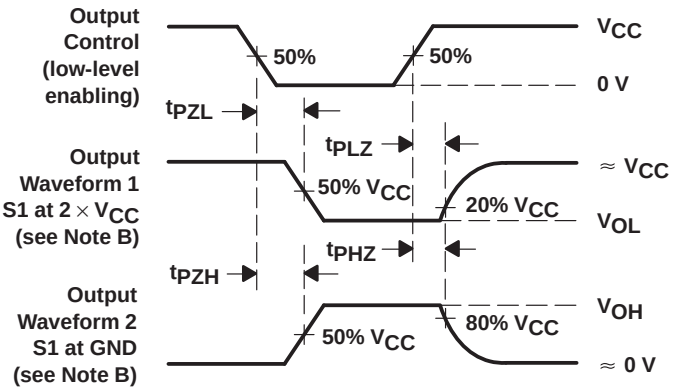

VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS




VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

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