54AC16373, 74AC16373
16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

- **Members of the Texas Instruments** *Widebus*™ **Family**
- **3-State True Outputs**
- **Full Parallel Access for Loading**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V$_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise**
- *EPIC*™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54AC16373 . . . WD PACKAGE
74AC16373 . . . DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V$_{CC}$	7	42	V$_{CC}$
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V$_{CC}$	18	31	V$_{CC}$
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2$\overline{OE}$	24	25	2LE
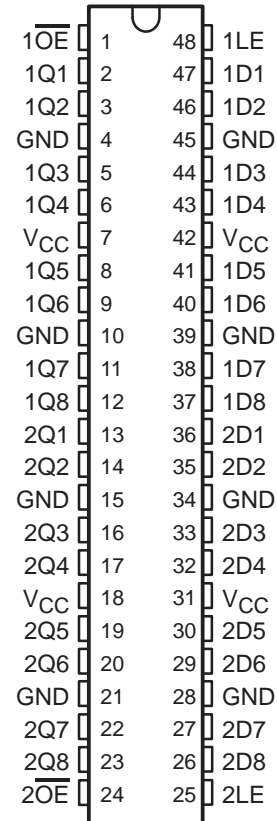
description

The 'AC16373 are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC16373 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16373 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16373 is characterized for operation from –40°C to 85°C.

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FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol[†]
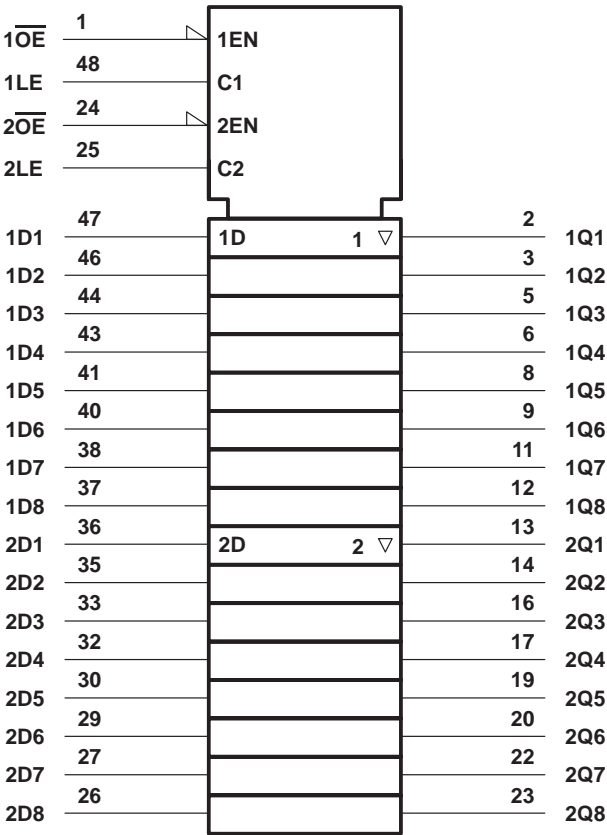
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)

To Seven Other Channels

To Seven Other Channels
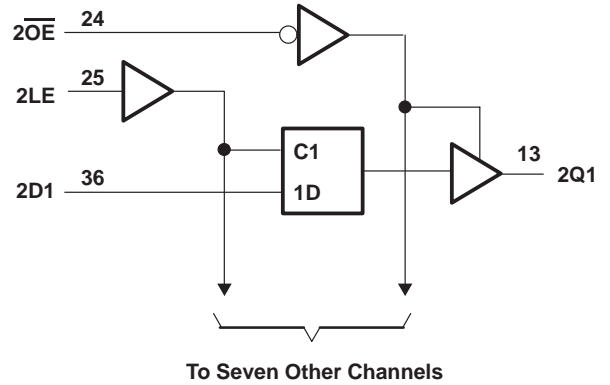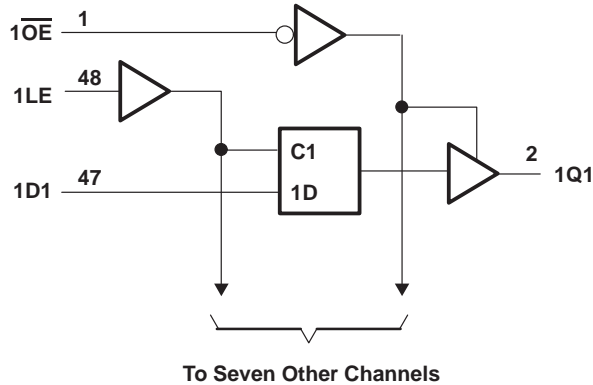
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DL package .... 1.2 W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			54AC16373			74AC16373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t / \Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC16373		74AC16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		
	I_{OL} = −24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		3.85		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65		1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5		±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80		80	µA
C_i	V_I = V_{CC} or GND	5 V		4.5						pF
C_O	V_O = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

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timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54AC16373		74AC16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5		5		5		ns
t_{su}	Setup time, data before LE↓	1.5		1.5		1.5		ns
t_h	Hold time, data after LE↓	3		3		3		ns

timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		54AC16373		74AC16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		4		4		ns
t_{su}	Setup time, data before LE↓	1.5		1.5		1.5		ns
t_h	Hold time, data after LE↓	2.5		2.5		2.5		ns

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16373		74AC16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.7	10.6	13.4	3.7	15.1	3.7	15.1	ns
t_{PHL}			4.3	11.3	14	4.3	14.8	4.3	14.8	
t_{PLH}	LE	Q	4.6	12.9	15.8	4.6	18.6	4.6	18.6	ns
t_{PHL}			4.5	12.1	14.6	4.5	16.4	4.5	16.4	
t_{PZH}	$\overline{OE}$	Q	4.2	11.8	14.8	4.2	17.5	4.2	17.5	ns
t_{PZL}			5.4	16.3	19.8	5.4	22.3	5.4	22.3	
t_{PHZ}	$\overline{OE}$	Q	4.2	7.9	9.5	4.2	10.2	4.2	10.2	ns
t_{PLZ}			3.8	7.1	8.9	3.8	9.8	3.8	9.8	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16373		74AC16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.1	6.7	8.5	3.1	9.7	3.1	9.7	ns
t_{PHL}			3.5	7.3	9.1	3.5	10.1	3.5	10.1	
t_{PLH}	LE	Q	3.8	8.2	10.2	3.8	11.9	3.8	11.9	ns
t_{PHL}			3.6	7.8	9.7	3.6	10.9	3.6	10.9	
t_{PZH}	$\overline{OE}$	Q	3.5	7.4	9.4	3.5	10.8	3.5	10.8	ns
t_{PZL}			4.3	9.1	11.3	4.3	12.8	4.3	12.8	
t_{PHZ}	$\overline{OE}$	Q	3.9	6.6	8	3.9	8.8	3.9	8.8	ns
t_{PLZ}			3.7	5.9	7.4	3.7	8.1	3.7	8.1	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF,	f = 1 MHz	43	pF
	Outputs disabled			5	

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PARAMETER MEASUREMENT INFORMATION
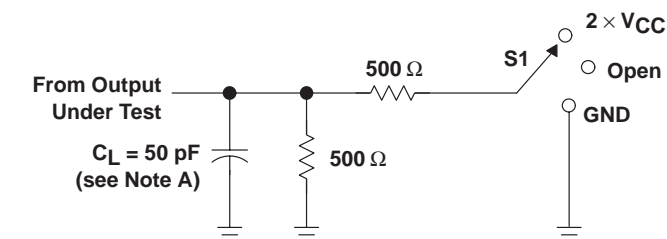
LOAD CIRCUIT

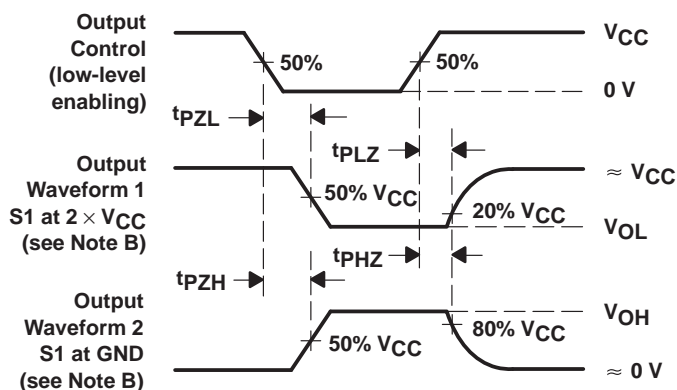| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND
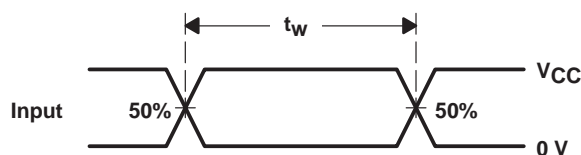
VOLTAGE WAVEFORMS
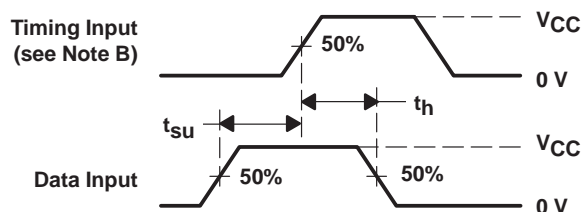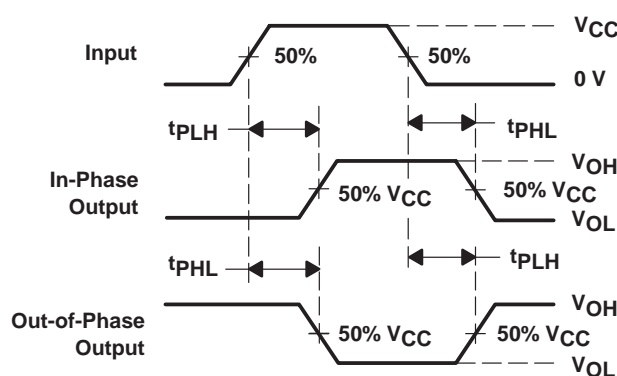
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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