7901 to 7902 Migration Application Note

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1 Purpose Statement

The purpose of this document is to provide engineers who have previously designed using the 7901 with the information necessary to transition easily to the 7902 device in hardware designs.

It is important to note that the internal functionality of the 7902 has not changed and allows software development to take place in advance using the 7901. This document has been created to serve as a guide to help understand the differences between the 7901 and the 7902 Network Security Processors. For more information or to request a copy of the schematic diagrams please contact your local Hifn Representative or email request at applications@hifn.com.

2 Overview

The 7901 is the industry's first Broadband Network Security Processor that implements symmetric key encryption, public key encryption, authentication, and data compression in hardware. In addition, it also includes math processor and true hardware random number generator which is used to support public key cryptography.

The 7902 Broadband Network Security Processor is a plug-in device that is functionally compatible to the 7901. The 7902, based on a smaller manufacturing process technology, offers a more cost effective solution with lower power consumption and higher performance.

2.1 7902 Advantages Over 7901

The 7902 device has the following enhancements over the 7901:

- Higher maximum (operating) frequency resulting in increased performance
- Reduced power requirements resulting in lower power consumption
- Increased addressable external memory resulting in more supportable sessions

2.2 Implementation Changes

There are minor hardware changes needed in a design in order to transition from the 7901 to 7902. The changes are mainly related to the V_{DD} power supply. In order to provide a better understanding of the two devices and the compatibility between them, the following items are covered in more detail:

- Power supply voltage
- Power dissipation
- Maximum operating frequency
- PLL operating frequency
- Timing specification
- Amount of external memory supported
- Pin List
- Chip ID

2.3 Reference Documentation

Detailed information on the 7902 is in the *7902 Network Security Processor Preliminary Datasheet*, PDS-0040. Detailed information on the 7901 is in the *7901 Network Security Processor Datasheet*, DS-0023.

3 7901 and 7902 Differences

3.1 Power Supplies

While the 7901 requires a 3.3 volt power supply for internal operation and the I/O interface, the 7902 requires a 2.5 volt power supply for internal operation and a 3.3 volt power supply for external memory and I/O interfaces.
To accommodate the 2.5 volt supply requirement for the core logic, four of the pins were changed from V_{DD} (3.3 volts) to V_{DD2} (2.5 volts) supply pins. To accommodate the 2.5 volt supply requirement for the PLL, the analog supply pin, AV_{DD}, was changed to AV_{DD2} (2.5 volts). Refer to Figure 11 for a list of the pin name differences between the 7901 to the 7902.

3.2 Power Sequencing

If the +2.5V and +3.3V power supply voltages are not asserted at the same time, the possibility of reverse currents arises. To prevent damage to the device, these voltages must be enabled within the time given in the absolute maximum ratings. The power supply should be designed to assert power within the time limits given under the recommended operating conditions.

3.3 Power Dissipation

The majority of the power consumed by the 7901 and 7902 is in the I/O interface logic. However, running the core logic on 2.5 volts instead of 3.3 volts results in approximately 5-10% reduction in the total power dissipation. See Figure 1 for a comparison of the power dissipation between the 7901 and 7902 devices.

Power Dissipation Clock Speed	Conditions	Typ	Max	Units
7901 - 50 MHz	V_{DD} = 3.6V	0.6	1.0	W
7902 - 50 MHz	V_{DD} = 3.6V	0.41	0.6	W
	V_{DD2} = 2.8V	0.14	0.23	
	Total	0.5	0.6	
7902 - 66 MHz	V_{DD} = 3.6V	0.54	0.80	W
	V_{DD2} = 2.8V	0.18	0.30	
	Total	0.65	0.80	

Figure 1. 7901 and 7902 Power Dissipation Comparison

3.4 Maximum Operating Frequency

Using a smaller manufacturing process technology enables the 7902 to operate at a higher clock frequency than the 7901—66MHz versus 50MHz.

3.5 PLL Operating Frequency Range

The 7901's PLL supports 25-50MHz operation. The PLL used to support 66MHz operation in the 7902 has a minimum operating frequency of 40MHz. To maintain compatibility with the 7901 at frequencies less than 40MHz requires the PLL to be disabled. The 7901's PLL enable signal pin name is V_{SS}. In the 7902 the PLL enable signal pin name is PLLE# (see Section 3.8 for the PLL's pin number). Note: PLLE#=VSS (PLL Enabled), PLLE#=VDD (PLL Disabled)
Figure 2 summarizes the operating frequency ranges for the 7901 and 7902 based on the state of the PLL.

Operating Frequency	PLLE#	
	7901	7902
Under 25MHz	VDD	VDD
25MHz to 40MHz	VSS	VDD
40MHz to maximum	VSS	VSS

Note: PLLE#=VSS (PLL Enabled), PLLE#=VDD (PLL Disabled)

Figure 2. 7901 and 7902 PLL Operating Frequency Range

3.6 AC Timing Differences

Some of the timing parameters for the CPU interface have changed between the 7901 and 7902. Refer to Figure 5 for the timing differences for 50MHz operation between the 7901 and 7902. All other timing parameters not listed remain the same.

Number	Description	PLL Condition	Min	Max	Units
1	Clock frequency (t_{CLK} = 1 / clock frequency)	enabled	40	66	MHz
		disabled		40	
2	Clock width high	enabled	6		ns
		disabled	9.5		
3	Clock width low	enabled	6		ns
		disabled	9.5		
4	Clock rise time from V_{IL} to V_{IH}	enabled 40-50 MHz		3	ns
		enabled 50-66 MHz		1.5	
		disabled		3	
5	Clock fall time from V_{IH} to V_{IL}	enabled 40-50 MHz		3	ns
		enabled 50-66 MHz		1.5	
		disabled		3	
–	PLL lock time	enabled		100	µs
		disabled		N / A	
–	Clock frequency jitter	enabled		3	%
		disabled		3	

Note: Clock widths are measured to / from 1.4V. PLLE#=low (PLL Enabled), PLLE#=high (PLL Disabled)

Figure 3. 7902 External Clock Timing

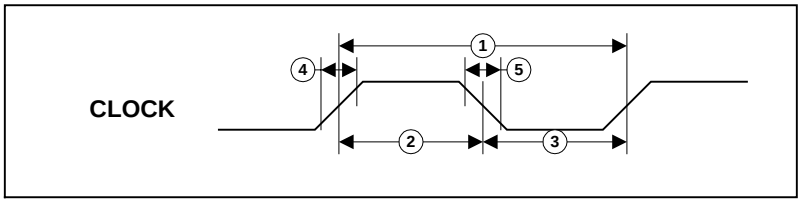

Figure 4. 7902 External Clock Timing Diagram

Number	Description	PLL Condition	7901		7902		Units
			Min	Max	Min	Max	
1	A/MA, TS#, CS#, TSIZ, R/W# setup		3		3		ns
2	A/MA, TS#, CS#, TSIZ, R/W# hold		1		1		ns
3	Write data setup		3		3		ns
4	Write data hold		1		1		ns
5	TA# high-z to low (assertion delay)	enabled	2	8	1.5[1]	8[1]	ns
		disabled	-	-	3[1]	14[1]	
6	TA# low to high (deassertion delay)	enabled	2	8	1.5[1]	8[1]	ns
		disabled	-	-	3[1]	14[1]	
7	TA# high to high-z	enabled	2	8	1.5[1]	8[1]	ns
		disabled	-	-	3[1]	14[1]	
8	Read data output valid delay (high-z to 0/1)	enabled	2	12	1.5[1]	9[1]	ns
		disabled	-	-	3[1]	16.5[1]	ns
9	Read data output invalid delay (0/1 to high-z)	enabled	2	12	1.5[1]	9[1]	ns
		disabled	-	-	3[1]	16.5[1]	ns

Note 1: Timing parameters that changed for 7902 operation.

Figure 5. 7901 and 7902 Read/Write CPU Timing (Single Beat)

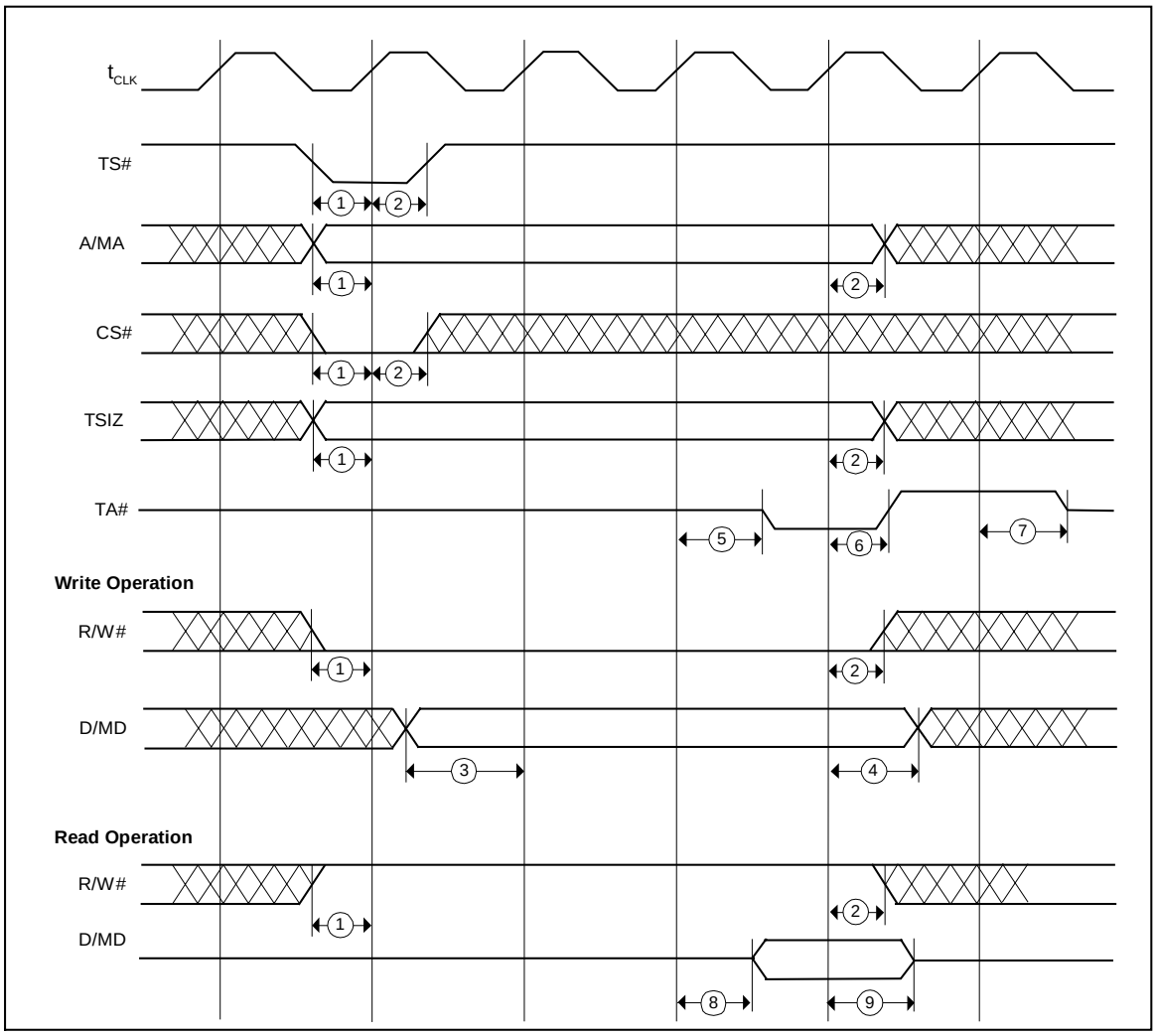

Figure 6. 7901 and 7902 Read/Write CPU Timing Diagram (Single Beat)

The operating conditions for the AC timing listed previously in Figure 5 are shown below in Figure 7.

Symbol	Parameter	Conditions
C_{L2}	Output load on CPU interface pins	50 pF
V_{DD}	Supply voltage	3.3V ± 5%
V_{DD2}	Supply voltage (only applies to the 7902)	2.5V ± 5%
V_{SS}	Ground potential	0V
T_A	Ambient operating temperature	0°C to +70°C
t_{CLK}	Clock frequency	PLL enabled: 40-66MHz PLL disabled: < 40MHz

Figure 7. Operating Conditions for the Timing Specifications

3.7 External Memory

The increase of external memory is supported and involves the change of two pins (80 and 97) from NC on the 7901 to external memory address lines CA[16] and CA[17] on the 7902. Refer to Figure 8 for the maximum amount of external memory supported.

	7901	7902
Max. SRAM Size	64Kx16	256Kx16

Figure 8. 7901 and 7902 Maximum External Memory Supported

External memory is not required if an application does not need compression. If compression is used, the amount of external memory required shall depend on the type and number of sessions that must be supported. Refer to the External RAM Usage section in the 7901 or 7902 Data Sheet for more information on the usage of external memory. Figure 9 and Figure 10 lists the number of sessions supported when the maximum amount of external memory (Figure 8) is used.

7901		7902	
LZS—Full Duplex (Sessions)	**MPPC—Full Duplex (Sessions)**	**LZS—Full Duplex (Sessions)**	**MPPC—Full Duplex (Sessions)**
8	4	32	16

Figure 9. 7901 and 7902 Stateful Sessions (Multiple History) Supported with Maximum Amount of External Memory

128 Byte (DES, 3-DES)		512 Byte (DES, 3-DES, RC4)	
7901 (Sessions)	**7902 (Sessions)**	**7901 (Sessions)**	**7902 (Sessions)**
768	3840	192	960

Figure 10. 7901 and 7902 Stateless Sessions (Single History) Supported with Maximum Amount of External Memory

3.8 Pin List

Five of the 7901's power supply pins (V_{DD} and AV_{DD}) have been changed to accommodate the 7902's core logic requirement for 2.5 volts. Two of the 7901's NC pins have also been changed to external memory address lines. The PLL enable is now labeled as PLLE#. Refer to Figure 11 for a list of the pin differences between the 7901 and the 7902.

Pin Number	7901 Pin Name	7902 Pin Name
18	VDD	VDD2
30	VSS	PLLE#
48	VDD	VDD2
49	VDD	VDD2
50	AVDD	AVDD2
80	NC	CA[16]
97	NC	CA[17]
125	VDD	VDD2

Figure 11. 7901 and 7902 Pin Name Differences

3.9 Chip ID

The Chip ID is used by software to determine the device and the revision level. A new unique chip ID was assigned to the 7902. Figure 12 shows the chip IDs for the 7901 and 7902.

Device	Chip ID
7901	0x00000800
7902	0x00040000

Figure 12. 7901 and 7902 Chip Identification Numbers

4 Supporting 7901 and 7902 on the Same PC Board

In designing a PC board that can support both the 7901 and 7902 consideration is needed only in connecting the power supply pins. Since the 7902 requires two power supply voltages (3.3V and 2.5V) and has three sets of power supply pins (V_{DD}, V_{DD2}, AV_{DD2}), it is necessary to separate those sets of pins in order to support both devices on the same board.

Separating the pins and inserting a jumper (J1), as shown in Figure 13, provides an easy way to select the appropriate voltage for the V_{DD}/V_{DD2} and AV_{DD}/AV_{DD2} pins. When the 7902 is used, J1 connects the V_{DD2} and AV_{DD2} pins to the 2.5V power supply. When the 7901 is used, J1 is used to connect the V_{DD} and AV_{DD} pins to the 3.3V power supply. The 7902, as does the 7901, requires some isolation of the appropriate power supply voltage (V_{DD} or V_{DD2}) to provide a clean analog supply voltage (AV_{DD} or AV_{DD2}) to the PLL circuit.

For clock frequencies in the 25MHz to 40MHz range, the PLL must be enabled on the 7901 and disabled on the 7902. Adding a jumper J2, as shown in Figure 13, provides an easy way to enable or disable the PLL so that both parts can be supported on the same PC board. When the 7901 is used, J2 connects the PLLE# signal to VSS enabling the PLL. When the 7902 is used, J2 connects the PLLE# signal to VDD to disable the PLL.

For clock frequencies outside of the 25MHz to 40MHz range a jumper (J2) is not required. If less than 25MHz is used, the PLL must be disabled (tied to VDD) and if greater than 40MHz is used, the PLL must be enabled (tied to VSS).

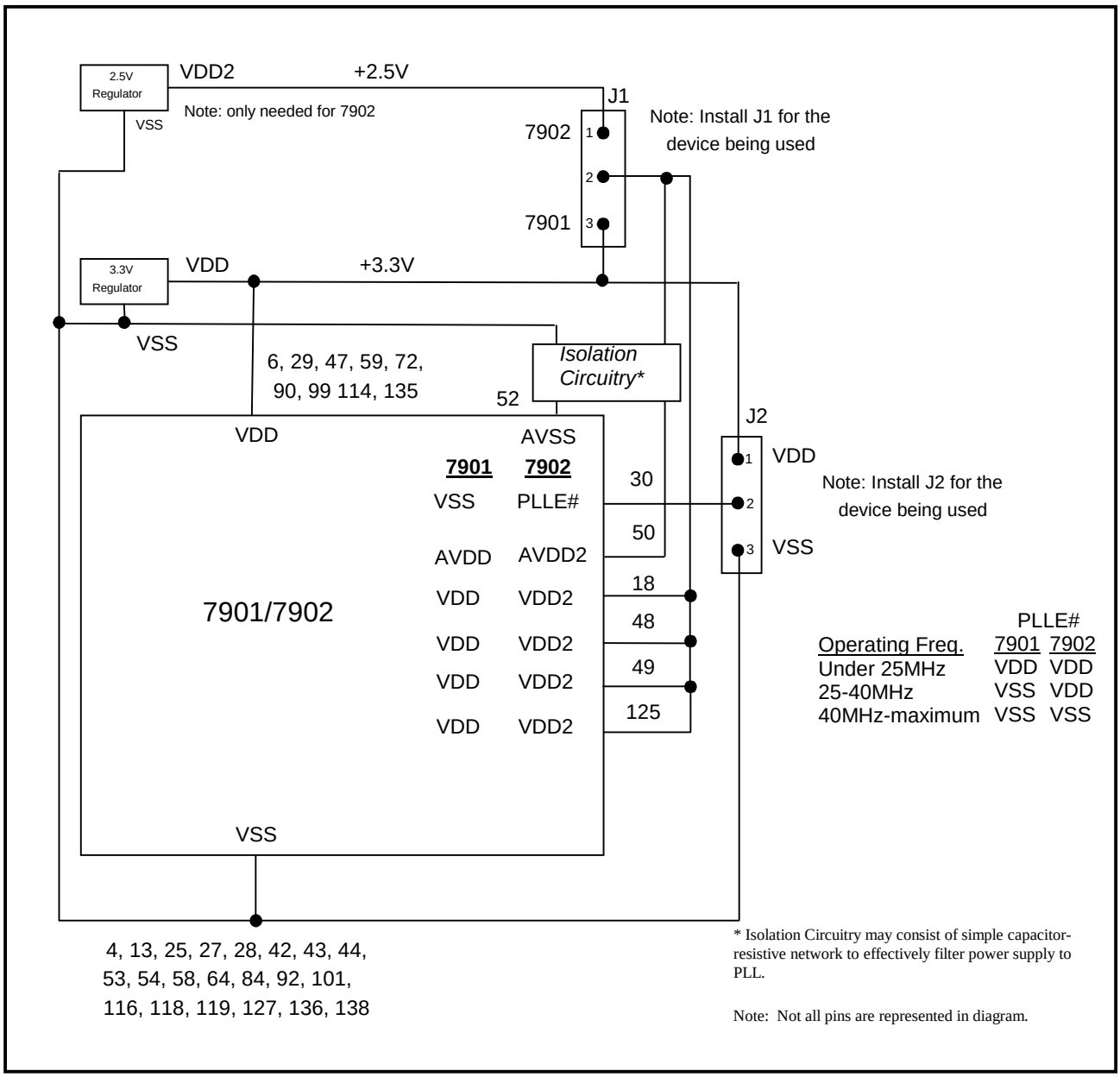

Figure 13. Recommend Connections for Supporting the 7901 and 7902 on the same PC Board