

74F543

Octal Registered Transceiver

General Description

The 'F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA (20 mA Mil) while the B outputs are rated for 64 mA (48 mA Mil).

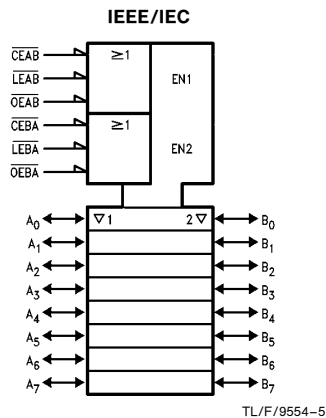
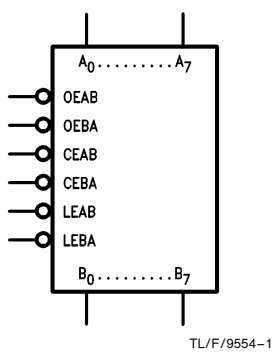
Features

- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 24 mA (20 mA Mil)
- B outputs sink 64 mA (48 mA Mil)
- 300 mil slim package

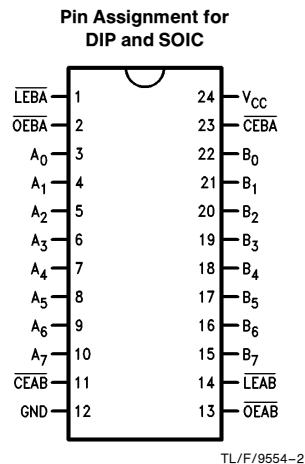
Commercial	Package Number	Package Description
74F543SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74F543SC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F543SJ (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, EIAJ
74F543MSA (Note 1)	MSA24	24-Lead Molded Shrink Small Outline, EIAJ, Type II

Note 1: Devices also available in 13" reel. Use suffix = SCX, SJX and MSAX

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)	1.0/1.0	20 μA / – 0.6 mA
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)	1.0/1.0	20 μA / – 0.6 mA
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)	1.0/2.0	20 μA / – 1.2 mA
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)	1.0/2.0	20 μA / – 1.2 mA
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)	1.0/1.0	20 μA / – 0.6 mA
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)	1.0/1.0	20 μA / – 0.6 mA
A_0 – A_7	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs	3.5/1.083 150/40 (33.8)	70 μA / – 650 μA – 3 mA/24 mA (20 mA)
B_0 – B_7	B-to-A Data Inputs or A-to-B TRI-STATE Outputs	3.5/1.083 600/106.6 (80)	70 μA / – 650 μA – 12 mA/64 mA (48 mA)

Functional Description

The 'F543 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0 – A_7 or take data from B_0 – B_7 , as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

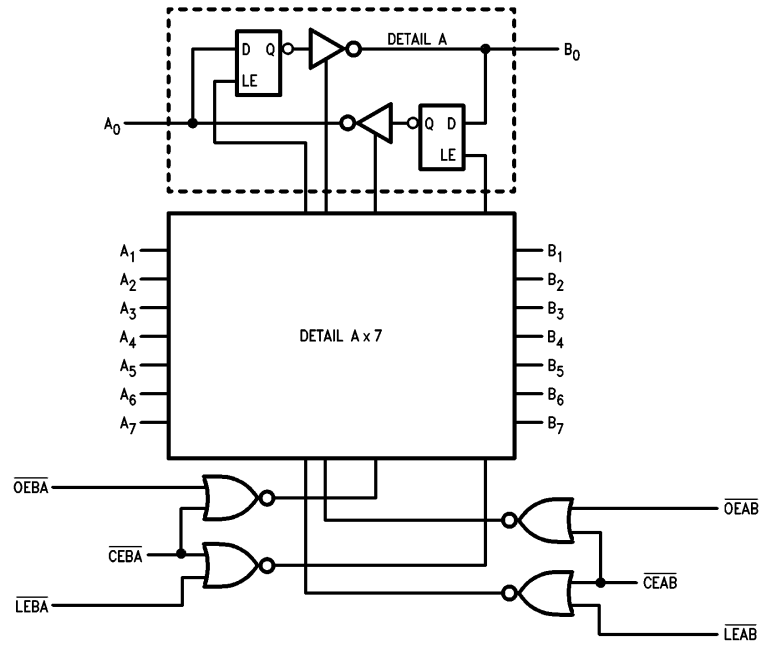
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



TL/F/9554-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

Symbol	Parameter		74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC}	2.5			V	Min	I _{OH} = −1 mA (A _n)
		74F 10% V _{CC}	2.4					I _{OH} = −3 mA (A _n , B _n)
		74F 5% V _{CC}	2.7					I _{OH} = −1 mA (A _n)
		74F 5% V _{CC}	2.7					I _{OH} = −3 mA (A _n , B _n)
		74F 10% V _{CC}	2.0					I _{OH} = −15 mA (B _n)
V _{OL}	Output LOW Voltage	74F 10% V _{CC}		0.5		V	Min	I _{OL} = 24 mA (A _n)
		74F 10% V _{CC}		0.55				I _{OL} = 64 mA (B _n)
I _{IH}	Input HIGH Current	74F		5.0		μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0		μA	Max	($\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)
I _{BVIT}	Input HIGH Current Breakdown (I/O)	74F		0.5		mA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current	74F		50		μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75		μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded

DC Electrical Characteristics (Continued)

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{IL}	Input LOW Current			−0.6 −1.2	mA	Max	V _{IN} = 0.5V ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) V _{IN} = 0.5V ($\overline{\text{CEAB}}$, $\overline{\text{CEBA}}$)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current			−650	μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	−60 −100		−150 −225	mA	Max	V _{OUT} = 0V (A _n) V _{OUT} = 0V (B _n)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (A _n , B _n)
I _{CCH}	Power Supply Current		67	100	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		83	125	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		83	125	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

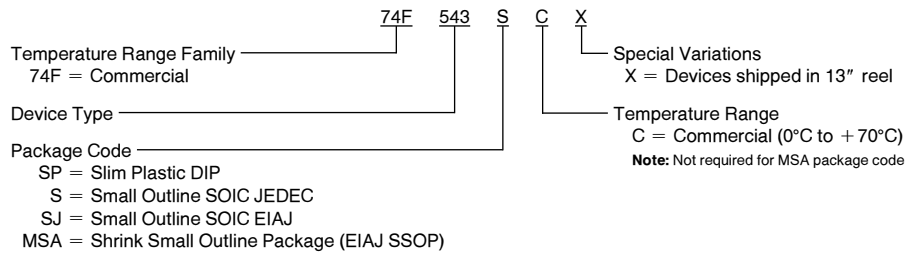
Symbol	Parameter	74F			74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A _n to B _n or B _n to A _n	3.0 3.0	5.5 5.0	7.5 6.5	3.0 3.0	8.5 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to A _n	4.5 4.5	8.5 8.5	11.0 11.0	4.5 4.5	12.5 12.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEAB to B _n	4.5 4.5	8.5 8.5	11.0 11.0	4.5 4.5	12.5 12.5	ns
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A _n or B _n CEBA or CEAB to A _n or B _n	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	10.0 12.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time OEBA or OEAB to A _n or B _n CEBA or CEAB to A _n or B _n	1.0 2.5	6.0 5.5	8.0 10.5	1.0 2.5	9.0 11.5	

AC Operating Requirements

Symbol	Parameter	74F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Com		
		Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW	3.0		3.5		ns
t _s (L)	A _n or B _n to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.0		3.5		
t _h (H)	Hold Time, HIGH or LOW	3.0		3.5		
t _h (L)	A _n or B _n to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	3.0		3.5		
t _w (L)	Latch Enable, B to A or B to A Pulse Width, LOW	8.0		9.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



The drawing illustrates the mechanical specifications of a 24-pin DIP package. The top view shows a rectangular body with 24 pins (12 on each side) and a circular lead identification feature. Dimensions include a body width of 0.6141 inches (15.60 mm) and a pin pitch of 0.0985 inches (2.50 mm). The side view shows a package height of 0.4190 inches (10.65 mm) and a seating plane offset of 0.014 inches (0.35 mm). The detail view shows a pin diameter of 0.0200 inches (0.508 mm) and a lead thickness of 0.004 inches (0.1 mm).

Top View Dimensions:

- Overall Width: 0.6141 (15.60)
- Pin Pitch: 0.0985 (2.50)
- Pin 1 Identification: 0.2992 (7.6)
- Pin 12 to Pin 13 Distance: 0.0200 (0.508)

Side View Dimensions:

- Overall Height: 0.4190 (10.65)
- Seating Plane Offset: 0.014 (0.35)

Detail View Dimensions:

- Pin Diameter: 0.0200 (0.508)
- Lead Thickness: 0.004 (0.1)
- Lead Angle: 45° x 0.029 (0.75)
- Lead Spacing: 0.0125 (0.32)
- Lead Width: 0.0091 (0.23)
- Lead Tip Radius: 0.0500 (1.27)
- Lead Tip Angle: 8° MAX TYP

Symbolic Callouts:

- [-B-]: Pin 1 Identification
- [-C-]: Pin 12 to Pin 13 Distance
- [-A-]: Seating Plane
- ⌀: Pin Diameter
- (M): Material
- (A): Finish
- (S): Surface
- (B): Body

Technical drawing of a 12-pin connector. The drawing shows two views: a top view and a side view.

Top View Dimensions:

- Overall length: $1.243 - 1.270$ (31.57 - 32.26) MAX
- Pin pitch: 0.092 (2.337) (2 PLS)
- Pin 1 IDENT: PIN NO. 1 IDENT
- Option 2: OPTION 2 (0.032 (0.813) RAD)
- Option 2: OPTION 2 (0.062 (1.575) RAD)
- EJECTOR PINS OPTIONAL: EJECTOR PINS OPTIONAL
- Pin 12: 0.260 ± 0.005 (6.604 $\pm$ 0.127)

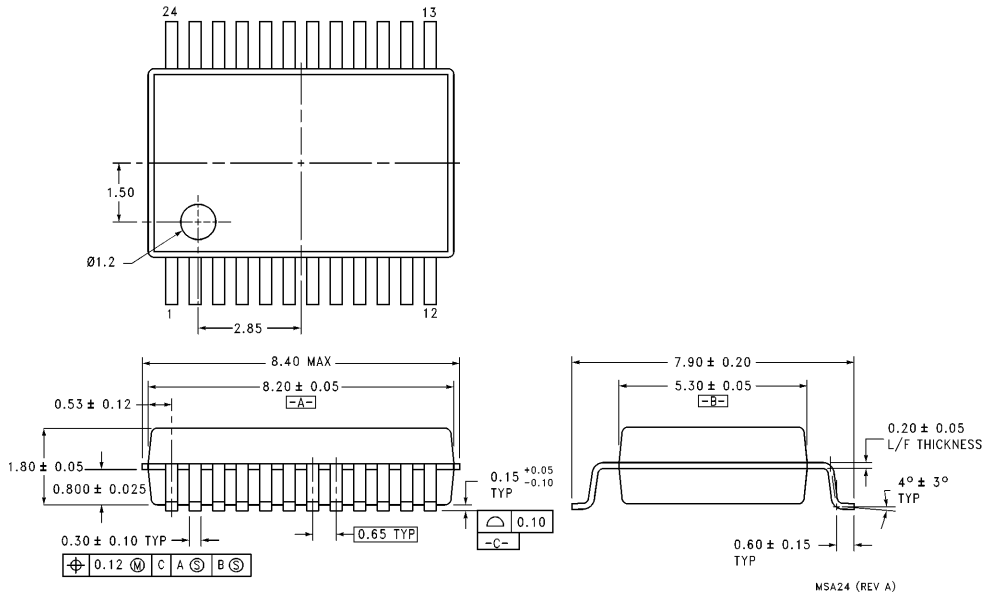
Side View Dimensions:

- Pin pitch: 0.075 ± 0.015 (1.905 $\pm$ 0.381)
- Pin height: 0.065 (1.651)
- Pin diameter: 0.040 (1.016) TYP
- Pin spacing: 0.130 ± 0.005 (3.302 $\pm$ 0.127)
- Pin diameter: 0.020 (0.508) MIN
- Pin diameter: $0.145 - 0.200$ (3.683 - 5.080)
- Pin diameter: $0.125 - 0.145$ (3.175 - 3.556) MIN
- Pin diameter: 0.018 ± 0.003 (0.457 $\pm$ 0.076) TYP
- Pin diameter: 0.100 ± 0.010 (2.54 $\pm$ 0.254) TYP
- Pin diameter: $90^\circ \pm 4^\circ$ TYP

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Physical Dimensions inches (millimeters) (Continued)

Lit. # 114647



**24-Lead Molded Shrink Small Outline Package, EIAJ Type II (MSA)
NS Package Number MSA24**

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