National Semiconductor

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74ACTQ3283T 32-Bit Latchable Transceiver with Parity Generator/Parity Checker and Byte Multiplexing with TRI-STATE® Outputs

General Description

The 'ACTQ3283T is a 32-bit latchable transceiver with parity checker/generator. The device can operate as a transceiver generating parity in the A-B direction and checking it in the B-A direction. It can be used to multiplex between data bytes, and provides an easy interface between 32-bit and 8- or 16-bit data busses. It has a guaranteed current sink/source capacity of 24 mA, and features reduced voltage swing outputs to improve output noise and EMI crosstalk.

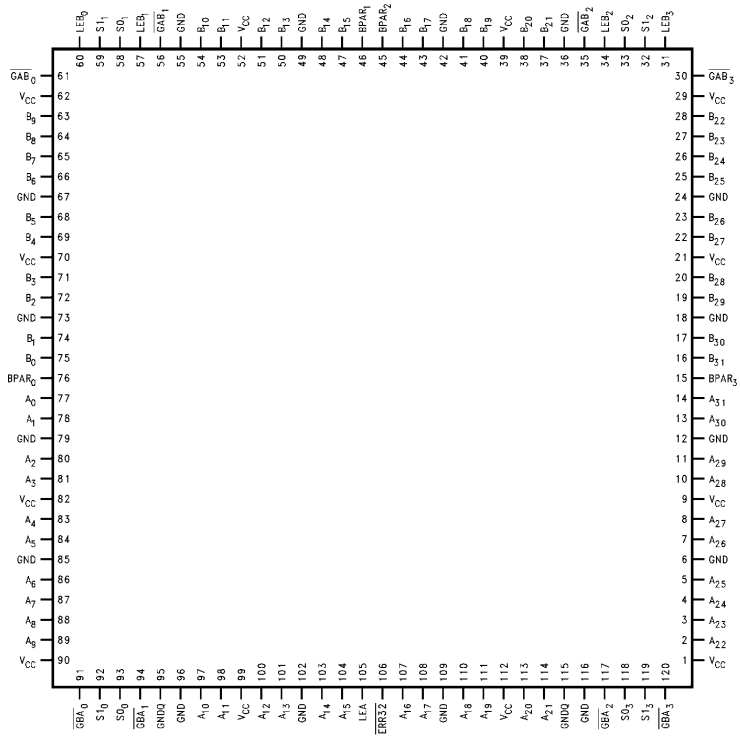
The 'ACTQ3283T features independent latch enables for the B side, and a 32-bit latch enable for the A side. Each byte is selectable separately for complete byte-wide multiplex control.

Features

- Utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control for superior performance
- Reduced voltage swing outputs for lower EMI
- Latchable transceiver with 24 mA source/sink capability
- Even parity generation in A-B direction and 32-bit parity check in B-A direction
- Fully selectable byte multiplexing allows byte swapping, byte copying, and 32-bit to 8-bit/16-bit multiplexing
- Separate control logic for each byte

Connection Diagram

Pin Assignment for PQFP



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74ACTQ3283T 32-Bit Latchable Transceiver with Parity Generator/Parity Checker and Byte Multiplexing with TRI-STATE Outputs

Functional Description

The 'ACTQ3283T can operate in transparent or latched modes, with complete byte multiplexing selectable at every byte. For the following descriptions data byte will be referred to as A_n or B_n, the n refers to 0–3 thus representing bytes A_0, A_1, A_2 or A_3.

— Byte A_n to B_n (Feedthrough mode), LEA is held HIGH to put latch in transparent mode. Parity is generated for each byte and select pins $S0_n$ and $S1_n$ select which data byte (A_0–A_3) is fed through.

— Byte B_n to A_n (Feedthrough mode), LEB_n is held HIGH to put latch in transparent mode. Parity is checked for each byte and $\overline{ERR32}$ goes LOW if there is one or more parity errors. Select pins $S0_n$ and $S1_n$ select which data byte (B_0–B_3) is fed through.

— Independent Latch enables LEA, LEB_0, LEB_1, LEB_2 and LEB_3 provide means of latching data at the A bus or at any byte (B_0–B_3) on the B bus. Select pins $S0_n$ and $S1_n$ select which data byte output. See function table and select table for further information.

Pin Description

Pin Names	Description
A_0–A_7	A_0 Byte Inputs/Outputs
A_8–A_{15}	A_1 Byte Inputs/Outputs
A_{16}–A_{23}	A_2 Byte Inputs/Outputs
A_{24}–A_{31}	A_3 Byte Inputs/Outputs
B_0–B_7	B_0 Byte Inputs/Outputs
B_8–B_{15}	B_1 Byte Inputs/Outputs
B_{16}–B_{23}	B_2 Byte Inputs/Outputs
B_{24}–B_{31}	B_3 Byte Inputs/Outputs
$\overline{GAB}_0$–$\overline{GAB}_3$	Output Enable for Byte B_0–B_3, Organized Byte Wide, Active LOW
$\overline{GBA}_0$–$\overline{GBA}_3$	Output Enable for Byte A_0–A_3, Organized Byte Wide, Active LOW
LEA	Latch Enable for A_0, A_1, A_2 and A_3. HIGH for Transparent mode.
LEB_0–LEB_3	Latch Enable for B_0–B_3 Organized byte wide. HIGH for Transparent mode.
$S0_0$–$S0_3$ $S1_0$–$S1_3$	Select Pins for Byte Multiplexing, Organized by Byte.
$BPAR_0$–$BPAR_3$	Parity bit input/output, one per byte B side only. LOW for EVEN parity.
$\overline{ERR32}$	32-bit parity error, generated by bytes B_0–B_3 and $BPAR_0$–$BPAR_3$. LOW indicates parity error on ONE or MORE of B side bytes.

Select Table

Inputs		Operation
$S1_n$	$S0_n$	
0	0	Byte 0 Data Selected
0	1	Byte 1 Data Selected
1	0	Byte 2 Data Selected
1	1	Byte 3 Data Selected

Select pins for the 'ACTQ3283T are organized by byte, and allow for complete byte multiplexing of data. Two control pins S0 and S1 are available for each byte, and the data is selected as described in the Select Tabe for both the A–B and B–A direction.

Function Table

Inputs						Operation
$\overline{GAB}_n$	$\overline{GBA}_n$	LEA	LEB_n	$S1_n$	$S0_n$	
H	H	X	X	X	X	Busses A_n and B_n are in TRI-STATE
L	H	H	X	L	L	Data on bus A_0 is fed through to B_n Parity $BPAR_n$ is generated from A_0
L	H	H	X	L	H	Data on bus A_1 is fed through to B_n Parity $BPAR_n$ is generated from A_1
L	H	H	X	H	L	Data on bus A_2 is fed through to B_n Parity $BPAR_n$ is generated from A_2
L	H	H	X	H	H	Data on bus A_3 is fed through to B_n Parity $BPAR_n$ is generated from A_3
H	L	X	H	L	L	Data on bus B_0 is fed through to A_n Parity is checked by B_n and $BPAR_n$ $\overline{ERR32}$ is pulled LOW on parity ERROR
H	L	X	H	L	H	Data on bus B_1 is fed through to A_n Parity is checked by B_n and $BPAR_n$ $\overline{ERR32}$ is pulled LOW on parity ERROR
H	L	X	H	H	L	Data on bus B_2 is fed through to A_n Parity is checked by B_n and $BPAR_n$ $\overline{ERR32}$ is pulled LOW on parity ERROR
H	L	X	H	H	H	Data on bus B_3 is fed through to A_n Parity is checked by B_n and BPARn $\overline{ERR32}$ is pulled LOW on parity ERROR
L	H	L	X	X	X	Data on bus A is latched and output on B_n based on the select signals
H	L	X	L	X	X	Data on bus B_n is latched and output on A_n based on the select signals

H = High Voltage Level

L = Low Voltage Level

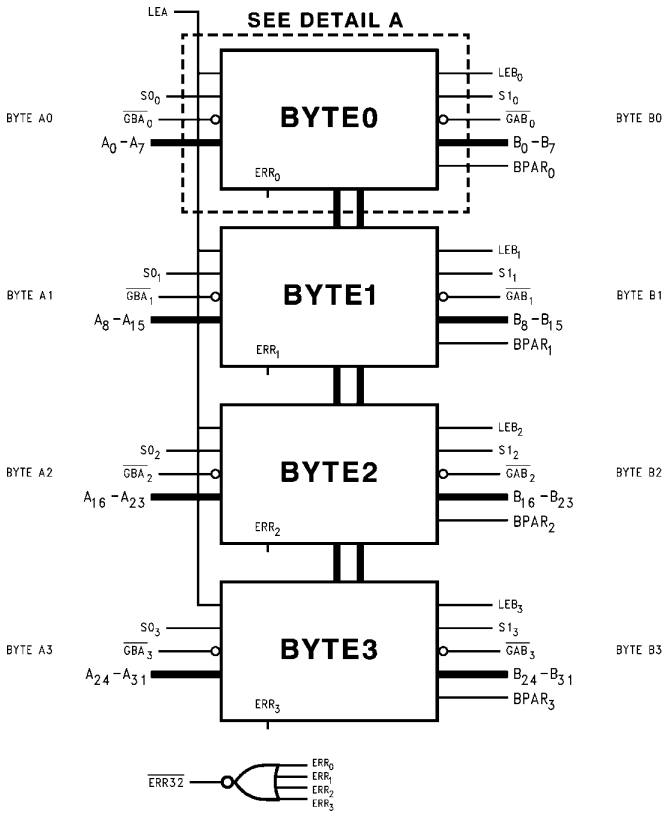
X = Immaterial

A_n – indicates byte A_0, A_1, A_2 or A_3

B_n – indicates byte B_0, B_1, B_2 or B_3

A_0 – indicates byte 0, or pins A_0–A_7

Logic Diagrams



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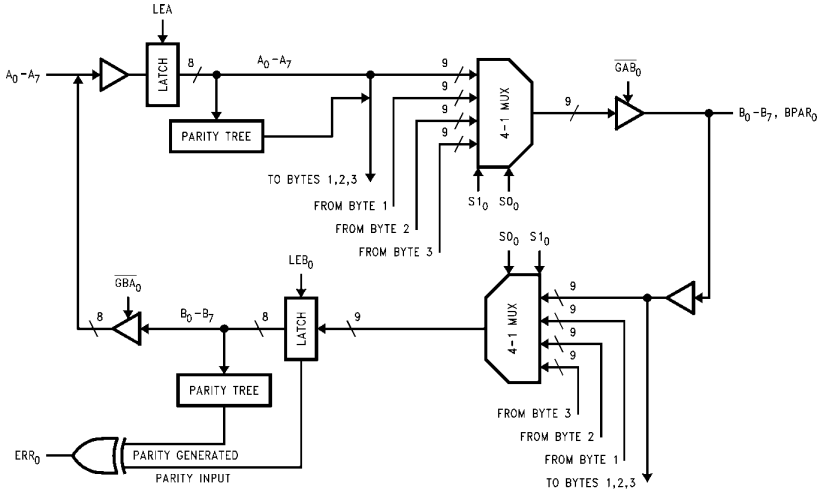
Detail A



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	±50 mA
Junction Temperature PQFP	+140°C
Storage Temperature	−65°C to +150°C
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACTQ	−40°C to +85°C
Minimum Input Edge Rate dV/dt	
'ACTQ Devices	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics for ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ		74ACTQ	Units	Conditions
			+25°C		−40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{OH}
V_{IL}	Maximum Low Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{OH}
V_{OH}	Minimum High Output Voltage	4.5 5.5		3.15 3.85	3.15 3.85	V	$I_{OUT} = -50\ \mu A$
		4.5 5.5		2.0 2.0	2.0 2.0	V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50\ \mu A$
		4.5 5.5		0.36 0.36	0.44 0.44	V	$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			63	mA	V_{OLD} = 0.8V Max
I_{OHD}					−40	mA	V_{OHD} = 2.0V Min
I_{OZT}	Max I/O Leakage Current	5.5		±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH}

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ		74ACTQ	Units	Conditions
			+25°C		−40°C to +85°C		
			Typ	Guaranteed Limits			
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.7	1.2		V	*Figures 9, 10* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.7	−1.2		V	*Figures 9, 10* (Notes 2, 3)
V_{OHP}	Maximum Overshoot	5.0	V_{OH} + 0.6	V_{OH} + 1.2		V	*Figures 9, 10* (Notes 1, 3)
V_{OHV}	Minimum V_{CC} Droop	5.0	V_{OH} − 0.3	V_{OH} − 0.7		V	*Figures 9, 10* (Notes 1, 3)
V_{IHD}	Minimum High Dynamic Input Voltage Level	5.0	1.7	2.0		V	(Notes 1, 4)
V_{ILD}	Maximum Low Dynamic Input Voltage Level	5.0	1.2	0.8		V	(Notes 1, 4)

Note 1: Worst case package.

Note 2: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 3: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 4: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V ('ACTQ). Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ			74ACTQ		Units	Fig. No.
			+25°C 50 pF			−40°C to +85°C 50 pF			
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A to B	5.0	3.5	7.6	9.7	3.5	10.8	ns	1
t_{PLH} t_{PHL}	Propagation Delay B to A	5.0	3.5	8.9	11.2	3.5	12.5	ns	1
t_{PLH} t_{PHL}	Propagation Delay A to $BPAR_n$	5.0	4.5	9.6	12.1	4.5	13.6	ns	3
t_{PLH} t_{PHL}	Propagation Delay B to $\overline{ERR32}$	5.0	5.0	12.0	14.8	5.0	16.7	ns	4
t_{PLH} t_{PHL}	Propagation Delay $BPAR_n$ to $\overline{ERR32}$	5.0	3.5	10.5	13.2	3.5	14.8	ns	4
t_{PLH} t_{PHL}	Propagation Delay LEA to B_n	5.0	4.5	8.8	10.9	4.5	12.1	ns	2
t_{PLH} t_{PHL}	Propagation Delay LEA to $BPAR_n$	5.0	5.0	10.6	13.1	5.0	14.7	ns	2
t_{PLH} t_{PHL}	Propagation Delay LEB_n to A_n	5.0	4.5	8.7	10.9	4.5	12.3	ns	2
t_{PLH} t_{PHL}	Propagation Delay $S0/S1_n$ to A_n	5.0	4.5	9.3	11.6	4.5	12.9	ns	5
t_{PLH} t_{PHL}	Propagation Delay $S0/S1_n$ to B_n $S0/S1_n$ to BPARn	5.0	3.5	8.6	10.9	3.5	12.1	ns	5
t_{PZL} t_{PZH}	Enable Time	5.0	2.5	7.6	9.8	2.5	10.8	ns	6, 7
t_{PLZ} t_{PHZ}	Disable Time	5.0	1.0	4.5	6.6	1.0	7.2	ns	6, 7

*Voltage range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACTQ	74ACTQ	Units
			Typical $T_A = +25°C$	Commercial $T_A = -40°C$ to $+85°C$	
t_s	Setup Time A_n to LEA	5.0	1.0	3.0	ns
t_s	Setup Time B_n, $BPAR_n$ to LEB_n	5.0	1.0	3.0	ns
t_h	Hold Time A_n to LEA	5.0	1.0	1.5	ns
t_h	Hold Time B_n, $BPAR_n$ to LEB_n	5.0	1.0	1.5	ns
t_w	Min Pulse Width LEA	5.0	1.5	4.0	ns
t_w	Min Pulse Width LEB_n	5.0	1.5	4.0	ns

*Voltage range 5.0 is 5.0V ±0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	74ACTQ		74ACTQ		74ACTQ		Units
		T_A = Com V_{CC} = Com C_L = 50 pF 32 Outputs Switching (Note 1)		$T_A = -40°C$ to $+85°C$ V_{CC} = Com C_L = 250 pF (Note 2) 1 Output Switching		$T_A = -40°C$ to $+85°C$ V_{CC} = Com C_L = 250 pF (Notes 1, 2) 32 Outputs Switching		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A to B	4.5	11.8	5.0	14.5	6.0	15.5	ns
t_{PLH} t_{PHL}	Propagation Delay B to A	5.0	13.0	5.0	15.0	6.0	16.0	ns
t_{PLH} t_{PHL}	Propagation Delay A to $BPAR_n$	5.5	14.5	6.0	17.0	7.0	19.0	ns
t_{PLH} t_{PHL}	Propagation Delay B to $\overline{ERR32}$	6.0	17.5	7.0	19.5	8.0	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay $BPAR_n$ to $\overline{ERR32}$	4.5	15.5	5.0	17.5	6.0	19.5	ns
t_{PLH} t_{PHL}	Propagation Delay LEA to B_n	5.0	13.0	6.0	15.5	7.0	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay LEA to $BPAR_n$	6.0	15.5	6.5	18.5	7.5	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay LEB_n to A_n	5.0	14.0	5.5	16.0	7.0	18.0	ns
t_{PLH} t_{PHL}	Propagation Delay $S0_n/S1_n$ to A_n	6.0	17.0	7.0	20.0	8.0	21.0	ns
t_{PLH} t_{PHL}	Propagation Delay $S0_n/S1_n$ to B_n $S0_n/S1_n$ to $BPAR_n$	5.0	13.0	5.5	16.5	6.0	18.0	ns
t_{PZL} t_{PZH}	Enable Time			(Note 3)				ns
t_{PLZ} t_{PHZ}	Disable Time			(Note 4)				ns

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (il.e., all low-to-high, high-to-low, etc.).

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 3: TRI-STATE delays are load dominated and have been excluded from the datasheet.

Note 4: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	7.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	62	pF	V_{CC} = 5.0V

AC Path

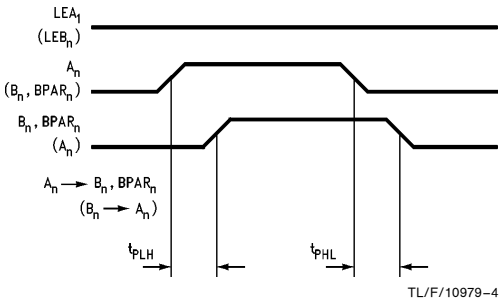

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FIGURE 1

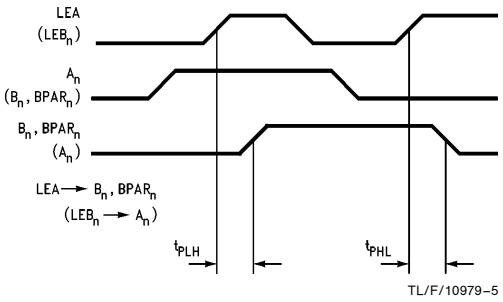

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FIGURE 2

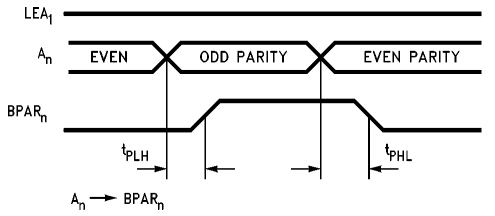

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FIGURE 3

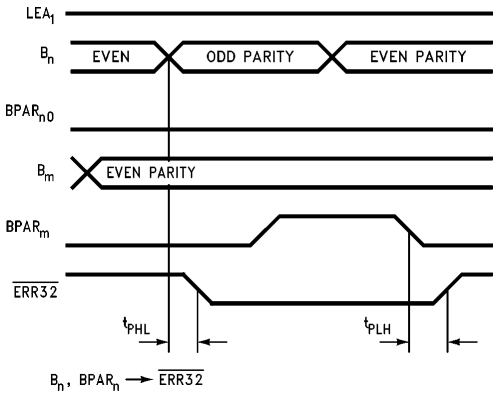

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FIGURE 4

AC Path (Continued)

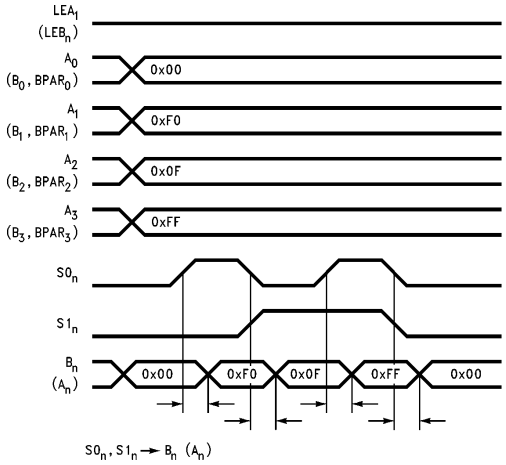

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FIGURE 5. 32-Bit to 8-Bit Multiplexing

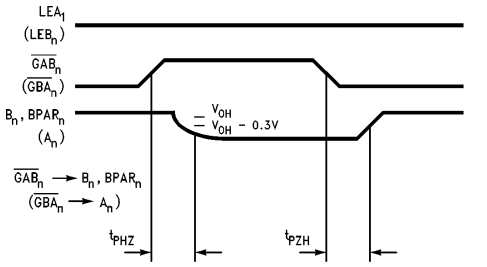

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FIGURE 6

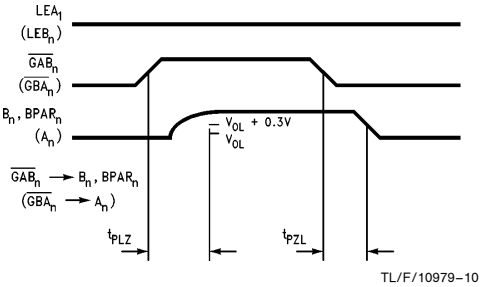

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FIGURE 7

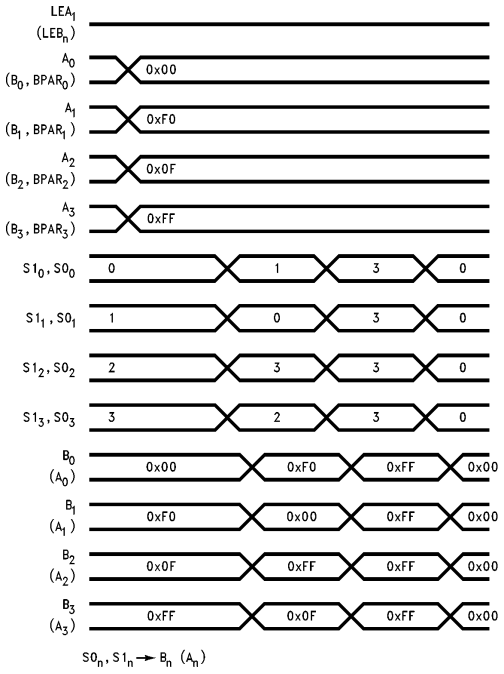

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FIGURE 8. Byte Swapping and Byte Copying

Application 1: 32-Bit or 2/16-Bit Data Buffer and Parity Generate/Check

Detailed Pin Description

The following is a table that relates the pin names of the discrete implementation to the 'ACTQ3283T. Also listed are the number of pins, the type of each pin and the function performed.

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type*	Function
A_0–A_7 A_8–A_{15} A_{16}–A_{23} A_{24}–A_{31}	A_{00}–A_{07} A_{08}–A_{15} A_{16}–A_{23} A_{24}–A_{31}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from A bus to B bus the signal associations are: A_0–A_7 B_0–B_7 A_8–A_{15} B_8–B_{15} A_{16}–A_{23} B_{16}–B_{23} A_{24}–A_{31} B_{24}–B_{31}
B_0–B_7 B_8–B_{15} B_{16}–B_{23} B_{24}–B_{31}	B_{00}–B_{07} B_{08}–B_{15} B_{16}–B_{23} B_{24}–B_{31}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from B bus to A bus the signal associations are: B_0–B_7 A_0–A_7 B_8–B_{15} A_8–A_{15} B_{16}–B_{23} A_{16}–A_{23} B_{24}–B_{31} A_{24}–A_{31}
$BPAR_0$–$BPAR_3$	$BPAR_0$–$BPAR_3$	4	I/O	When data is transferred from the A side to the B side each parity bit will be generated to perform even parity for each byte. Data transferred from the B side to the A side will provide the parity bit which will be checked internally.
$\overline{GAB}_0$–$\overline{GAB}_3$	$\overline{EN}_0$–$\overline{EN}_3$ T/$\overline{R}$ (L) T/$\overline{R}$ (H)	4	I	A output enables. When this signal is low the data on the A side, latched or active will be output to the B side. Signal associations are: $\overline{GAB}_0$ A_0–A_7 B_0–B_7 $\overline{GAB}_1$ A_8–A_{15} B_8–B_{15} $\overline{GAB}_2$ A_{16}–A_{23} B_{16}–B_{23} $\overline{GAB}_3$ A_{24}–A_{31} B_{24}–B_{31}

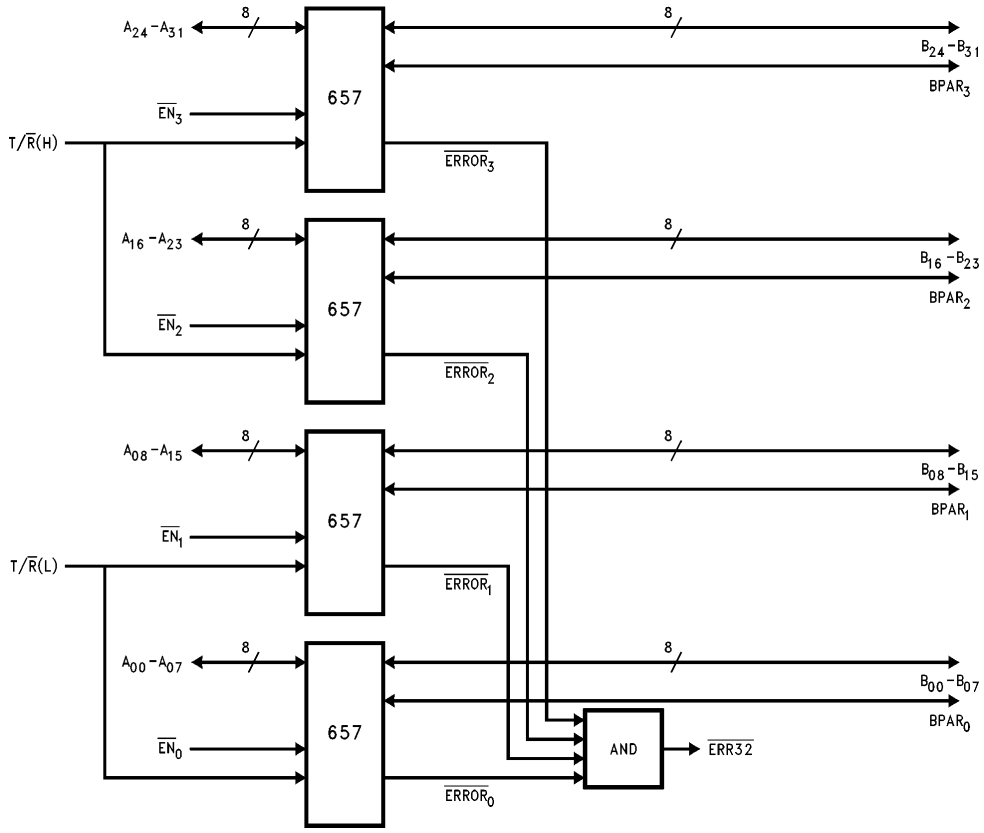
*I = Input, O = Output

Application 1: 32-Bit or 2/16-Bit Data Buffer and Parity Generate/Check
(Continued)

Detailed Pin Description (Continued)

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
$\overline{GBA}_0$–$\overline{GBA}_3$	$\overline{EN}_0$–$\overline{EN}_3$ T/$\overline{R}$ (L) T/$\overline{R}$ (H)	4	I	B output enables. When this signal is low the data on the B side, latched or active will be output to the A side. Signal associations are: $\overline{GAB}_0$ B_0–B_7 A_0–A_7 $\overline{GAB}_1$ B_8–B_{15} A_8–A_{15} $\overline{GAB}_2$ B_{16}–B_{23} A_{16}–A_{23} $\overline{GAB}_3$ B_{24}–B_{31} A_{24}–A_{31}
$\overline{ERR32}$	$\overline{ERR32}$	1	O	This pin indicates if any one or more bytes had a parity error.

Application 1: 32-Bit or 2/16-Bit Data Buffer and Parity Generate/Check



TL/F/10979–12

Application 2: 16-Bit Data and 16-Bit Address Buffer

Detailed Pin Description

The following is a table that relates the pin names of the discrete implementation to the 'ACTQ3283T. Also listed are the number of pins, the type of each pin and the function performed.

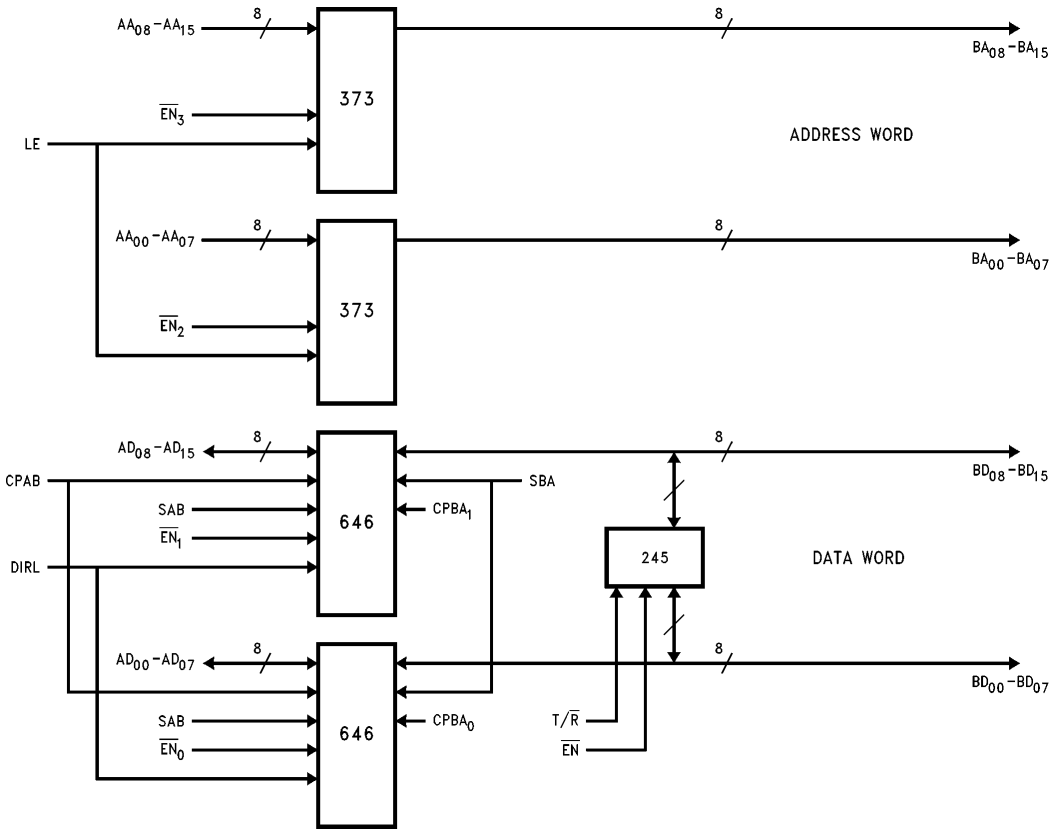
'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
A_0–A_7 A_8–A_{15} A_{16}–A_{23} A_{24}–A_{31}	AD_{00}–AD_{07} AD_{08}–AD_{15} AA_{00}–AA_{07} AA_{08}–AA_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from A bus to B bus the signal associations are: A_0–A_7 B_0–B_7 A_8–A_{15} B_8–B_{15} A_{16}–A_{23} B_{16}–B_{23} A_{24}–A_{31} B_{24}–B_{31}
B_0–B_7 B_8–B_{15} B_{16}–B_{23} B_{24}–B_{31}	BD_{00}–BD_{07} BD_{08}–BD_{15} BA_{16}–BA_{23} BA_{24}–BA_{31}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from B bus to A bus the signal associations are: B_0–B_7 A_0–A_7 B_8–B_{15} A_8–A_{15} B_{16}–B_{23} A_{16}–A_{23} B_{24}–B_{31} A_{24}–A_{31}
$BPAR_0$–$BPAR_3$	$BPAR_0$–$BPAR_3$	4	I/O	Each BPAR pin should be tied to V_{CC} through a suitable resistor if parity is not used.
$\overline{GAB}_0$–$\overline{GAB}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL	4	I	A output enables. When this signal is low the data on the A side, latched or active will be output to the B side. Signal associations are: $\overline{GAB}_0$ A_0–A_7 B_0–B_7 $\overline{GAB}_1$ A_8–A_{15} B_8–B_{15} $\overline{GAB}_2$ A_{16}–A_{23} B_{16}–B_{23} $\overline{GAB}_3$ A_{24}–A_{31} B_{24}–B_{31}
$\overline{GBA}_0$–$\overline{GBA}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL	4	I	B output enables. When this signal is low the data on the B side, latched or active will be output to the A side. Signal associations are: $\overline{GBA}_0$ B_0–B_7 to A_0–A_7 $\overline{GBA}_1$ B_8–B_{15} to A_8–A_{15} $\overline{GBA}_2$ Tied high for this app. $\overline{GBA}_3$ Tied high for this app.
LEA	LE CPAB	1	I	Will latch in the address and data.
LEB_0–LEB_3	$CPBA_0$ $CPBA_1$	4	I	Individual B byte latch enable. When in high state, B data is transparent and if in low state, B data is latched LEB_0 H or L LEB_1 H or L LEB_2 Low for this app. LEB_3 Low for this app.

Application 2: 16-Bit Data and 16-Bit Address Buffer (Continued)

Detailed Pin Description (Continued)

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
$S0_0$–$S0_3$ $S1_0$–$S1_3$	T/$\overline{R}$ (245) $\overline{EN}$ (245)	8	I	These pins allow byte multiplexing, organized by byte, Each byte may be directed to any other byte by setting S0, S1 in a binary fashion to select the stimulus. For this application: $S1_0$ = L $S0_0$ = L B_0 selected at B_0 $S1_0$ = L $S0_0$ = H B_1 selected at B_0 $S1_1$ = L $S0_1$ = L B_0 selected at B_1 $S1_1$ = L $S0_1$ = H B_1 selected at B_1 $S1_2$ = H $S0_2$ = L B_2 selected at B_2 $S1_2$ = H $S0_3$ = H B_3 selected at B_3
N/A	SAB SBA			Select of active byte or latched byte not available.

Application 2: 16-Bit Data and 16-Bit Address Buffer (Continued)



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Application 3: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer

Detailed Pin Description

The following is a table that relates the pin names of the discrete implementation to the 'ACTQ3283T. Also listed are the number of pins, the type of each pin and the function performed.

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
A_0–A_7 A_8–A_{15} A_{16}–A_{23} A_{24}–A_{31}	AD_{00}–A_{07} AD_{08}–A_{15} AA_{00}–A_{07} AA_{08}–A_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from A bus to B bus the signal associations are: A_0–A_7 B_0–B_7 A_8–A_{15} B_8–B_{15} A_{16}–A_{23} B_{16}–B_{23} A_{24}–A_{31} B_{24}–B_{31}
B_0–B_7 B_8–B_{15} B_{16}–B_{23} B_{24}–B_{31}	BD_{00}–B_{07} BD_{08}–B_{15} BA_{00}–B_{07} BA_{08}–B_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from B bus to A bus the signal associations are: B_0–B_7 A_0–A_7 B_8–B_{15} A_8–A_{15} B_{16}–B_{23} A_{16}–A_{23} B_{24}–B_{31} A_{24}–A_{31}
$BPAR_0$–$BPAR_3$	$BPAR_0$–$BPAR_3$	4	I/O	Each BPAR pin should be tied to V_{CC} through a suitable resistor if parity is not used.
$\overline{GAB}_0$–$\overline{GAB}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL DIRH	4	I	A output enables. When this signal is low the data on the A side, latched or active will be output to the B side. Signal associations are: $\overline{GAB}_0$ A_0–A_7 to B_0–B_7 $\overline{GAB}_1$ A_8–A_{15} to B_8–B_{15} $\overline{GAB}_2$ A_{16}–A_{23} to B_{16}–B_{23} $\overline{GAB}_3$ A_{24}–A_{31} to B_{24}–B_{31}
$\overline{GBA}_0$–$\overline{GBA}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL DIRH	4	I	B output enables. When this signal is low the data on the B side, latched or active will be output to the A side. Signal associations are: $\overline{GBA}_0$ B_0–B_7 to A_0–A_7 $\overline{GBA}_1$ B_8–B_{15} to A_8–A_{15} $\overline{GBA}_2$ B_{16}–B_{23} to A_{16}–A_{23} $\overline{GBA}_3$ B_{24}–B_{31} to A_{24}–A_{31}
LEA	CPBA	1	I	Will latch in the 32-bit A bus.
LEB_0–LEB_3	$CPBA_0$ $CPBA_1$ $CPBA_2$ $CPBA_3$	4	I	Individual B byte latch enable. When in high state, B data is transparent and in low state B data is latched. LEB_0 H or L LEB_1 H or L LEB_2 H or L LEB_3 H or L

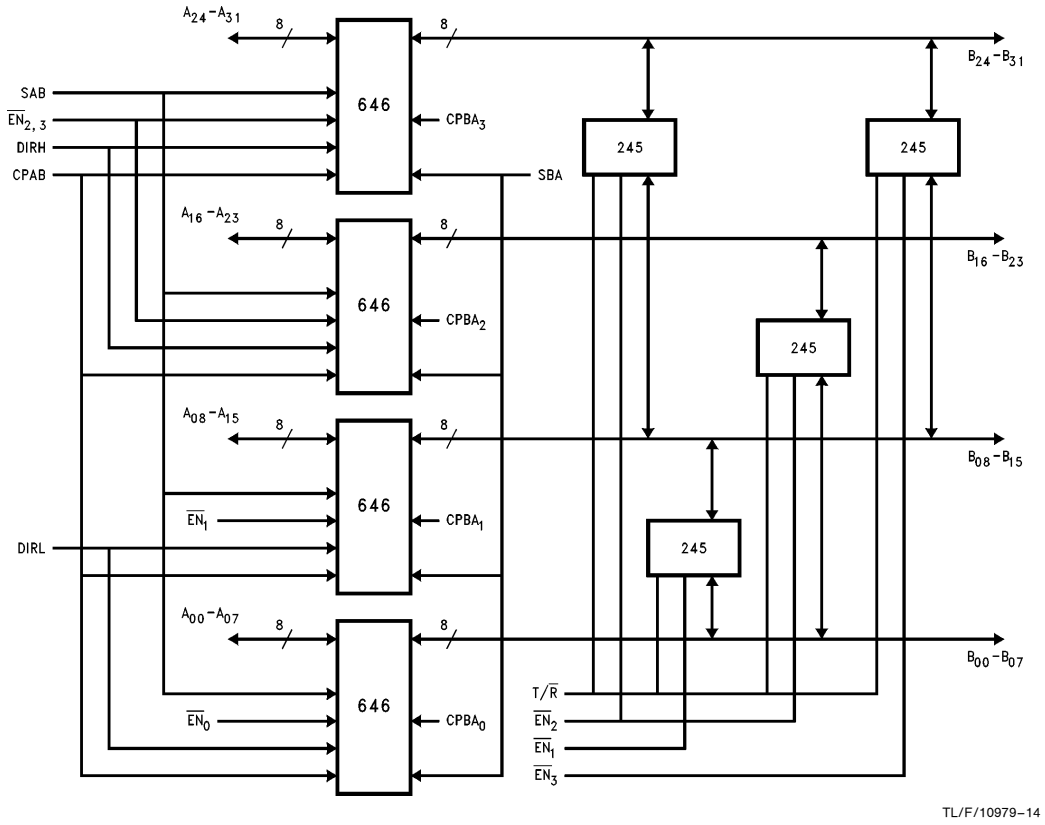
Application 3: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer
(Continued)

Detailed Pin Description (Continued)

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
$S0_0$–$S0_3$ $S1_0$–$S1_3$	T/$\overline{R}$ (245) $\overline{EN}_1$ (245) $\overline{EN}_2$ (245) $\overline{EN}_3$ (245)	8	I	These pins allow byte multiplexing, organized by byte. Each byte may be directed to any other byte by setting S0, S1 in a binary fashion to select the stimulus. For this application: $S1_0 = L$ $S0_0 = L$ A_0 selected at B_0 B_0 selected at A_0 $S1_0 = L$ $S0_0 = H$ A_1 selected at B_0 B_1 selected at A_0 $S1_0 = H$ $S0_0 = L$ A_2 selected at B_0 B_2 selected at A_0 $S1_0 = H$ $S0_0 = H$ A_3 selected at B_0 B_3 selected at A_0 $S1_1 = L$ $S0_1 = L$ A_0 selected at B_1 B_0 selected at A_1 $S1_1 = L$ $S0_1 = L$ A_1 selected at B_1 B_1 selected at A_1 $S1_1 = H$ $S0_1 = H$ A_3 selected at B_1 B_3 selected at A_1 $S1_2 = L$ $S0_2 = L$ A_0 selected at B_2 B_0 selected at A_2 $S1_2 = H$ $S0_2 = L$ A_2 selected at B_2 B_2 selected at A_2 $S1_3 = L$ $S0_3 = L$ A_0 selected at B_3 B_0 selected at A_3 $S1_3 = L$ $S0_3 = H$ A_1 selected at B_3 B_1 selected at A_3 $S1_3 = H$ $S0_3 = H$ A_3 selected at B_3 B_3 selected at A_3

Application 3: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer
(Continued)

Application 3: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer



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Application 4: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer with Parity Generator (A to B)/Check (B to A)

Detailed Pin Description

The following is a table that relates the pin names of the discrete implementation to the 'ACTQ3283T. Also listed are the number of pins, the type of each pin and the function performed.

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
A_0–A_7 A_8–A_{15} A_{16}–A_{23} A_{24}–A_{31}	AD_{00}–A_{07} AD_{08}–A_{15} AA_{00}–A_{07} AA_{08}–A_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from A bus to B bus the signal associations are: A_0–A_7 B_0–B_7 A_8–A_{15} B_8–B_{15} A_{16}–A_{23} B_{16}–B_{23} A_{24}–A_{31} B_{24}–B_{31}
B_0–B_7 B_8–B_{15} B_{16}–B_{23} B_{24}–B_{31}	BD_{00}–BD_{07} BD_{08}–BD_{15} BA_{00}–BA_{07} BA_{08}–BA_{15}	8 8 8 8	I/O I/O I/O I/O	One of the two 32-bit busses serviced by the 'ACTQ3283T. During transfer from B bus to A bus the signal associations are: B_{0-7} A_{0-7} B_{8-15} A_{8-15} B_{16-23} A_{16-23} B_{24-31} A_{24-31}
$BPAR_0$–$BPAR_3$	$BPAR_0$–$BPAR_3$	4	I/O	When the A side data is received a parity bit is generated for each byte and output on the B bus when active. When data is input on the B bus the parity bit is an input which is checked against an internally generated parity bit. $BPAR_0$ Byte 0 $BPAR_1$ Byte 1 $BPAR_2$ Byte 2 $BPAR_3$ Byte 3
$\overline{GAB}_0$–$\overline{GAB}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL DIRH	4	I	A output enables. When this signal is low the data on the A side, latched or active will be output to the B side. Signal associations are: $\overline{GAB}_0$ A_0–A_7 to B_0–B_7 $\overline{GAB}_1$ A_8–A_{15} to B_8–B_{15} $\overline{GAB}_2$ A_{16}–A_{23} to B_{16}–B_{23} $\overline{GAB}_3$ A_{24}–A_{31} to B_{24}–B_{31}
$\overline{GBA}_0$–$\overline{GBA}_3$	$\overline{EN}_0$–$\overline{EN}_3$ DIRL DIRH	4	I	B output enables. When this signal is low the data on the B side, latched or active will be output to the A side. Signal associations are: $\overline{GBA}_0$ B_0–B_7 to A_0–A_7 $\overline{GBA}_1$ B_8–B_{15} to A_8–A_{15} $\overline{GBA}_2$ B_{16}–B_{23} to A_{16}–A_{23} $\overline{GBA}_3$ B_{24}–B_{31} to A_{24}–A_{31}

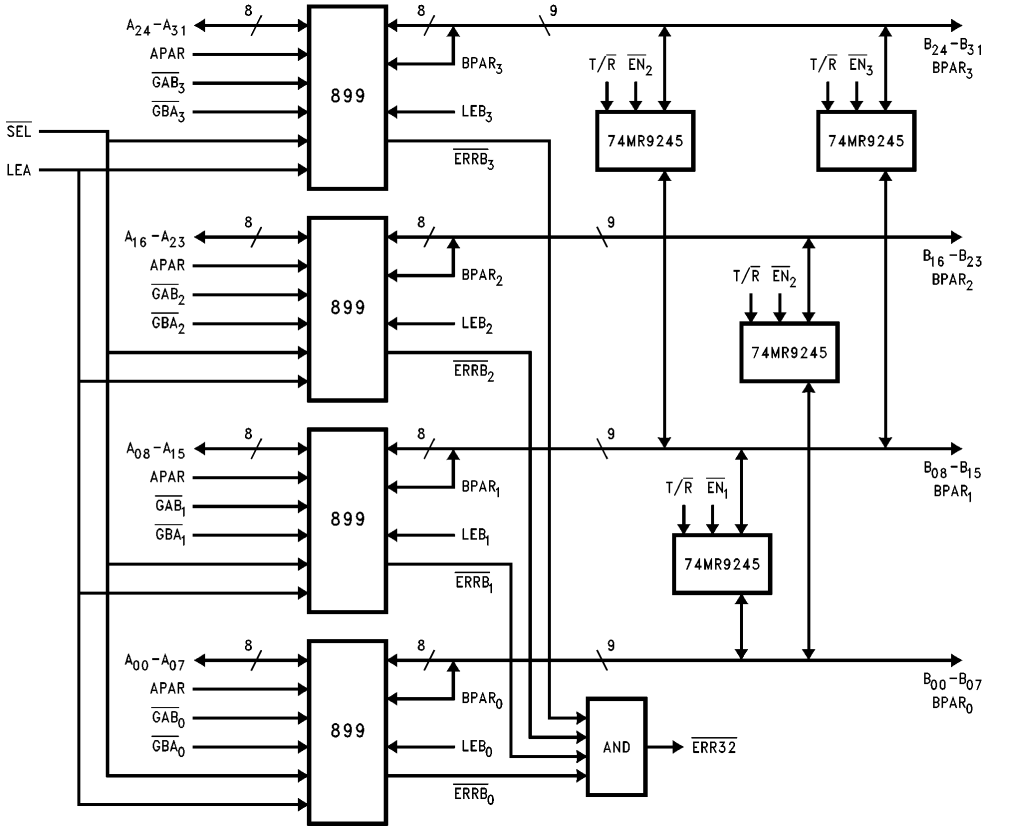
Application 4: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer with Parity Generator (A to B)/Check (B to A) (Continued)

Detailed Pin Description (Continued)

'ACTQ3283T Symbol	Discrete Symbol	# of Pins	Type	Function
LEA	CPAB	1	I	Will latch in the 32-bit A bus.
$\overline{ERR32}$	$\overline{ERR32}$	1	O	Signal that indicates an error in one or more of the bytes.
LEB_0–LEB_3	$CPBA_0$ $CPBA_1$ $CPBA_2$ $CPBA_3$	4	I	Individual B byte latch enable. When in high state B data is transparent and when in low state B data is latched. LEB_0 H or L LEB_1 H or L LEB_2 H or L LEB_3 H or L
$S0_0$–$S0_3$ $S1_0$–$S1_3$	T/$\overline{R}$ (245) $\overline{EN}_1$ (245) $\overline{EN}_2$ (245) $\overline{EN}_3$ (245)	8	I	These pins allow byte multiplexing, organized by byte, Each byte may be directed to any other byte by setting S0, S1 in a binary fashion to select the stimulus. For this application: $S1_0 = L$ $S0_0 = L$ A_0 selected at B_0 B_0 selected at A_0 $S1_0 = L$ $S0_0 = H$ A_1 selected at B_0 B_1 selected at A_0 $S1_0 = H$ $S0_0 = L$ A_2 selected at B_0 B_2 selected at A_0 $S1_0 = H$ $S0_0 = H$ A_3 selected at B_0 B_3 selected at A_0 $S1_1 = L$ $S0_1 = L$ A_0 selected at B_1 B_0 selected at A_1 $S1_1 = L$ $S0_1 = L$ A_1 selected at B_1 B_1 selected at A_1 $S1_1 = H$ $S0_1 = H$ A_3 selected at B_1 B_3 selected at A_1 $S1_2 = L$ $S0_2 = L$ A_0 selected at B_2 B_0 selected at A_2 $S1_2 = L$ $S0_2 = L$ A_2 selected at B_2 B_2 selected at A_2 $S1_3 = L$ $S0_3 = L$ A_0 selected at B_3 B_0 selected at A_3 $S1_3 = L$ $S0_3 = H$ A_1 selected at B_3 B_1 selected at A_3 $S1_3 = H$ $S0_3 = H$ A_3 selected at B_3 B_3 selected at A_3

Application 4: DWORD (32-Bit) to WORD (16-Bit) to BYTE (8-Bit) Transfer with Parity Generator (A to B)/Check (B to A) (Continued)

Application 4: DWORD to WORD to BYTE Transfer with Parity



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/ = 1 byte

\= 1 byte + 1 parity bit

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

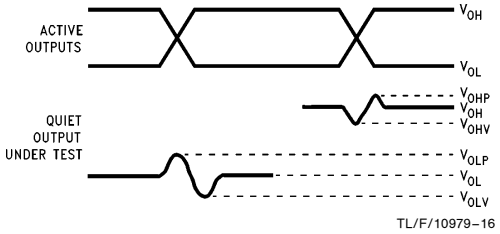


FIGURE 9. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

6. Set the word generator input levels at 0V LOW and 3V HIGH. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

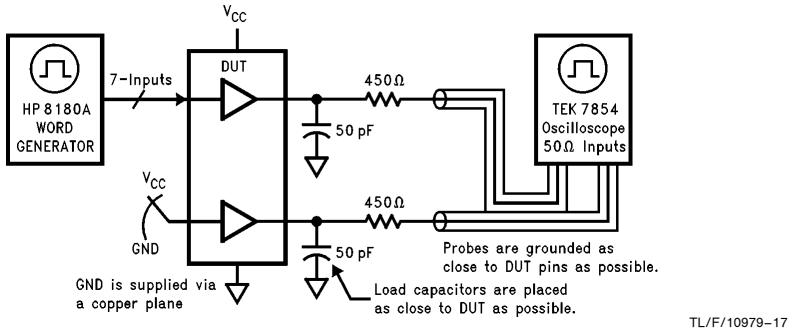
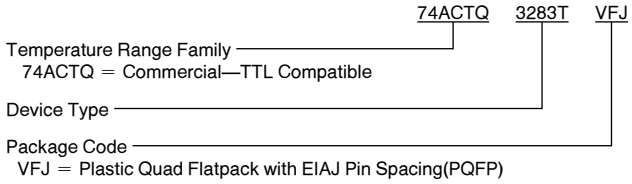


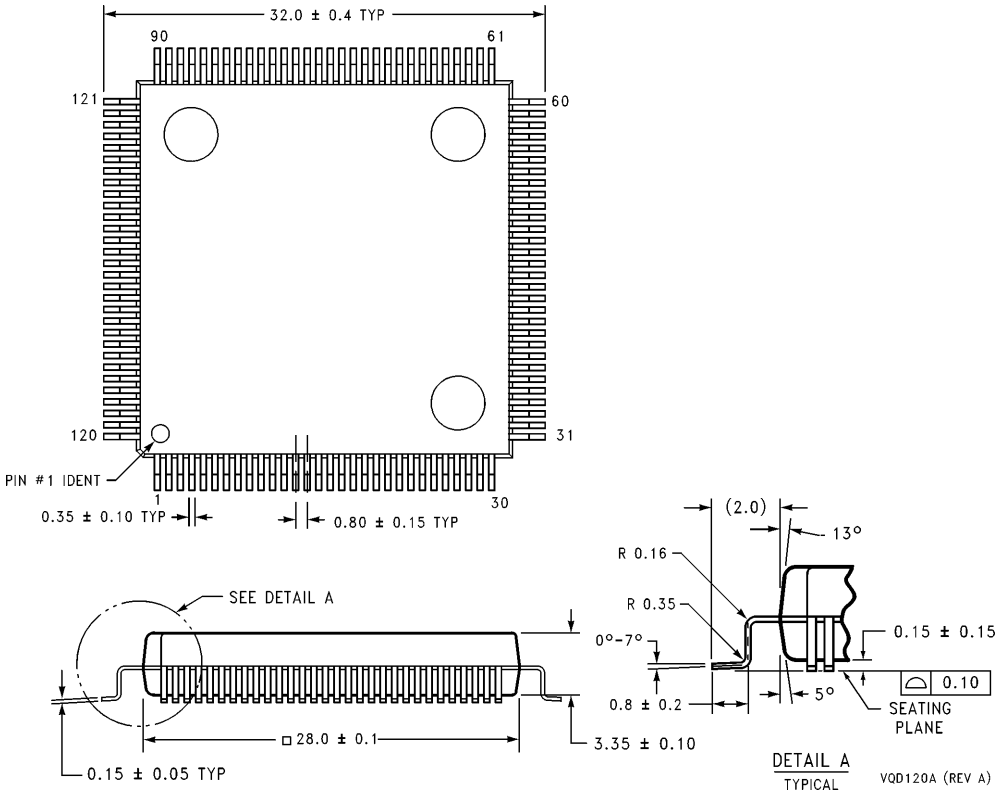
FIGURE 10. Simultaneous Switching Test Circuit

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)



120-Lead PQFP (VFJ)
NS Package Number VQD120A

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