

# 54F/74F657 Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

## General Description

The 'F657 contains eight non-inverting buffers with TRI-STATE® outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA (20 mA mil) at the A port and 64 mA (48 mA mil) at the B port.

## Features

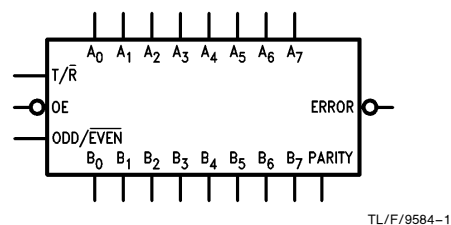
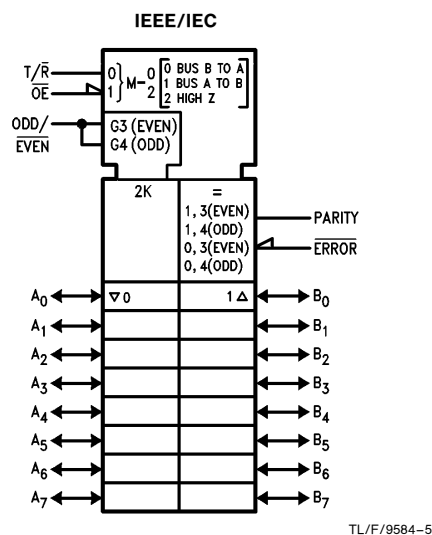
- 300 Mil 24-pin slimline DIP
- Combines 'F245 and 'F280A functions in one package
- TRI-STATE outputs
- B Outputs sink 64 mA (48 mA mil)
- 12 mA source current, B side
- Input diodes for termination effects

Commercial	Military	Package Number	Package Description
74F657SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F657SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
75F657SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F657FM (Note 2)	W24C	24-Lead Cerpack
	54F657LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

**Note 1:** Devices also available in 13" reel. Use suffix = SCX.

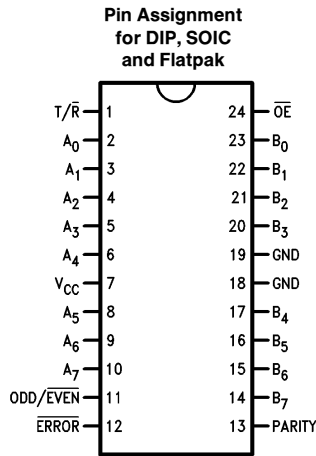
**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

## Logic Symbols

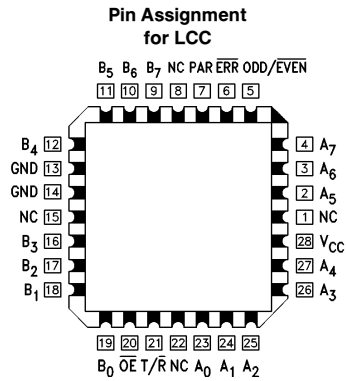


TRI-STATE® is a registered trademark of National Semiconductor Corporation.

## Connection Diagrams



TL/F/9584-2



TL/F/9584-3

## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
A <sub>0</sub> –A <sub>7</sub>	Data Inputs/ TRI-STATE Outputs	4.5/0.15 150/40 (33.3)	90 $\mu$ A/ – 90 $\mu$ A –3 mA/24 mA (20 mA)
B <sub>0</sub> –B <sub>7</sub>	Data Inputs/ TRI-STATE Outputs	3.5/0.117 600/106.6 (80)	70 $\mu$ A/ – 70 $\mu$ A –12 mA/64 mA (48 mA)
T/ $\bar{R}$	Transmit/Receive Input	2.0/0.067	40 $\mu$ A/ – 40 $\mu$ A
$\overline{OE}$	Enable Input	2.0/0.067	40 $\mu$ A/ – 40 $\mu$ A
PARITY	Parity Input/ TRI-STATE Output	3.5/0.117 600/106.6 (80)	70 $\mu$ A/ – 70 $\mu$ A –12 mA/64 mA (48 mA)
ODD/ $\overline{EVEN}$	ODD/ $\overline{EVEN}$ Parity Input	1.0/0.033	20 $\mu$ A/ – 20 $\mu$ A
$\overline{ERROR}$	Error Output	600/106.6 (80)	–12 mA/64 mA (48 mA)

## Functional Description

The Transmit/Receive (T/ $\bar{R}$ ) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A port to the B port; Receive (active LOW) enables data from the B port to the A port.

The Output Enable ( $\overline{OE}$ ) input disables the parity and  $\overline{ERROR}$  outputs and both the A and B ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting (T/ $\bar{R}$  HIGH), the parity generator detects whether an even or odd number of bits on the A port are HIGH and compares these with the condition of the parity select (ODD/ $\overline{EVEN}$ ).

If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode (T/ $\bar{R}$  LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then  $\overline{ERROR}$  will be HIGH to indicate no error. If an odd number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the  $\overline{ERROR}$  will be LOW indicating an error.

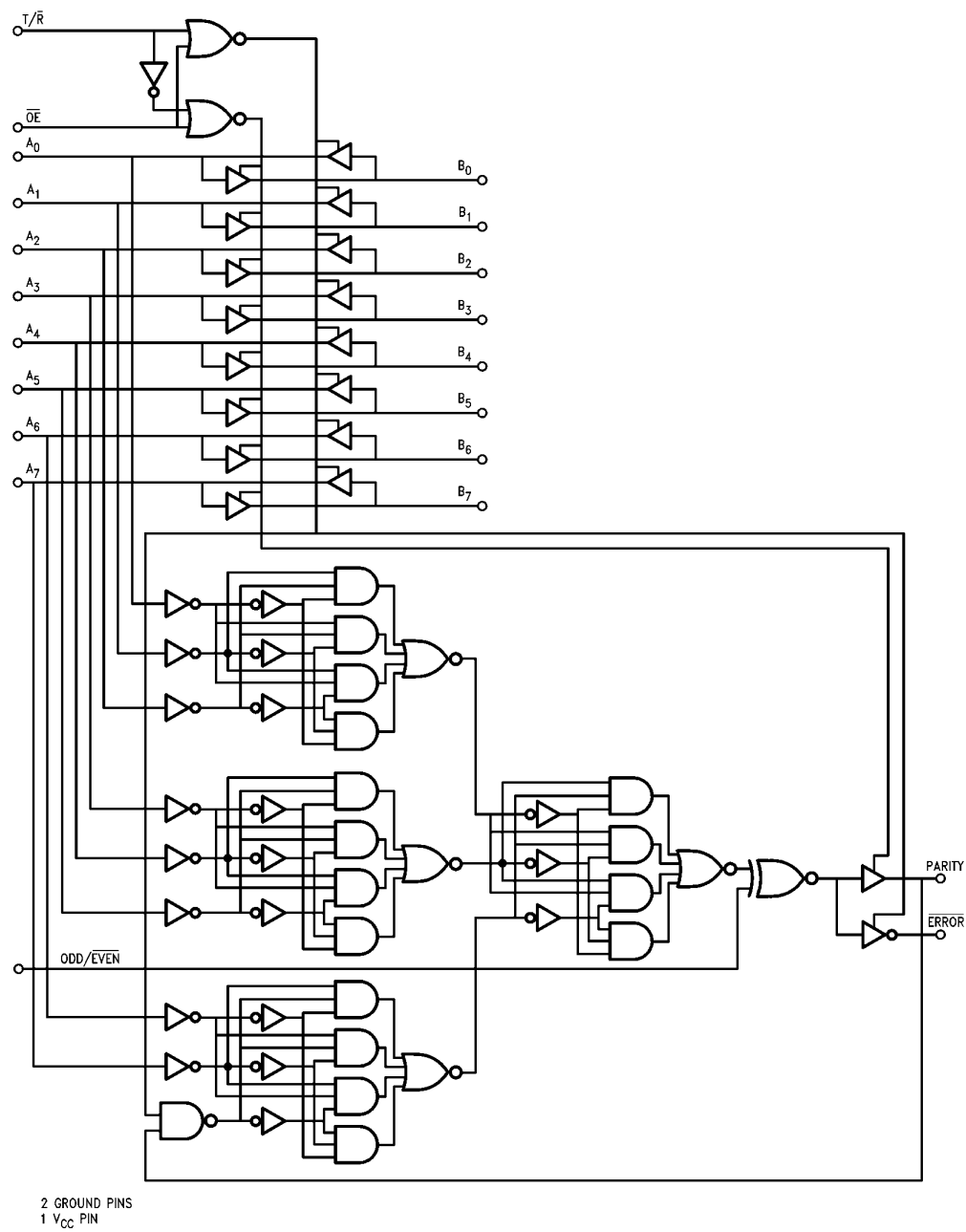
Function Table						
Number of Inputs That Are High	Inputs			Input/Output	Outputs	
	OE	T/R	ODD/EVEN	Parity	ERROR	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

Function Table		
Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

Functional Block Diagram



TL/F/9584-4

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	−55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.0 2.5 2.4 2.0 2.7 2.7		V	Min	I <sub>OH</sub> = −1 mA (A <sub>n</sub> ) I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR) I <sub>OH</sub> = −12 mA (B <sub>n</sub> , Parity, ERROR) I <sub>OH</sub> = −1 mA (A <sub>n</sub> ) I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR) I <sub>OH</sub> = −15 mA (B <sub>n</sub> , Parity, ERROR) I <sub>OH</sub> = −1 mA (A <sub>n</sub> ) I <sub>OH</sub> = −3 mA (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR)
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.55 0.5 0.55	V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> ) I <sub>OL</sub> = 48 mA (B <sub>n</sub> , Parity, ERROR) I <sub>OL</sub> = 24 mA (A <sub>n</sub> ) I <sub>OL</sub> = 64 mA (B <sub>n</sub> , Parity, ERROR)
I <sub>IH</sub>	Input HIGH Current			20 40	μA	Max	V <sub>IN</sub> = 2.7V (ODD/EVEN) V <sub>IN</sub> = 2.7V (T/R, OE)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	V <sub>CC</sub> = 0	V <sub>IN</sub> = 7.0V (T/R, OE, ODD/EVEN)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			1.0 2.0	mA	Max	V <sub>IN</sub> = 5.5V (Parity, B <sub>n</sub> ) V <sub>IN</sub> = 5.5V (A <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current			−20 −40	μA	Max	V <sub>IN</sub> = 0.5V (ODD/EVEN) V <sub>IN</sub> = 0.5V (T/R, OE)
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V (ERROR)
I <sub>OZL</sub>	Output Leakage Current			−50	μA	Max	V <sub>OUT</sub> = 0.5V (ERROR)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70 90	μA	Max	V <sub>I/O</sub> = 2.7V (B <sub>n</sub> , Parity) V <sub>I/O</sub> = 2.7V (A <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			−70 −90	μA	Max	V <sub>I/O</sub> = 0.5V (B <sub>n</sub> , Parity) V <sub>I/O</sub> = 0.5V (A <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	−60 −100	−150 −225		mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> , Parity, ERROR)
I <sub>CEX</sub>	Output HIGH Leakage Current		250 1.0 2.0		μA mA mA	Max Max Max	V <sub>OUT</sub> = V <sub>CC</sub> (ERROR) V <sub>OUT</sub> = V <sub>CC</sub> (B <sub>n</sub> , Parity) V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test		500		μA	0.0V	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> , Parity, ERROR)
I <sub>CCH</sub>	Power Supply Current	101	125		mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current	112	150		mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current	109	145		mA	Max	V <sub>O</sub> = HIGH Z

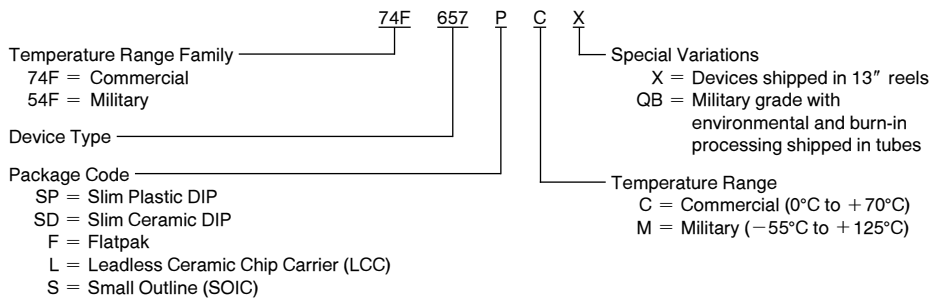
## AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to $B_n$ , $B_n$ to $A_n$	2.5 3.0	4.5 4..9	8.0 7.5	2.5 3.0	9.5 8.5	2.5 3.0	9.0 8.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to Parity	6.5 7.0	10.1 10.9	14.0 15.0	5.5 5.5	18.0 20.5	6.0 6.0	16.0 16.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay ODD/EVEN to PARITY	4.5 4.5	7.8 8.8	11.0 12.0	4.0 4.5	14.0 16.5	4.0 4.5	13.0 13.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay ODD/EVEN to $\overline{\text{ERROR}}$	4.5 4.5	7.5 8.2	11.0 12.0	4.0 4.5	14.0 16.5	4.0 4.5	13.0 13.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $B_n$ to $\overline{\text{ERROR}}$	8.0 8.0	14.0 15.0	20.5 21.5	7.5 7.5	27.0 28.5	7.5 7.5	23.0 23.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay PARITY to $\overline{\text{ERROR}}$	7.0 7.5	10.8 11.8	15.5 16.5	6.0 6.5	20.0 22.0	6.0 7.5	17.0 18.5	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{\text{OE}}$ to $A_n/B_n$	3.0 4.0	5.0 6.5	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{\text{OE}}$ to $A_n/B_n$	1.0 1.0	4.5 4.9	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{\text{OE}}$ to $\overline{\text{ERROR}}$ (Note 1)	3.0 4.0	5.0 7.7	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{\text{OE}}$ to $\overline{\text{ERROR}}$	1.0 1.0	4.5 4.9	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{\text{OE}}$ to PARITY	3.0 4.0	5.0 7.7	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{\text{OE}}$ to PARITY	1.0 1.0	4.6 5.1	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns

**Note 1:** These delay times reflect the TRI-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the ERROR pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the ERROR output after the ERROR pin has been enabled (Output Enable times). VALID data at the ERROR pin  $\geq$  (A to PARITY) + (Output Enable Time).

## Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:









The drawing illustrates the mechanical specifications of the M24B package. The top view shows a rectangular body with 24 pins (13 on top, 12 on bottom) and a lead identification feature. Dimensions include a total length of 15.60 (0.6141, 0.5985, 15.20), a body width of 10.00 (0.4190, 0.3940, 10.65), and a pin pitch of 0.050 (1.27). The side view shows a height of 0.0926 (0.1043, 2.65, 2.35) and a seating plane. The detail view shows a lead height of 0.029 (0.0200, 0.0138, 0.508, 0.350) and a lead width of 0.018 (0.0040, 0.3, 0.1). The package is marked with a diamond symbol, 0.010, 0.25, M, A, C, S, B. The drawing is labeled M24B (REV F).

Technical drawing of a 12-pin connector. The drawing shows two views: a top view and a side view.

**Top View Dimensions:**

- Overall length:  $1.243 - 1.270$  (31.57 - 32.26) MAX
- Pin pitch:  $0.092$  (2.337) (2 PLS)
- Pin 1 location: PIN NO. 1 IDENT
- Option 2: OPTION 2
- Radius:  $0.032$  (0.813) RAD
- Radius:  $0.062$  (1.575) RAD
- Ejector pins: EJECTOR PINS OPTIONAL
- Pin numbers: 1 through 12
- Overall width:  $0.260 \pm 0.005$  (6.604  $\pm$  0.127)

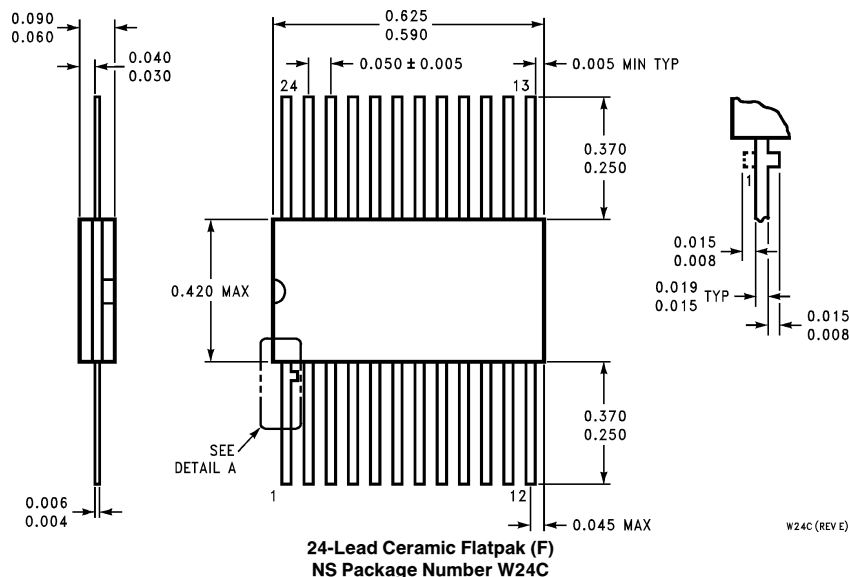
**Side View Dimensions:**

- Pin height:  $0.075 \pm 0.015$  (1.905  $\pm$  0.381)
- Pin width:  $0.065$  (1.651)
- Pin spacing:  $0.040$  (1.016) TYP
- Pin width:  $0.130 \pm 0.005$  (3.302  $\pm$  0.127)
- Pin width:  $0.020$  (0.508) MIN
- Pin width:  $0.145 - 0.200$  (3.683 - 5.080)
- Pin width:  $0.125 - 0.145$  (3.175 - 3.556) MIN
- Pin width:  $0.018 \pm 0.003$  (0.457  $\pm$  0.076) TYP
- Pin width:  $0.100 \pm 0.010$  (2.54  $\pm$  0.254) TYP
- Pin width:  $90^\circ \pm 4^\circ$  TYP

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# 54F/74F657 Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE Outputs

## Physical Dimensions inches (millimeters) (Continued)



### LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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