TDK SEMICONDUCTOR CORP.

78Q2131
1Mbps HomePNA Transceiver

Target Specification

March 2001

DESCRIPTION

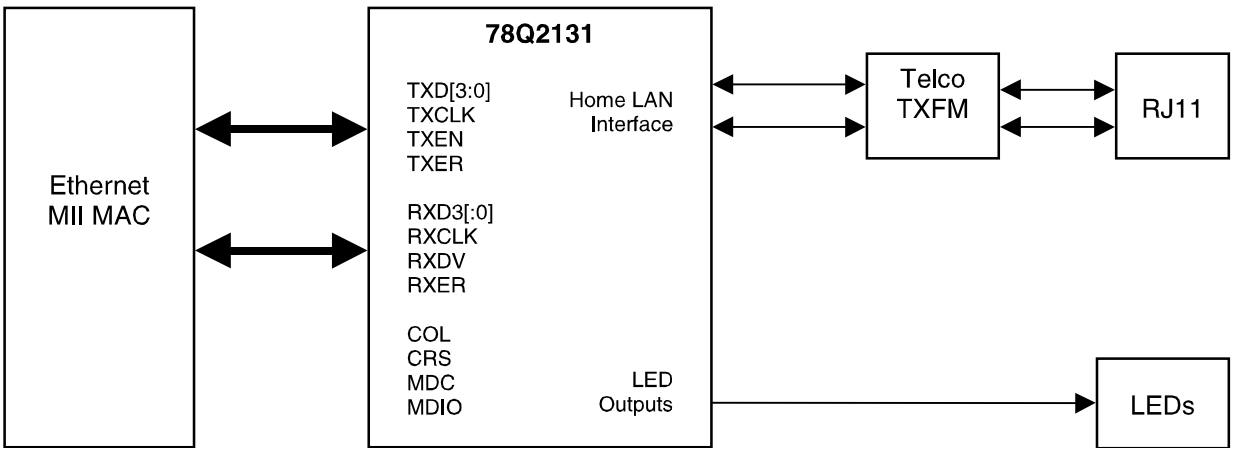
The 78Q2131 is a fully Home Phoneline Networking Alliance (HomePNA) 1.1 compliant 1Mbps transceiver extending Ethernet over POTS. The HomePNA interface includes the pulse encoder and decoder plus transmit and receive line interface filters. Only an isolation transformer and external protection devices are required to complete the interface.

The 78Q2131 also integrates the Media Independent Interface (MII) and General Purpose Serial Interface (GPSI) for connecting to an external Ethernet Media Access Controller (MAC). HomePNA is connected to the line via a HomePNA compatible 1:1 transformer having a series capacitor in the line side. With its integrated filters, the 2131 requires no external filtering in the transformer or board layout. Communication to the MAC is accomplished through an IEEE-802.3 compliant MII or GPSI interface. The product is designed for high performance and low power operation, and can operate from a single 3.3 V or 5 V supply.

FEATURES

- **1M8 Home LAN interface over POTS**
- **HomePNA 1.1 compliant**
- **Integrated HomePNA interface and line filters**
- **Simultaneous Spectral Compatibility with Voice, Fax, ISDN, xDSL, Cable Modem with HomePNA**
- **Integrated MII and GPSI**
- **Power-saving and power-down modes including transmitter disable**
- **Operates with a single 3.3V or 5V supply**
- **LINK, TX, RX, COL, SPD, and PWR LED indicators**
- **User programmable Interrupt pin**
- **General Purpose I/O Interface**
- **80-Lead TQFP or 64-Lead VTQFP package**

TYPICAL APPLICATION DIAGRAM



FUNCTIONAL DESCRIPTION

GENERAL

Supply Voltage

The 78Q2131 can operate from either a single 3.3V (± 10%) or 5.0V (± 10%) power supply. The chip automatically adapts to the supply voltage used. No pin configuration is required.

Power Management

Chip power-down is activated by setting the PWRDN bit in the MII register (MR0.11) or pulling high the PWRDN pin. When the chip is in power-down mode, all on-chip circuitry is shut off, and the device consumes minimum power. While in power-down state, the 78Q2131 still responds to the management transactions.

Analog Biasing

The 78Q2131 uses the onchip bandgap and an external resistor to generate accurate bias voltages and currents for the circuitry.

Clock Input

The 78Q2131 can use the on-chip crystal oscillator. In this mode a 25MHz crystal is connected between the XTALI and XTALO pins. Alternatively, an externally generated 25MHz clock can be connected to the XTALI pin. In conjunction with the oscillator the device uses an internal PLL to generate 60MHz. The HomePNA section uses the time unit, TIC defined as 60MHz/7 (approx. 116.6ns).

HOMEPNA OPERATION

HomePNA Transmit

The 78Q2131 contains all of the necessary pulse waveform circuitry to convert the transmit signaling from a MAC to a HomePNA compliant data-stream. The conversion is from either a 4bit parallel data word via the MII interface or the serial data-stream from GPSI interface to a serial data stream to a RLL25 encoded set of 3 to 6 bits. The value created, between 0 and 24, is used to modulate the time, in TIC increments, between pulse bursts. The pulse bursts are filtered to bandlimit the signal passed to the line driver, and to the line for transmission. The integrated envelope-shaper reduces out-of-band energy to reduce interference. The line driver requires an external 1:1 isolation transformer to interface with the line media. Only an external transient protector and a couple of EMI suppression inductors are required with the transformer. Note the transformer requires a coupling capacitor on the line side.

The 78Q2131 conforms to the required envelope for transmission bursts on the line. See Figure 8 for the detail of a single pulse burst signal.

The output is fed to a bandpass filter to reduce out-of-band components. When not transmitting the transmit circuitry is put into a mode that rejects common-mode signals appearing at the receiver input.

HomePNA Receive

The 78Q2131 receives the encoded digital signal through the same 1:1 transformer used for transmission. The signal is internally filtered and compared to an adjusted noise threshold prior to being decoded. From the resulting signal and internal time reference a value is assigned to the time interval. The value is RLL25 decoded and the bit-stream is presented to the serial to parallel converter. The parallel data from the converter is then aligned and mapped as a 4 bit data for the MII as outlined in Table 24-1 in Clause 24 of IEEE-802.3 or sent to the serial GPSI interface.

The receive channel consists of a prefilter, main filter, FWR, LPF and comparator with adjustable level.

Natural Loopback

When the 78Q2131 is transmitting on the twisted pair media, data on the TXD pins is looped back onto the RXD pins. The natural loopback function can be disabled through register bit MR16.10.

Reference Packet Framing and Sequence

The frame passed between the MAC and 1M8 PHY on TX-DATA and RX-DATA conforms to the 802.3 Ethernet MAC frame. When a pulse begins transmission, the previous Symbol interval ends and a new one immediately begins.

The Run Length Limit (RLL25) code was developed for the 1M8 PHY. It produces both the highest bit rate for a given value of Inter Symbol Blanking Interval (ISBI) and Time Interval Clock (TIC) size. In a manner similar to run length limited disk coding, RLL25 encodes data bits in groups of varying sizes, specifically, 3,4,5 and 6 bits. Pulse positions are assigned to the encoded bit groups in a manner that causes more data bits to be encoded in positions that are farther apart. This keeps both the average and minimum bit rates higher.

HomePNA 1.1 Compatibility

MR19.11 will reflect the version of HomePNA to be utilized to set the Link Status bit MR1.2. When MR19.11 is a logic zero, the device will behave as a HomePNA v1.0 compliant PHY. This will result in the Link Status bit MR1.2 always being logic one. If MR19.11 is set to logic one, the device will behave as a HomePNA 1.1 compliant PHY.

To enable link integrity checking as specified by HomePNA v1.1, the PHY continually checks for packet reception. Upon a lapse of packets greater than 4 seconds, the link status bit, MR1.2, is cleared.

Also, for HomePNA v1.1 compatibility, the PHY can be commanded to place a RUNT or MINIMUM packet out at any time. These packets, along with normal packets, indicate to other transceivers that the link is up when sent at least every 2seconds.

MEDIA INDEPENDENT INTERFACE

MII Transmit and Receive Operation

The MII interface on the 78Q2131 provides an independent transmit and receive path for the 1Mbps HomePNA interface as described in Clause 22 of the IEEE-802.3 standard.

The transmit clock, TX_CLK, provides the timing reference for the transfer of TX_EN, and TXD[3:0], signals from the MAC to the 78Q2131. TXD[3:0] is captured on the rising edge of TX_CLK when TX_EN is asserted.

The receive clock, RX_CLK, provides the timing reference to transfer RX_DV, and RXD[3:0], signals from the 78Q2131 to the MAC. RX_DV transitions synchronously with respect to RX_CLK and is asserted when the 78Q2131 is presenting valid data on RXD[3:0].

General Purpose Serial Interface

The seven signals which comprise the GPSI are TX_CLK, TX_EN, TX_DATA, RX_CLK, RX_DATA, CRS, and CLSN. Of these, only TX_EN and TX_DATA are inputs to the 78Q2131; the other five are outputs from the 78Q2131.

The transmit clock, TX_CLK, provides the timing reference for the transfer of TX_EN and TX_DATA signals from the MAC to the 78Q2131. TX_DATA is captured on the rising edge of TX_CLK when TX_EN is asserted.

The receive clock, RX_CLK, provides the timing reference to transfer the RX_DATA signal from the 78Q2131 to the MAC. RX_DATA transitions synchronously on the rising edge of RX_CLK.

Carrier Sense, CRS, is asserted high whenever a non-idle condition exists on either the receiver or the transmitter. Typically, GPSI MACs will ignore CRS during transmit modes.

The Collision signal, CLSN, indicates a collision has been detected by the 78Q2131 on the wiring network.

MII/GPSI Selection

The MII on the 78Q2131 is internally connected to the transmit and receive paths for the 1M8 HomePNA interface as described in Clause 22 of the IEEE 802.3 standard. The MII_EN pin or MII_Enable bit MR16.1 can select either the MII or GPSI Interface.

Station Management Interface

The station management interface consists of circuitry which implements the serial protocol as described in Clause 22.2.4.4 of IEEE-802.3. A 16-bit shift register receives serial data applied to the MDIO pin at the rising edge of the MDC clock signal. Once the preamble is received, the station management control logic looks for the start-of-frame sequence and a read or write op-code, followed by the PHYAD and REGAD fields. For a read operation, the MDIO port becomes enabled as an output and the register data is loaded into a shift register for transmission. The 78Q2131 can work with a one-bit preamble rather than the 32 bits prescribed by IEEE-802.3. This allows for faster programming of the registers. If a register does not exist at an address indicated by the REGAD field or if the PHYAD field does not match the 78Q2131 PHYAD indicated by the PHYAD pins, a read of the MDIO port will return all ones. For a write operation, the data is shifted in and loaded into the appropriate register after the sixteenth data bit has been received. Writes to registers not supported by the 78Q2131 are ignored.

ADDITIONAL FEATURES

LED Indicators

There are six LED pins that can be used to indicate various states of operation of the 78Q2131. There are LED pins that indicate when the 78Q2131 is either transmitting LEDTX or receiving LEDRX, one that signals a collision event LEDCOL, L_SPD reflects transmit speed and LEDL indicates the link is up. The LEDPWR pin indicates the power level of the HomePNA port. All LED signals are active low.

General Purpose I/O Interface

The 78Q2131 has a two pin, bi-directional, general purpose interface that can be used for external control or to monitor external signals. The direction of these pins and the data that is either driven or read from these pins is configured via bits MR16.9:6 as detailed in the Vendor Specific Register description in MR16.

Interrupt Pin

The 78Q2131 has an Interrupt pin (INTR) that is asserted whenever any of the sixteen interrupt bits of P1R3 15:0 are set. These interrupt bits can be disabled via MR19.12 Interrupt Enable bits. The Interrupt Level bit, MR16.14, controls the active level of the INTR pin. When the INTR pin is not asserted, the pin is held in a high impedance state.

PIN DESCRIPTION

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
A	Analog Pin	I	Digital Input
O	Digital Output	I/O	Digital Bi-directional Pin
S	Supply	OZ	Tri-stateable digital output

MII (MEDIA INDEPENDENT INTERFACE)/ GPSI (GENERAL PURPOSE SERIAL INTERFACE)

PIN	80-PIN	64-PIN	TYPE	DESCRIPTION
TX_CLK (GPSI & MII)	33	27	OZ	TRANSMIT CLOCK: TX_CLK is a continuous clock which provides a timing reference for the TX_EN, TX_ER and TXD[3:0] signals from the MAC. The clock frequency is bursty. When the GPSI port is selected, this is the transmit clock for the General Purpose Serial Interface. This pin is tri-stated in isolate mode.
TX_EN (GPSI & MII)	34	28	I	TRANSMIT ENABLE: TX_EN is asserted by the MAC to indicate that valid data for transmission is present on the TXD[3:0] pins. This pin is shared for both the GPSI interface and the MII interface.
TXD[3:0] (TXD[0] = TXDAT in GPSI mode)	40-37	32-29	I	TRANSMIT DATA: When the MII port is selected via the MII_EN select pin, TXD[3:0] receives data from the MAC for transmission on a nibble basis. This data is captured on the rising edge of TX_CLK when TX_EN is high. When the GPSI port is selected, TXD[0] is used for the serial transmit data, TXDAT.
TX_ER	32	26	I	RESERVED
CRS (GPSI & MII)	42	34	OZ	CARRIER SENSE: CRS is high whenever a non-idle condition exists on either the transmitter or the receiver. When the GPSI port is selected, this pin becomes the CRS pin of the GPSI. This pin is tri-stated in isolate mode.
COL (CLSN in GPSI mode)	41	33	OZ	COLLISION: When the MII port is selected via the GPSI/MII select pin, COL is asserted high when a collision has been detected on the media.. When the GPSI port is selected, this pin becomes the CLSN pin of the GPSI. This pin is tri-stated in isolate mode.
RX_CLK (GPSI & MII)	30	24	OZ	RECEIVE CLOCK: RX_CLK is a continuous clock which provides a timing reference to the MAC for the RX_DV, RX_ER and RXD[3:0] signals. When the GPSI port is selected, this pin becomes the RX_CLK pin of the GPSI signals. The clock frequency is bursty. This pin is tri-stated in isolate mode.
RX_DV	29	23	OZ	RECEIVE DATA VALID: RX_DV is asserted high to indicate that valid data is present on the RXD[3:0] pins. It transitions high when the start-of-frame delimiter (SFD) is detected. This pin is tri-stated in isolate mode.
RXD[3:0] (RXD[0] = RXDAT in GPSI mode)	23-26	19-22	OZ	RECEIVE DATA: When the MII port is selected via the MII_EN select pin, received data is provided to the MAC via RXD[3:0]. When the GPSI port is selected, RXD[0] is used for the serial received data, RXDAT. This pin is tri-stated in isolate mode.
RX_ER	31	25	OZ	RESERVED

STATION MANAGEMENT INTERFACE (SMI)

PIN	80-PIN	64-PIN	TYPE	DESCRIPTION
MDC	22	18	I	MANAGEMENT DATA CLOCK: MDC is the clock used for transferring data via the MDIO pin.
MDIO	21	17	I/O	MANAGEMENT DATA INPUT/OUTPUT: MDIO is a bi-directional port used to access management registers within the 78Q2131. This pin requires an external pull-up resistor as specified in IEEE-802.3.
PHYAD[4:0]	14-18	12-16	I	PHY ADDRESS: Allows 31 configurable PHY addresses. The 78Q2131 always responds to data transactions via the MII interface when the PHYAD bits are all zero independent of the logic levels of the PHYAD pins.

CONTROL AND STATUS

NAME	80-PIN	64-PIN	TYPE	DESCRIPTION
$\overline{\text{RST}}$	6	4	I	$\overline{\text{RESET}}$: When pulled low the pin resets the chip. There are 3 other ways to reset the chip: i) through the internal power-on-reset (activated when the chip is being powered up) ii) through the MII register bit MR 0.15 iii) upon exiting power-down mode Refer to the Reset Modes section for more details.
PWRDN	7	5	I	POWER-DOWN: The 78Q2131 may be placed in a low power consumption state by setting this signal to logic high. While in power-down state, the 78Q2131 still responds to management transactions. The same power-down state can also be achieved through the PWRDN bit in the MII register MR0.11.
ISO	57	49	I	ISOLATE: When set to logic one, the 78Q2131 will present a high impedance on its MII output pins. This allows for multiple PHYs to be attached to the same MII interface. When the 78Q2131 is isolated, it still responds to management transactions. The same high impedance state can also be achieved through the ISO bit in the MII register MR0.10.

CONTROL AND STATUS (continued)

NAME	80-PIN	64-PIN	TYPE	DESCRIPTION
ISODEF	58	N/A	I	ISOLATE DEFAULT: This pin determines the power-up/reset default of the ISO bit, MR0.10. If it is connected to VDD, ISO bit will have a default value of 1. If it is connected to GND, ISO bit will have a default value of 0.
MII_EN	74	60	I	MII ENABLE: When this pin is high, the MII port mode is selected. When low, the GPSI port is selected.

MDI (MEDIA DEPENDENT INTERFACE)

NAME	80-PIN	64-PIN	TYPE	DESCRIPTION
HLIP, HLIN	68, 67	56, 55	A	RECEIVE POSITIVE/NEGATIVE: Receiver inputs for HomePNA
HLOP, HLON	78, 80	62, 64	A	TRANSMIT POSITIVE/NEGATIVE: Transmitter outputs for HomePNA.

LED INDICATORS

The LED pins use standard logic drivers. They output a logic low when the LED is meant to be on and a logic high when it is meant to be off. The LED should be connected in series with a resistor between the output pin and the power supply.

NAME	80-PIN	64-PIN	TYPE	DESCRIPTION
$\overline{\text{LEDL}}$	53	43	O	LED LINK: ON for link up.
$\overline{\text{LEDTX}}$	50	42	O	LED TRANSMIT: ON when there is a transmission (normally OFF).
$\overline{\text{LEDRX}}$	49	41	O	LED RECEIVE: ON when there is a reception (normally OFF).
$\overline{\text{LEDCOL}}$	48	40	O	LED COLLISION: This is a collision indicator and turns-ON when a collision occurs.
$\overline{\text{LEDPWR}}$	47	39	O	LED POWER: ON when in high power mode and OFF when in low power mode.
L_$\overline{\text{SPD}}$	55	45	O	LED SPEED: ON to indicate high speed mode.

OSCILLATOR/CLOCK

NAME	80-PIN	64-PIN	TYPE	DESCRIPTION
XTLI	9	7	A/I	CRYSTAL INPUT: Should be connected to a 25 MHz crystal. Otherwise, it doubles as the clock input pin and connects to a 25 MHz clock source.
XTLO	10	8	A	CRYSTAL OUTPUT PIN: Should be connected to a 25 MHz crystal. When the clock comes from an external clock module, it is not used.

MISCELLANEOUS PINS

NAME	80-PIN	64-PIN	TYPE	DESCRIPTION
GPIO0	19	N/A	I/O	GENERAL PURPOSE I/O PIN: This is an I/O pin that is configurable as an input or an output via management interface. A value of one in bit MR16.6 configures GPIO0 as an input, and a zero configures it as an output. The logic level of the GPIO0 pin is reflected in MR16.7. This pin has a weak internal pull-down to prevent it from floating when configured as an input (it is configured as an input by default).
GPIO1	20	N/A	I/O	GENERAL PURPOSE I/O PIN: This is an I/O pin, which is configurable as an input or an output via the management interface. A value of one in bit MR16.8 configures GPIO1 as an input, and a zero configures it as an output. The logic level of the GPIO1 pin is reflected in MR16.9. This pin has a weak internal pull-down to prevent it from floating when configured as an input (it is configured as an input by default).
INTR	43	35	OZ	INTERRUPT PIN: This pin is used to signal an interrupt to the media access controller. The pin is held in the high impedance state when an interrupt is not indicated. The pin will be forced high or low to signal an interrupt depending upon the value of the INTR_LEVEL bit (MR16.14). The events that trigger an interrupt can be programmed via the Interrupt Control Register located at address MR17 and P1R3 for HomeLAN.

POWER SUPPLY

NAME	80-PIN	64-PIN	TYPE	DESCRIPTION
V_{CC}	8,13, 27,36, 45,51, 60, 79	6,11, 37,48, 63	S	SUPPLY VOLTAGE: Two supply ranges are supported: 5V ± 0.5V, or 3.3V ± 0.3V.
GND	4,11, 12,28, 35,44, 46,52, 59,77	2,9,10, 36,38, 47,61	S	GROUND

REFERENCE PIN

NAME	80-PIN	64-PIN	TYPE	DESCRIPTION
RIBB	70	58	A	BIAS CURRENT SETTING RESISTOR: To be tied to an external resistor that is also connected to the RIBB_RET pin. This resistor should be placed as close as possible to the package pin. A recommended value of 9.76 KΩ ± 1% is provided for reference purposes only.
RIBB_RET	69	57	A	BIAS CURRENT SETTING RESISTOR RETURN PIN: To be connected to external RIBB resistor.
VBG	71	59	A	V BANDGAP BYPASS: Pin for tying bypass cap ~ 0.1uF.

REGISTER DESCRIPTION

The 78Q2131 implements twenty user accessible 16-bit registers which are accessible through the Station Management Interface on the MDIO and MDC pins. The supported registers are shown below. Unsupported registers will be read as all zeros. All of the registers respond to the broadcast address, PHYAD value 00000. The register map is implemented in two pages, with page 0 being the power-up reset default. Page 0 implements the standard 802.3 MII registers along with the vendor specific register set. The vendor specific registers 16, 17, 18, 19 are mapped into both pages for convenience and to implement the page selection via bit MR19.0. Page 1 contains the HomePNA specific registers. The MII management 16-bit register set implemented in the 78Q2131 is as follows:

ADDRESS	Page	SYMBOL	NAME	RESET VALUE (HEX)
0	0	MR0	Control	(0000)
1	0	MR1	Status	(1801)
2	0	MR2	PHY Identifier 1	000E
3	0	MR3	PHY Identifier 2	7121
4	0	MR4	Auto-Negotiation Advertisement	(0061)
5	0	MR5	Auto-Negotiation Link Partner Ability	0000
6	0	MR6	Auto-Negotiation Expansion	0000
7	0	MR7	(Not implemented, read as zero)	0000
8-15	0	MR8-15	(Reserved, read as zero)	0000
16	both	MR16	Vendor Specific	(0140)
17	both	MR17	Interrupt Control/Status Register	0000
18	both	MR18	Diagnostic Register	(0000)
19	both	MR19	HomePNA Register	0000
0	1	P1R0	HomePNA Control	4004
1	1	P1R1	HomePNA Status	0000
2	1	P1R2	HomePNA IMASK	0000
3	1	P1R3	HomePNA ISTAT	0000
4,5	1	P1R4,5	HomePNA TX_PCOM	00000000
6,7	1	P1R6,7	HomePNA RX_PCOM	00000000

Note: MR 3.3:0 contains revision specific data.

In above table, the (xxxx) denotes that some of the bit values are determined by pin settings, and so, the default may be a bit different.

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
R	Read-able by management	W	Write-able by management
RC	Cleared on a read operation	SC	Self clearing, write-able
0/1	Default value upon power-up or reset	(0/1)	Default value dependent on pin setting. The value in brackets indicates typical case.

REGISTER DESCRIPTION (continued)

MR0 - CONTROL REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
0.15	RESET	R, W, 0, SC	RESET: Setting this bit to logic one resets the entire 78Q2131. This bit is self clearing.
0.14	LOOPBK	R, W, 0	LOOPBACK: When this bit is set, no transmission of data on the network medium occurs and any receive data on the network medium is ignored. The internal loopback signal path encompasses the 78Q2131 digital core and most of the analog circuitry.
0.13:12	RSVD	R, 0	Reserved for Other Technologies
0.11	PWRDN	R, W, 0	POWER-DOWN: The 78Q2131 may be placed in a low power consumption state by setting this bit to logic one. While in power-down state, the 78Q2131 still responds to management transactions. The power-down state can also be achieved by setting PWRDN pin high.
0.10	ISO	R, W, (0)	ISOLATE: When set, the 78Q2131 will present a high impedance on its MII output pins. This allows for multiple PHYs to be attached to the same MII interface. When the 78Q2131 is isolated, it stills responds to management transactions. The same high impedance state can be achieved through the ISO pin.
0.9:0	RSVD	R, 0	Reserved for Other Technologies

MR1 - STATUS REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
1.15:3	RSVD	R, 0	Reserved for Other Technologies
1.2	LINK	R, 0	LINK STATUS is always logic one if MR19.11 is equal to logic zero. This reflects that the device will be put into HomePNA v1.0 mode. If MR19.11 is a logic 1, then LINK STATUS will reflect the link integrity of the link defined in HomePNA v1.1LINK STATUS: A logic one indicates that a valid link has been established. If the link status should transition from an OK status to a NOT-OK status, this bit will become cleared and remain cleared until it is read.
1.1	JAB	R, 0, RC	Reserved
1.0	EXTD	R, 1	EXTENDED CAPABILITY: This bit is permanently set to logic one to indicate that the 78Q2131 provides an extended register set (MR2 and beyond).

MR2, 3 - PHY IDENTIFIER REGISTER

2.15:0	OUI	R, 000Eh	ORGANIZATIONALLY UNIQUE IDENTIFIER: This value is 00-C0-39 for TDK Semiconductor Corporation. This translates to a value of 000Eh for this register.
3.15:10	OUI	R, 011100	ORGANIZATIONALLY UNIQUE IDENTIFIER: Remaining 6 bits of the OUI.
3.9:4	MN	R, 010010	MODEL NUMBER: The last 2 digits of the model number 78Q2131 is encoded into the 6 bits. (32d-20d=12h)
3.3:0	RN	R,0001	REVISION NUMBER: For example, a value of 0010 corresponds to the second version of the silicon.

REGISTER DESCRIPTION (continued)

MR4,5,6 - AUTO-NEGOTIATION REGISTERS - RESERVED FOR OTHER TECHNOLOGIES

MR16 - VENDOR SPECIFIC REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
16.15	RSVD	R, 0	Reserved
16.14	INT LEVEL	R, W, 0	When this bit is a zero, the INTR pin is forced low to signal an interrupt. Setting this bit causes the INTR pin to be forced high to signal an interrupt.
16.13:11	RSVD	R, 0	Reserved
16.10	NATURAL LOOPBACK	R, W, (0)	The default is 1 and the transmit symbol NT_SYM is looped back into the receive symbol RD_SYM.
16.9	GPIO1_DAT	R, W, 0	GENERAL PURPOSE I/O 1 DATA BIT: When the GPIO_DIR is set, this bit reflects the value of the GPIO1 pin. When the GPIO1_DIR is reset, the value of this bit is driven onto the GPIO1 pin.
16.8	GPIO1_DIR	R, W, 1	GENERAL PURPOSE I/O 1 DIRECTION BIT: Setting this bit configures the GPIO1 pin as an input. Resetting configures GPOI_1 as an output.
16.7	GPIO0_DAT	R, W, 0	GENERAL PURPOSE I/O 0 DATA BIT: When the GPIO0_DIR is set, this bit reflects the value of the GPIO0 pin. When the GPIO0_DIR is reset, the value of this bit is driven onto the GPIO0 pin.
16.6	GPIO0_DIR	R, W, 1	GENERAL PURPOSE I/O 0 DIRECTION BIT: Setting this bit configures the GPIO0 pin as an input. Resetting it configures GPIO0 as an output.
16.5:2	RSVD	R, 0	Reserved
16.1	MII_EN	R,W,0	MII ENABLE: When this bit is high, the MII port mode is selected. When low, the GPSI port mode is selected.
16.0	RSVD	R, 0	Reserved

MR17 - INTERRUPT CONTROL/STATUS REGISTER - RESERVED FOR OTHER TECHNOLOGIES

MR18 - DIAGNOSTIC REGISTER - RESERVED FOR OTHER TECHNOLOGIES

MR19 – HOMEPNA REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
19.15	RSVD		Reserved
19.14	HPNAEN	R,1	Reserved; must be one
19.13	RSVD	R,W,0	Reserved
19.12	HLAN IE	R, W, 0	HOMEPNA INTERRUPT ENABLE. Master enable for HomePNA generated interrupts. Works with HomePNA Interrupt registers on page 1.
19.11	HOMEVER	R,0	HOMEPNA VERSION: Implements the HomePNA functionality of v1.1 when a 1. 0 = HomePNA v 1.0 1 = HomePNA v1.1

REGISTER DESCRIPTION (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
19.10:1	RSVD	R, 0	Reserved; must be zero.
19.0	PAGE Select	R,W,0	PAGE SELECT: Selects the page of MII registers to be addressed and thus read and/or written. The default, 0, selects the normal MII registers. When 1, the HomePNA and internal registers are accessible. Registers 16, 17, 18, 19 are available (mapped) in both pages.

The HomePNA registers are mapped onto page 1 of the MII register set. They are accessible by setting MR19.0 to a one.

P1R0-14 - Programmable Register Map, PAGE 1

REGISTER	SYMBOL	TYPE	DESCRIPTION	Default
0	CONTROL	R/W	The CONTROL register provides a common location for controlling the general operation of the PHY. This register is composed of the following bit fields: bit 0 = (reserved) bit 1 = high power bit 2 = high speed bit 4,3 = (reserved) bit 5 = stop SLICE_LVL adaptation bit 6 = clear the NSE_EVENTS register bit 7 = stop AID address negotiation bit 8 = Cmd high speed bit 9 = Cmd low speed bit 10 = Cmd high power bit 11 = Cmd low power bit 12-14 = (reserved) bit 15 = ignore remote commands	0x4004
1	STATUS	R/W	The STATUS register provides information regarding the global aspects of the operation of the PHY. This register is composed of the following bit fields: bit 0-3 = (reserved) bit 4 = RxVERSION bit 5 = RxSPEED (1=high speed) bit 6 = RxPOWER (1=high power) bit 7-11 = (reserved) bit 12 = invert RXCLK bit 13 = invert TXCLK bit 14 = invert CLSN bit 15 = invert CRS	0x0000

REGISTER DESCRIPTION (continued)

REGISTER	SYMBOL	TYPE	DESCRIPTION	Default
2	IMASK (IMR)	R/W	The interrupt mask register determines which interrupt sources may activate the INTR function. When low, the interrupt is off. The various interrupt sources are mapped into this register (as well as the ISTAT register) as follows: bit 0 = Remote Cmd Done (sent) bit 1 = Remote Cmd Valid (received) bit 2 = Packet Transmitted bit 3 = Packet Received bit 4 = Home Link Status Change bit 8 = TxPCOM Ready bit 9 = RxPCOM Valid bit 10-15 = software interrupts	0x0000
3	ISTAT (ISR)	R/W	The interrupt status register reports the state of each interrupt source, regardless of the state of the IMASK register. The interrupt sources are mapped into this register in an identical manner as the IMASK register. Furthermore, any bit may be written and so facilitate software-stimulated interrupt testing. The appropriate bits in this register must be cleared for the INTN signal to be cleared.	0x0000
4, 5	TX_PCOM	R/W	The 32-bit transmitted data field to be used for out-of-band communication between PHY management entities. No protocol for out-of-band management has been defined. Accessing the low word causes the PHY to send all-0 PCOM's until the high byte has been accessed. Once accessed, the next transmitted packet will cause this register's contents to be shifted out in the PCOM field of the transmitted packet. Upon transmission, this register will read back as all-0's. A non-null transmitted PCOM will set the TxPCOM Ready bit in the ISTAT register. An access to any of the two TxPCOM words will clear the TxPCOM Ready bit in the ISTAT register.	ALL 0's
6, 7	RX_PCOM	R/O	The 32-bit received data field to be used for out-of-band communication between PHY management entities. No protocol for out-of-band management has been defined. Accessing the low word of the register is sufficient to ensure that subsequently received packets will not over-write the register contents. A non-null received PCOM will set the RxPCOM Valid bit of the ISTAT. Accessing the high word of the register clears this bit and allows over-writing of the register by subsequent received packets.	ALL 0's

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum rating may permanently damage the device.

PARAMETER	RATING
DC Supply Voltage	7 VDC
Storage Temperature	-65 to 150°C
Pin Voltage	-0.3 to (Vcc+0.3) VDC
Pin Current	± 100 mA

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges:

PARAMETER	RATING
DC Voltage Supply, Vcc	3.3 V ± 0.3V, 5 V ± 0.5V VDC
Ambient Operating Temperature, Ta	0 - 70°C

DC CHARATERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	I_{CC}	V_{CC} = 3.3V; Idle Peak		70	 90 110	mA
Supply Current	I_{CC}	V_{CC} = 5.0V; Idle Peak		75	 100 120	mA
Supply Current	I_{CC}	Powerdown mode, oscillator disabled		5	20	µA

DIGITAL INPUT CHARACTERISTICS

Pins of type I, I/O

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
TTL Input Voltage Low	V_{IL}				0.8	V
TTL Input Voltage High	V_{IH}		2.0			V
TTL Input Current, excluding pins with external pulls	I_{IL}, I_{IH}	V_{CC} = 5.5V	-10		+10	µA
TTL Input Current, on pins with internal pulls		V_{CC} = 5.5V, V_{in}, or 0V, as appropriate	-90		+90	µA
Input Capacitance	C_{IN}			10		pF

ELECTRICAL SPECIFICATIONS (continued)

DIGITAL OUTPUT CHARACTERISTICS

Pins of type O, OZ

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage High	V_{OH}	$4.5V \le V_{CC} \le 5.5V$ I_{OH} = 4.0mA	V_{CC}-0.6			V
Output Voltage Low	V_{OL}	$4.5V \le V_{CC} \le 5.5V$ I_{OL} = 4.0mA			0.4	V
Output Transition Time Between V_{OL} and V_{OH}	T_t	$4.5V \le V_{CC} \le 5.5V$ I_{OH}, I_{OL} = 4.0mA		5		ns
Output Voltage High	V_{OH}	$3.0V \le V_{CC} \le 3.6V$ I_{OH} = 2.0mA	V_{CC}-0.4			V
Output Voltage Low	V_{OL}	$3.0V \le V_{CC} \le 3.6V$ I_{OL} = 2.0mA			0.4	V
Output Transition Time Between V_{OL} and V_{OH}	T_t	$3.0V \le V_{CC} \le 3.6V$ I_{OH}, I_{OL} = 2.0mA		5		ns

ELECTRICAL SPECIFICATIONS (continued)

DIGITAL TIMING CHARACTERISTICS

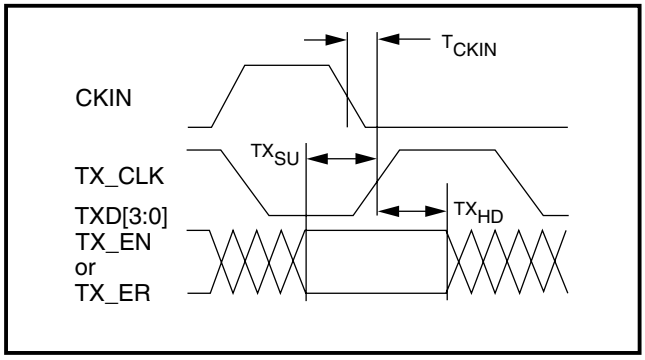


FIGURE 1: Transmit Inputs to the 78Q2131

MII Transmit Interface

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX_{SU}		15			ns
Hold Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX_{HD}		0			ns
CKIN-to-TX_CLK Delay	T_{CKIN}		0		10	ns
TX_CLK Duty-Cycle			40		60	%

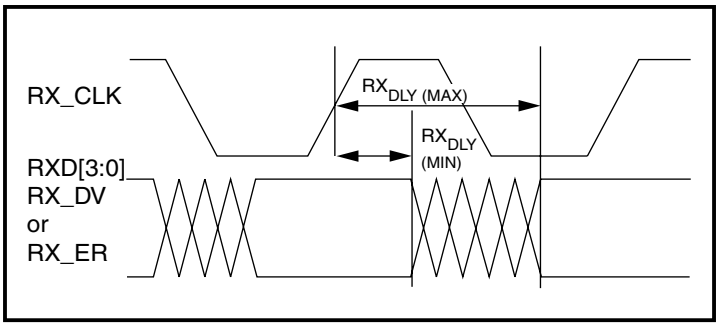


FIGURE 2: Receive Outputs from the 78Q2131

MII Receive Interface

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Receive Output Delay: RX_CLK to RXD[3:0], RX_DV, RX_ER	RX_{DLY}	Data must change at least 10ns before the next rising edge of RXCLK			50	ns
RX_CLK Duty-Cycle			40		60	%

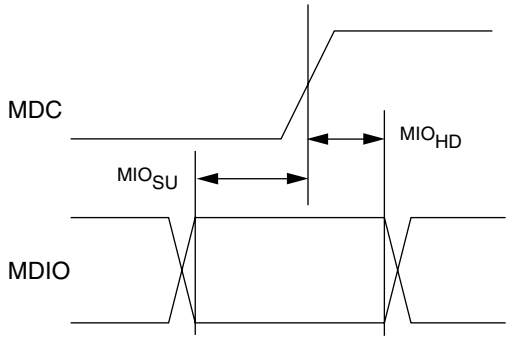


FIGURE 3: MDIO as an Input to the 78Q2131

MDIO Interface Input Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: MDC to MDIO	MIO_{SU}		10			ns
Hold Time: MDC to MDIO	MIO_{HD}		10			ns
Max Frequency: MDC	F_{max}				25	MHz

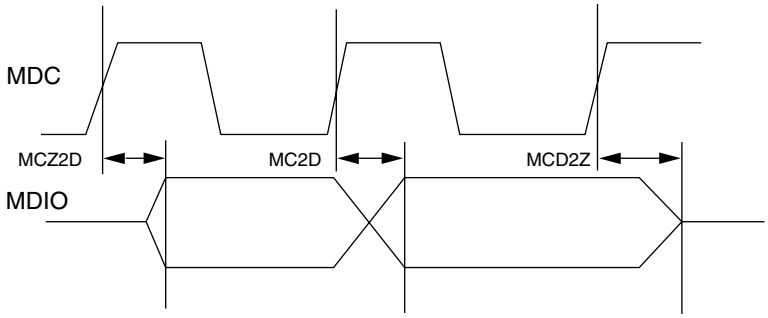
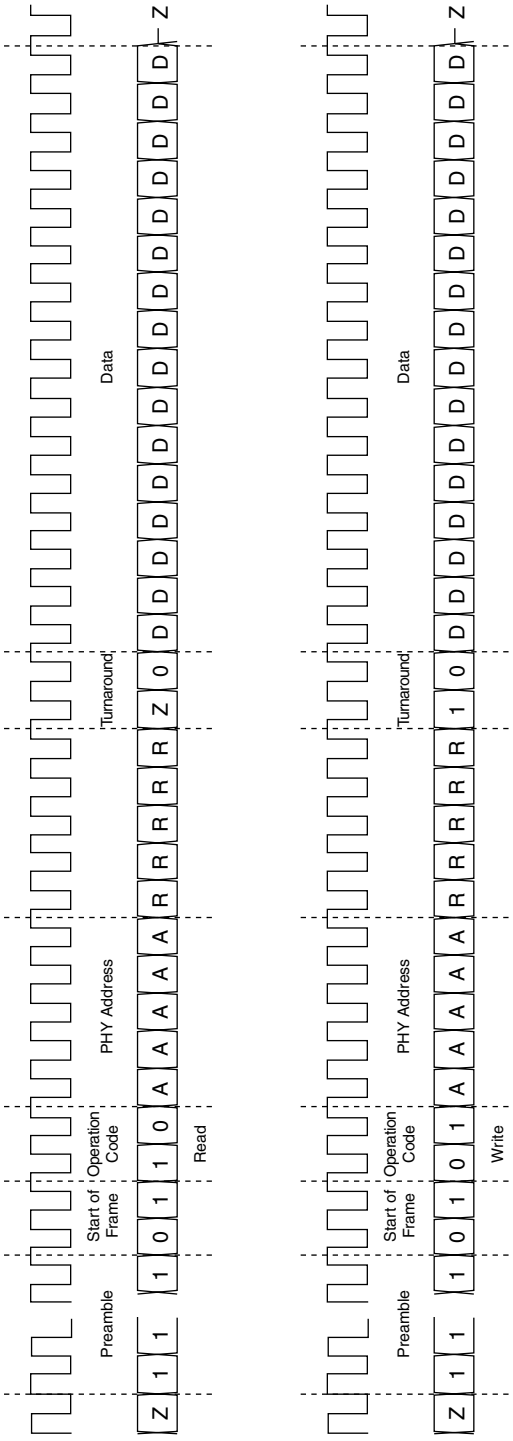


FIGURE 4: MDIO as an Output from the 78Q2131

MDIO Interface Output Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
MDC to MDIO data delay	MC2D				30	ns
MDIO output from high Z to driven after MDC	MCZ2D				30	ns
MDIO output from driven to high Z after MDC	MCD2Z				30	ns

FIGURE 5: MDIO Interface Output Timing



ELECTRICAL SPECIFICATIONS (continued)

HomePNA System Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TX_EN (MII) to TD Delay				6	BT
RD to RXDat (MII) Delay				6	BT
COL Assert Delay				9	BT
COL De-assert Delay				9	BT
CRS Assert Delay				6	BT
CRS De-assert Delay				6	BT

ANALOG ELECTRICAL CHARACTERISTICS

HomePNA Transmitter

The normalized transmitter output waveform is shown in Figure 6 – HomePNA Transmit Pulse Shape and must be measured directly at the transmitter terminated with 100 ohms. The waveform is bounded by the values of TX_PEAK_V ±15%. The waveform has been normalized to the peak value of the envelope TX_PEAK_V, which is specified in the transmit levels table for both HIGH and LOW power level options.

The maximum values of the waveform after 1 usec from when it first crosses the 5 mV threshold does not exceed the mask of Figure 7 – HomePNA Transmit mask for times greater than 1usec.

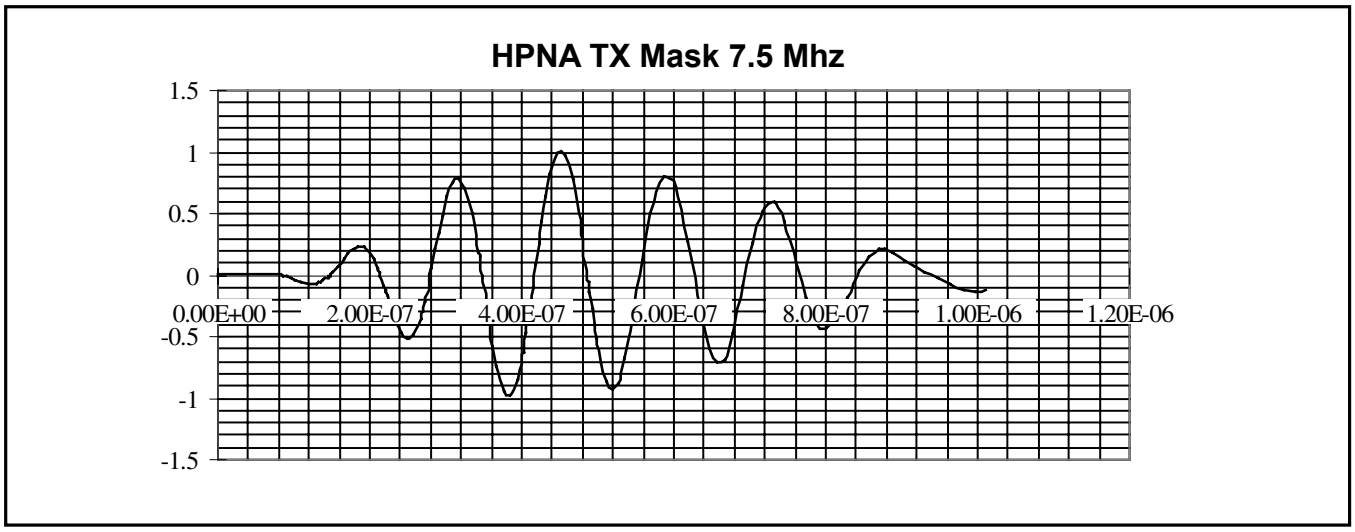


Figure 6 – HomePNA Transmit Pulse Shape

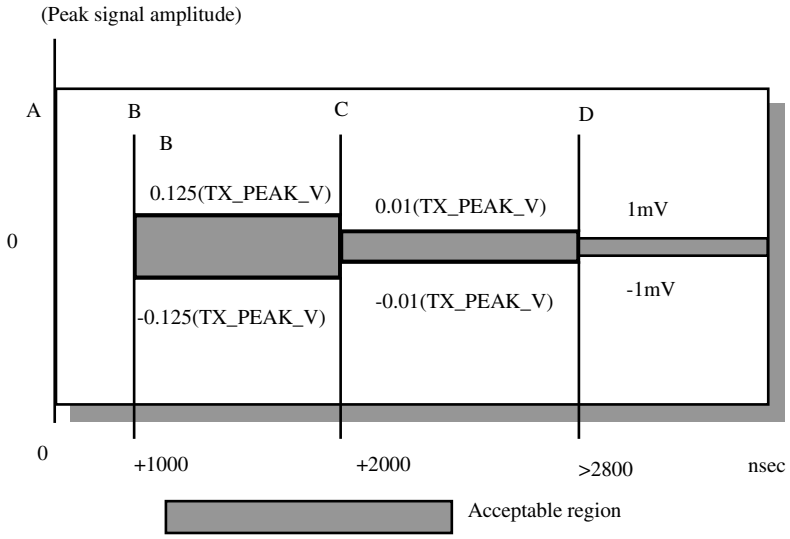


Figure 7 – HomePNA Transmit mask for times greater than 1usec

ELECTRICAL SPECIFICATIONS (continued)

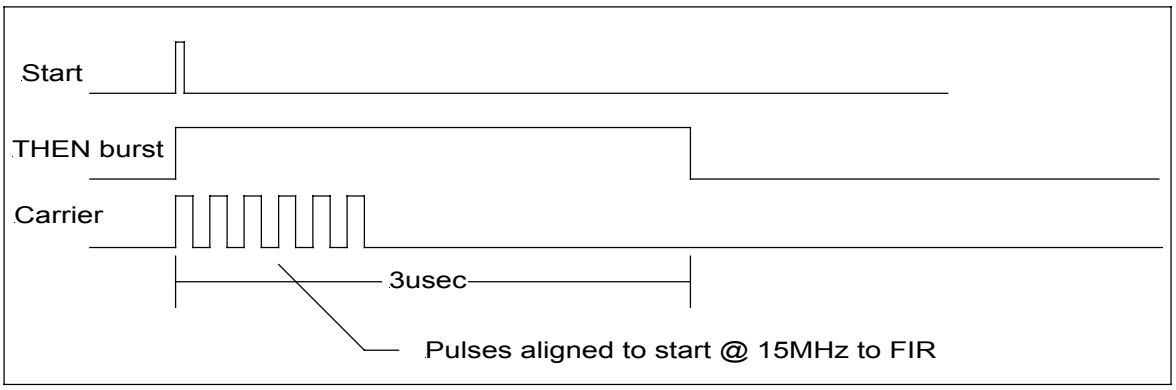


Figure 8 – HomeLAN Transmit Burst Detail

The output power spectrum meets the spectral mask of Figure 9 – HomePNA PSD Mask with a termination of 100 ohms and back-to-back Ethernet packets of 1518 bytes length with random data. The resolution bandwidth shall be 100 kHz. The specified PSD levels include thermal noise. The power level requirements below 1.1 MHz allow 1M8 PHY stations to interoperate with G.dmt and G.lite modems.

Two power operating modes are defined, LOW_POWER and HIGH_POWER. The maximum Power Spectral Density (PSD) levels for the modes are defined in Figure 9 – HomePNA PSD Mask. For applications interfacing to the PSTN, the power levels of FCC Part 68 shall not be exceeded.

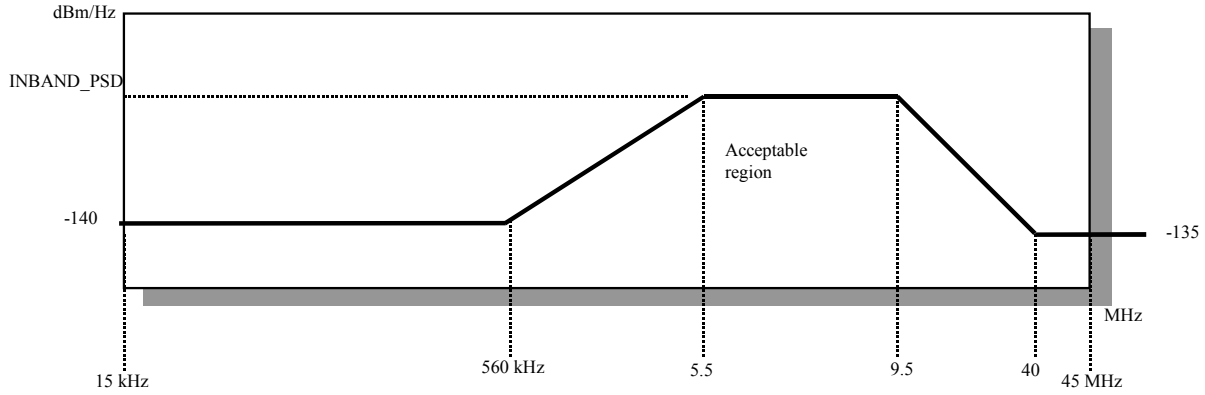


Figure 9 – HomePNA PSD Mask

Power Mode	Max INBAND_ PSD (dBm/Hz)	Min attenuation at > +/- 3.5 MHz from carrier	MAX PSD below 560 kHz dBm/Hz	MAX PSD below 1.2 MHz dBm/Hz	MAX PSD above 40 MHz dBm/Hz
LOW_POWER	-62	30 dB	-140	-135	-135
HIGH_POWER	-56	30 dB	-140	-135	-135

Table 1 – HomePNA Power Spectral Levels

HomePNA Transmitter

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Transmit Level – High Power TX_PEAK_V	At line output of HomePNA device with 100ohm load connected	1	1.2	1.4	Vpk
Transmit Level – Low Power TX_PEAK_V	same	0.5	0.6	0.7	Vpk
Out-of-Band Level @ 1.2Mhz	Nom transmit signal	-80			dB

HomePNA Receiver

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Dynamic Range for 0.01% PER	20mV necessary for PER measurements	20m		1.2	Vp diff
Collision Domain	Repeaters cannot be used			500	ft
Signal/Noise		100			mV

Impulse Noise Performance

Receiver Signal level (mV peak) ± 10%	Impulse Noise level (mV peak) ± 10%	Packet Error Rate (PER)
20 to 1200	5	0.1 %
100 to 200	20	1 %
200 to 1200	20	0.1 %

Gaussian Noise Performance

Receiver Signal level (mV peak ± 10 %)	Gaussian Noise level (mV peak ± 10 %)	Packet Error Rate (PER)
20 to 1200	5	0.01%
100 to 1200	20	0.5%

REFERENCE CRYSTAL

If the internal crystal oscillator is to be used, a crystal with the following characteristics should be chosen:

NAME	VALUE	UNITS
Frequency	25.00000	MHz
Load Capacitance	15	pF
Frequency Tolerance	±50	PPM
Aging	±2	PPM/yr
Temperature Stability (0 – 70°C)	±5	PPM
Oscillation Mode	Parallel Resonance, Fundamental Mode	
Parameters at 25°C ± 2°C ; Drive Level = 0.5 mW		
Shunt Capacitance (max)	8	pF
Motional Capacitance (min)	10	fF
Series Resistance (max)	25	Ω
Spurious Response (max)	> 5 dB below main within 500 kHz	

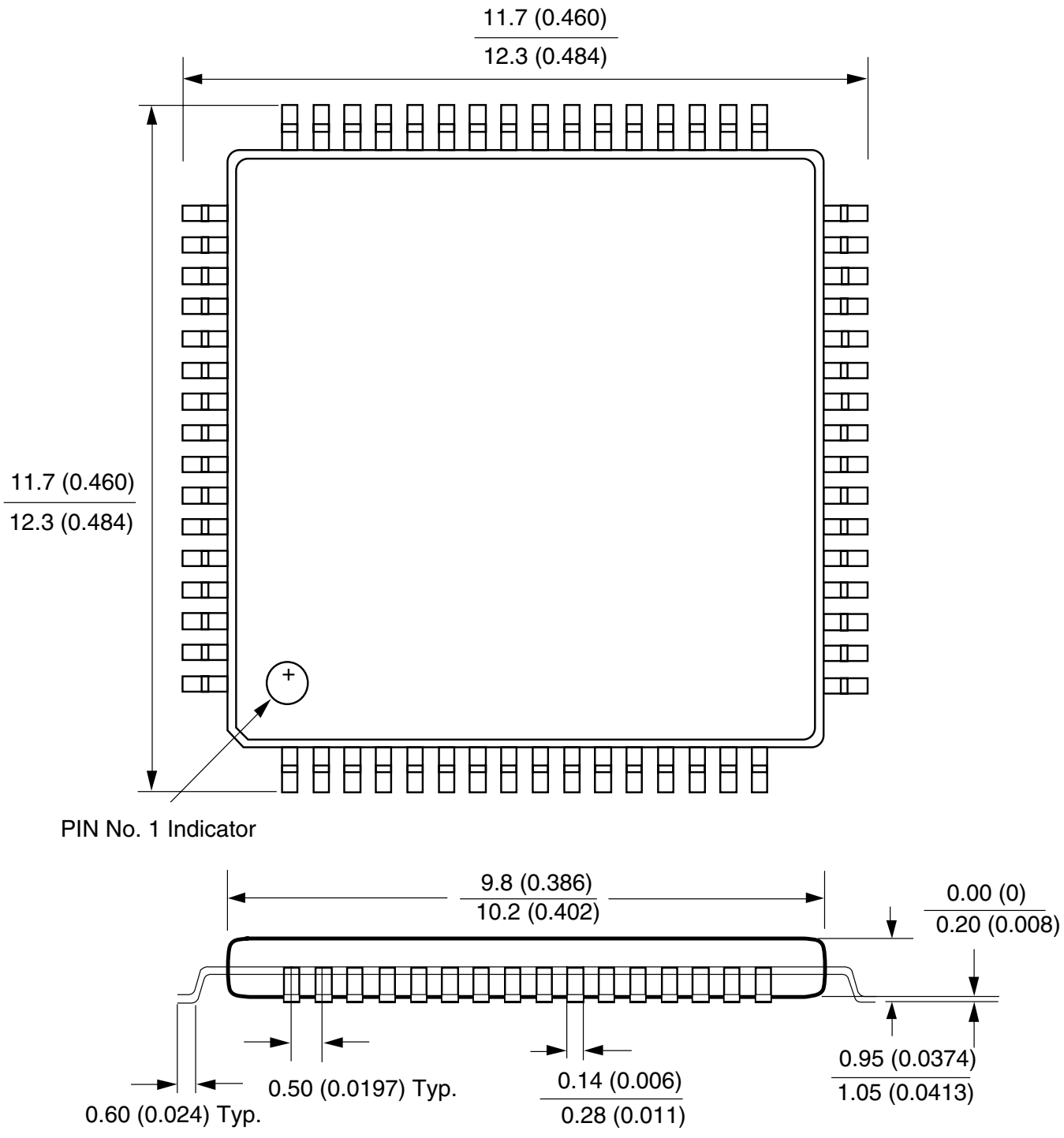
ELECTRICAL SPECIFICATIONS (continued)

HomePNA ISOLATION TRANSFORMER

A simple 1:1 isolation transformer with integrated series capacitor in the primary is required at the line interface, but transformers with integrated common-mode choke are recommended for exceeding FCC requirements. This table gives the recommended line transformer characteristics:

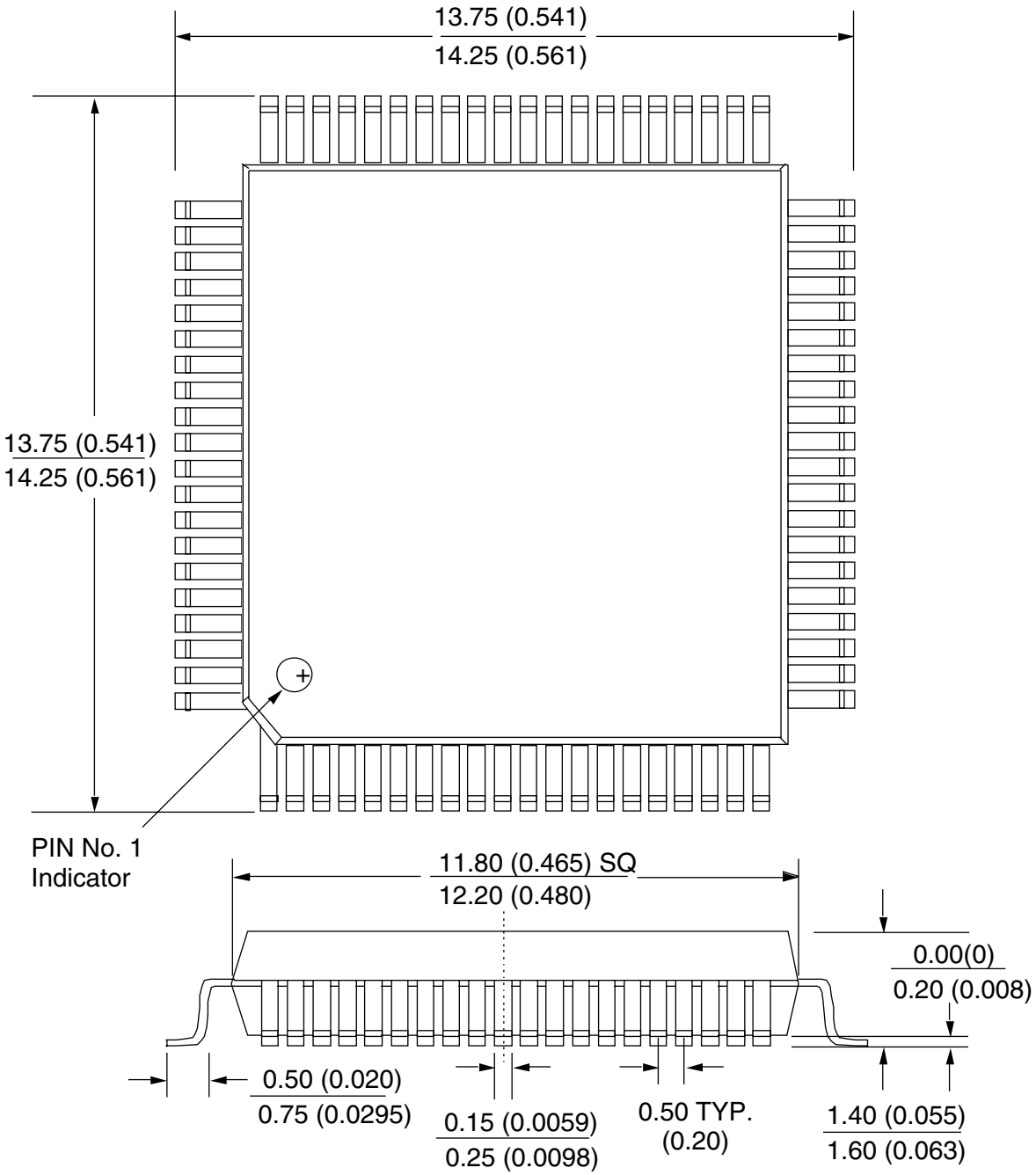
NAME	VALUE	CONDITION
Turns Ratio	1 CT : 1 CT ± 5%	
Open-Circuit Inductance	140 uH (min)	@ 100 mVRMS, 100 KHz
Leakage Inductance	2.0 uH (max)	@ 1 MHz (min)
Inter-Winding Capacitance	6 pF (max)	
D.C. Resistance	0.25 Ω (max)	
Insertion Loss	-1.1 dB (typ)	0 – 27 MHz
HIPOT	2000 Vrms	
Series C at line side	0.001uF @ 2000v	

MECHANICAL DRAWINGS



64-Lead Very Thin Quad Flatpack

MECHANICAL DRAWINGS (continued)



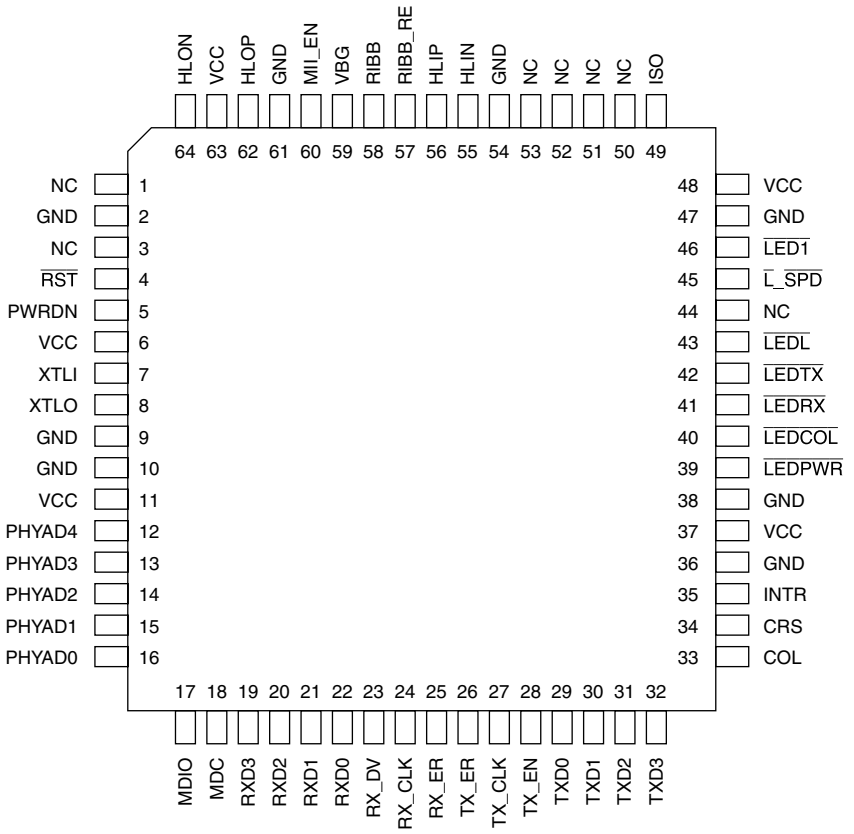
80-Lead Thin Quad Flatpack

Note: Controlling dimensions are in mm

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component

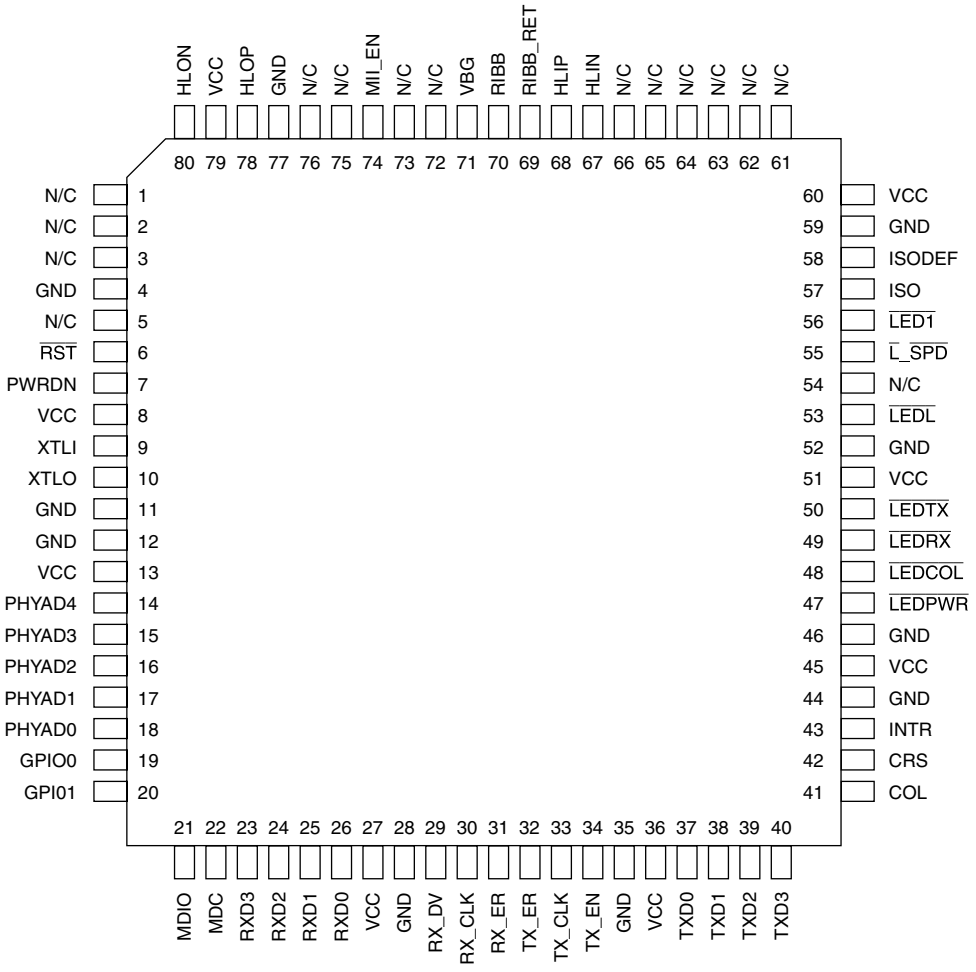


64-Lead Thin Quad Flatpack
78Q2131

PACKAGE PIN DESIGNATIONS (continued)

CAUTION: Use handling procedures necessary for a static sensitive component

(Top View)



80-Lead TQFP

78Q2131

Target Specification: The Target Specification is intended as a proprietary initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. TDK Semiconductor assumes no obligation regarding future manufacture unless agreed to in writing.

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