TDK SEMICONDUCTOR CORP.

78P2241 28-PIN PLCC Demo Board

APPLICATION NOTE

July 2000

INTRODUCTION

TDK Semiconductor Corporation has introduced a new transceiver for DS3/E3/STS1 applications called the 78P2241. This application note will explain the design of the demo board using a 78P2241 PLCC package.

78P2241 is available in both 28-pin PLCC and 48 pin TQFP packages. The information about the demo board for the 48 pin TQFP package is available in another Application Note titled “Demo Board Manual 2241 TQFP.

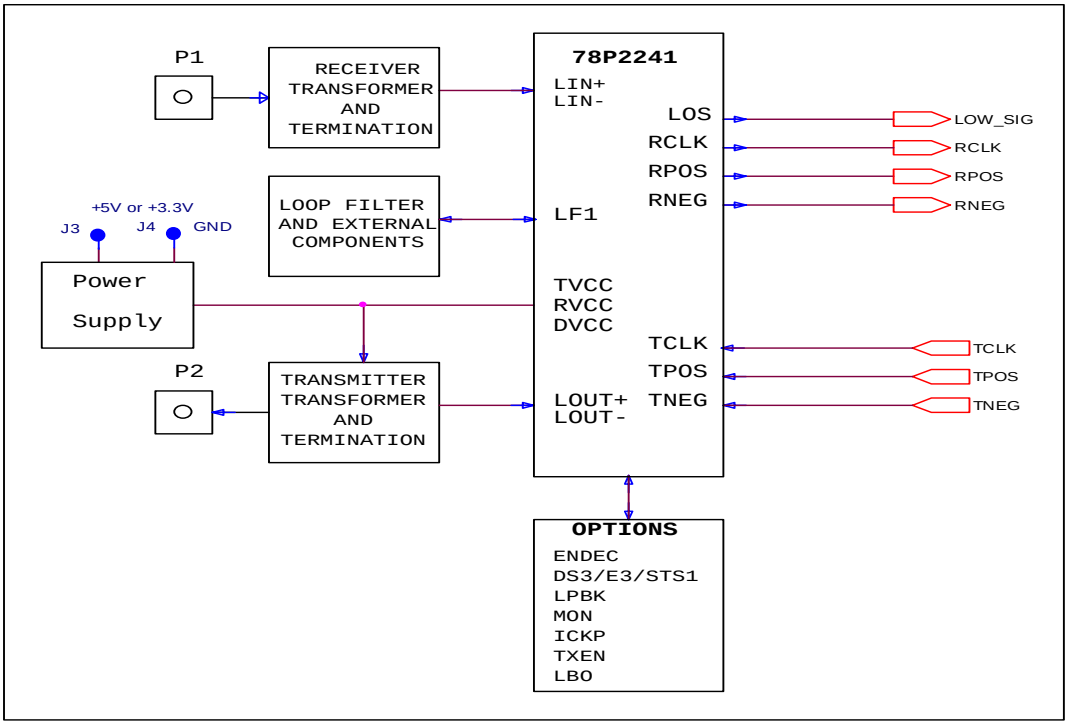
DESCRIPTION

The 78P2241-demo board is designed to facilitate the evaluation of the 78P2241 single chip DS3/E3/STS-1 transceiver IC. The demo board includes all of the necessary discrete components for the interface to a coded AMI line.
On-board jumpers control the option pins of the IC including the loop-back functions

FEATURES

- Allows easy evaluation of the 78P2241
- Includes all necessary external components
- Includes jumpers to control options
- Operates at DS3, E3 or STS-1 by changing proper jumpers
- Uses either the receive clock or an external clock for the transmit clock
- The demo board can operate with either a 5V or 3.3V supply
- 4 layer PC board construction

Block Diagram



POWER SUPPLY CONNECTION

The demo board is constructed as a four-layer PC board. The outer two planes carry the signals. The internal two layers are the ground and power supply planes. The power supply pins of the 78P2241are connected directly to the supply planes (see layout files Figures: 18 to 22).

RECEIVE SIGNAL PATH

The AMI input signal is connected to the BNC connector at P1. The maximum recommended distance of the demo board to a DSX3 cross-connect or test equipment is 450 feet. The IC recovers clock, positive and negative data from the AMI signal, and can handle added resistive attenuation. Table 1 shows the available receiver logic signals on the test points:

SIGNAL
LOSN U1-27
RPOS U1-25
RNEG U1-24
RCLK U1-23

Table 1. Receive Signals

The AMI input signal should be properly coded to prevent a long run of zero on the line. The proper code will limit the number of zeros to two or three depending on the speed. Table 2 shows the proper coding required by rate:

78P2241 RATE	SPEED Mbit/s	MAX zeros	CODE NAME
DS3	44.736	2	B3ZS
STS-1	51.840	2	B3ZS
E3	34.386	3	HDB3

Table 2. Coding names and rates

The 78P2241 has an option that will enable or disable the Encoder/Decoder, if the application does not required coding/decoding then the pin 20 (ENDEC) should be pulled high. If coding/decoding is required then pin 20 should be tied low and the 78P2241 will implement the proper codes as show in the table 2 above.

The AMI input signal to the IC can be monitored using a high impedance FET probe such as TEKTRONIX P4064 or HP 1141A.

The input signal is coupled through a 1:1 wide-band transformer. See Table 4 for a list of recommended transformers vendors.

The operation speed of the 78P2241, is controlled by changing the value of the resistor tied to RFO pin, pin 5. Table 6 shows the required external resistor (R8, R9 or R10) for the different speeds.

TRANSMIT SIGNAL PATH

The 78P2241 accept CMOS level logical inputs (TCLK, TPOS and TNEG) and converts them to the proper AMI signals. With pin 20 (ENDEC) low the 78P2241 will code the output signal in either HDB3 or B3ZS depending on the polarity of pin 13 (E3).

The following shows the test points used for the transmitter.

SIGNAL
TCLK U1-16
TNEG U1-15
TPOS U1-14

Table 3. Transmitter signals.

The output pins of the 78P2241, LOUT+ and LOUT- are connected to a 1:2CT wide-band transformer. See Table 4 for recommended transformers.

MANUFACTURER	PART NUMBER	PART NUMBER	COMMENTS
Reference	T1, Receiver	T2, Transmitter	
TDK	WBTT3.6-0340E	WBTT3.6-0401	Surface mount
PULSE	PE-65966	PE-65969	Through Hole
PULSE	PE-65967	PE-65968	Surface mount
PULSE	PE-68629	PE-68630	TH 3KV Isolation
PULSE	T3001	T3002	SMT Ext. Temp.
HALO	TD01-0406NE	TD07-0206NE	Through Hole
HALO	TG01-0406NS	TG07-0206NS	Surface mount
HALO	TD01-0456NE	TD07-0356NE	DIP Ext. Temp.
HALO	TG01-0456NS	TG07-0356NS	SMT Ext. Temp.

Table 4. Recommended Transformers and vendors

The transmitter transformer center tap is connected to the positive supply. The objective is to meet a pulse template at any cable length up to the maximum of 450 feet. The generated AMI signal is available on the BNC connector, P2, and it can be monitored using a high impedance probe, or via a 75 Ohm to 50 Ohm adapter (see Figure 3).

OPTION PINS CONTROL

ENDEC pin 20. This pin selects the B3ZS/HDB3 encoder, if low then the encoder is selected and only RPOS, TPOS will be active, RNEG is low, and TNEG is ignored. If pin 20 is high then the encoder is disabled and RPOS, RNEG, TPOS and TNEG will be active.
E3 pin 13. This pin selects the mode the 78P2241 will operate in; three possible modes are selectable DS3 (high), E3 (low) or STS-1 (floating). This pin selects the HDB3/B3ZS coder/decoder, if pin 13 is high or floating, B3ZS will be used, if pin 13 is low, HDB3 code will be used.
TXEN pin 18. This input enables the transmitter drivers. When high, the part is in normal operation. When low, the outputs LOUT+ and LOUT- are in high impedance state, this feature is used connect two transmitters together and to save power when the drivers are not used.
MON pin 21. When enabled (high state) 78P2241 will add 20dB flat gain in the input path. This feature is used when flat attenuation is added to the system or for monitoring purposes.
ICKP pin 10. When this input is low, the data are presented at the output at the high to low transition of the clock, and the data are sampled at the input at the low to high transition of the clock. If pin 10 is high then transmit clock is inverted. If the pin 10 is floating then both received and transmit clocks are inverted.
LPBK pin 28. This input controls the two loop-backs. When pin 28 is high then no loop-back is selected. Remote loop-back is selected when pin 28 is floating, this loops the receive data and receive clock pins to transmit data and clock inputs, receive data and clock are still present at the logic outputs. Local loop-back is selected when pin 28 is low then the LOUT+ and LOUT- are connected to LIN+ and LIN- such that the data present at the logic transmit inputs will be reflected at the receive logic outputs.
LBO pin 12. This input controls the amplitude of the output signal in DS3 and STS-1 mode. If the cable length is less than 225 feet this pin need to be high or floating. For all cable lengths higher than 225 feet this input should be low.
To ensure that the 78P2241 recognizes a float condition, the input should sink less than 10 microampere. Consider that the input impedance of the input pin is between 15 and 20KOhm and the float voltage is 1.5V with a tolerance of 20%.

BOARD LAYOUT CONSIDERATIONS

Most applications will use multi layer board therefore the demo board is constructed with four layers PC board as a system implementation example. The two outer layers are reserved for signal traces and the two inner layers carriy the power supply. A possible layout approach is to use two different grounds for noise immunity. The two grounds are the component ground and the Chassis ground. The component ground should be a plane that directly connects to the negative supply pin, this ground plane will carry all the return currents of all board logic and it is wiser to cut the analog portion of the circuitry out of the plane. The analog ground could be part of the ground plane but cut as an island such that return current would not flow under pins 1,2,3,4 , 5 and 6 and components, R8, R9, R10, R3, T1 secondary and the traces. The system ground at connector P1 should be isolated from the other grounds if possible. Some systems require a connection from the connector to the logic ground. In such cases as the coaxial cable may be run near high disturbance sources and the far end may be connected to a separate system with a separate ground reference, DC current and EMI generated AC currents may flow through the shield of the cable. The demo board provides placement for two components C8 and C10, which connects the cable shield to the GND. These components can be completely removed for full isolation or include either capacitors or zero Ohm resistors for direct connection to GND. The customer can experiment to establish which option will satisfy his requirements best. The possible problem with the zero Ohm resistors is the DC path between the far end and the near end, which may connect the two building grounds together. The advantage with the capacitors is that the DC path is cut, but we have introduce an AC impedance between to two grounds, this means that the capacitor value will have to be chosen depending on the predominant interference frequency. For the positive supply we recommend a plane that connect all the supply pins of the 78P2241. This supply plane should be connected with the lowest possible impedance to the major supply, if that supply is feeding the digital logic a ferrite bead with decoupling capacitors on both sides of the ferrite bead is strongly advice. This will suppress any noise generated by the digital logic that could interfere with the 78P2241. It is advisable to void the positive supply under the coaxial connectors and primary of the transformers to avoid noise to be coupled in the supply.

PERFORMING TESTS WITH DEMO BOARD

The general test setup using the demo board is show in figure 2. When remote loop back (DLB) is enabled at pin 26 (floating), the receiver logical outputs (RCLK, RPOS and RNEG) connected to the transmitter logical inputs (TCLK, TPOS and TNEG). As a result, the received AMI signal is transmitted back to the test equipment. Monitoring bit error rate

indicates the ability of the IC to receive and transmit the AMI signal without errors.
As show in Figure 2, 450 feet of 75 Ohm coaxial cable (type RG59B) plus resistive attenuation are used in the receive path to exercise the IC. The following tests are performed on the receiver.

BIT ERROR RATE TEST

The test equipment generates a pseudo-random pattern. This pattern is created using a shift register of N bits. A combination of 2**N-1 patterns of N bits is created in a random manner. This pattern is used to simulate live traffic on the AMI line. The following table shows the typical patterns to test the IC:

SPEED	RANDOM PATTERN	FIXED PATTERN
DS3	2**15-1	100100
STS-1	2**15-1	100100
E3	2**23-1	10001000

Table 5. Test patterns.

When running these patterns, the bit error ratio should be lower than 10^{-9}. The test is repeated for fixed patterns to exercise the IC for any pattern sensitivity.

JITTER TOLERANCE

Telecommunication equipment should be able to recover clock and correct data even if the AMI signal includes a certain amount of timing jitter. For this test, the test equipment adds jitter to the random AMI signal. For jitter at a set frequency, the jitter amplitude is slowly increased until bit errors are observed. This process is repeated at different frequencies. A plot of tolerated jitter amplitude vs.jitter frequency is made as show in Figures 6 and 7. The system should tolerate jitter in excess of specified requirements. For the test set up see Figure 4.

INTRINSIC JITTER

The jitter generated by the IC in the absence of any jitter on the transmitter logical input (TCLK, TPOS, TNEG) is minimal (see Figures 8 and 9). For the bench test set up see Figure 4.

JITTER TRANSFER FUNCTION

The IC should not cause any amplification of the system jitter, i.e., very small peaking should be observed in the jitter transfer function. This objective is achieved by selecting the PLL filter components for an over damped response. The test equipment adds jitter to the AMI signal received by the IC. Measuring the jitter transmitted by the IC in the remote loop back mode indicates the shape of the transfer function. As show in Figure 10, the IC adds very small peaking and higher frequency jitter is attenuated. Figure 5 shows the bench test set up.

TRANSMITTER TESTS

The AMI pulse generated by the IC can be tested for its shape, amplitude and frequency contents over different lengths of cable. The demo board is usually placed in remote loop back this by leaving pin 28 floating. For bench test set up see Figure 3.

TRANSMITTER PULSE FREQUENCY CONTENTS

For an AMI signal with an “all ones” pattern, the transmitted signal should have a frequency spectrum with the main component at half of the bit rate. The signal power at the harmonics including the component at the bit rate should be at least 20 dB lower than the main component. A spectrum analyzer is used for this purpose. The measured power is 4.9 dBm for DS3 at 3.3V supply and the second harmonic is at most 35 dB lower. At 5.5V supply the output power is 5.2 dBm and the second harmonic is at most 35 dB lower.

TRANSMITTER PULSE AMPLITUDE

The pulse amplitude for a pattern of 100100… is measured at different cable lengths by connecting the end of the cable to the scope using a 75-Ohm adapter (PONOMA 4119 see figure 3). For E3 the transmitted pulse amplitude needs to be fairly exact (2Vp-p $\pm$ 10%) see figure 13. For DS3 and STS-1 the transmit amplitude may fall in a wide range of amplitudes from 0.72 to 1.7 Vp-p (see Figures 11 and 12). For STS-1 a pseudo random pattern is used and the output signal is matched against an Eye diagram as seen in Figures 14 and 15.

TRANSMITTER PULSE SHAPE

The shape of the signal at the end of a 75-Ohm cable is examined by comparing it to the published templates. The test setup is show in Figure 3. The program resident in the scope reads the transmitter waveform, scales it vertically, and plots it together with the published template masks. For DS3, the pulse shape should meet the mask for all cable lengths from zero to 450 feet. A typical pulse shape for the 78P2241 at the end of 450 feet of cable is show in Figure 11 and 12.

TRANSMITTER PULSE IMBALANCE

The AMI pulse generated by the IC includes pulses of both negative and positive polarities. Pulse imbalance is examined by inverting the negative pulse with the scope and overlaying it on a typical positive pulse. No significant imbalance is observed.

Data Sheet ref.	RFO
Demo Board ref.	R8,R9 or R10
Unit	KΩ
Tolerance	1%
DS3	5.23
STS-1	4.53
E3	6.81

Table 6: External Resistor List for Different Speeds

Position	IC pin	Function	Jumper in	Default
ICKP 1-2	ICKP	Clock polarity	TCLK inverted	
ICKP 3-4	ICKP	Clock polarity	Same as 7200	All Boards
ICKP 5-6	ICKP	Clock polarity	Both clock inv.	
RFO 1-2	DS3/E3	Speed select	STS-1	STS-1
RFO 3-4	DS3/E3	Speed select	DS3	DS3
RFO 5-6	DS3/E3	Speed select	E3	E3
LPBK 1-2	LPBK	Loop Back	Remote	
LPBK 3-4	LPBK	Loop Back	No Loop Back	All Boards
LPBK 5-6	LPBK	Loop Back	Local	
MON 1-2	MON	Flat Gain	20dB	
MON 3-4	MON	Normal	0dB	All Boards
TXEN 1-2	TXEN	Driver enable	Enable	All Boards
TXEN 3-4	TXEN	Driver enable	Disable	
MODE 1-2	MODE	TX Pulse shape	STS-1	STS-1
MODE 1-2	MODE	TX Pulse shape	DS3	DS3
MODE 1-2	MODE	TX Pulse shape	E3	E3
Test 1-2	LBO	TX Cable > 225’	Test	
Test off	LBO	TX Cable < 225’	Off	All Boards
ENDEC 1-2	ENDEC	B3ZS/HDB3	Coding on	
ENDEC 3-4	ENDEC	B3ZS/HDB3	Coding off	All Boards

Table 7: Function of Jumpers, Default column shows factory settings

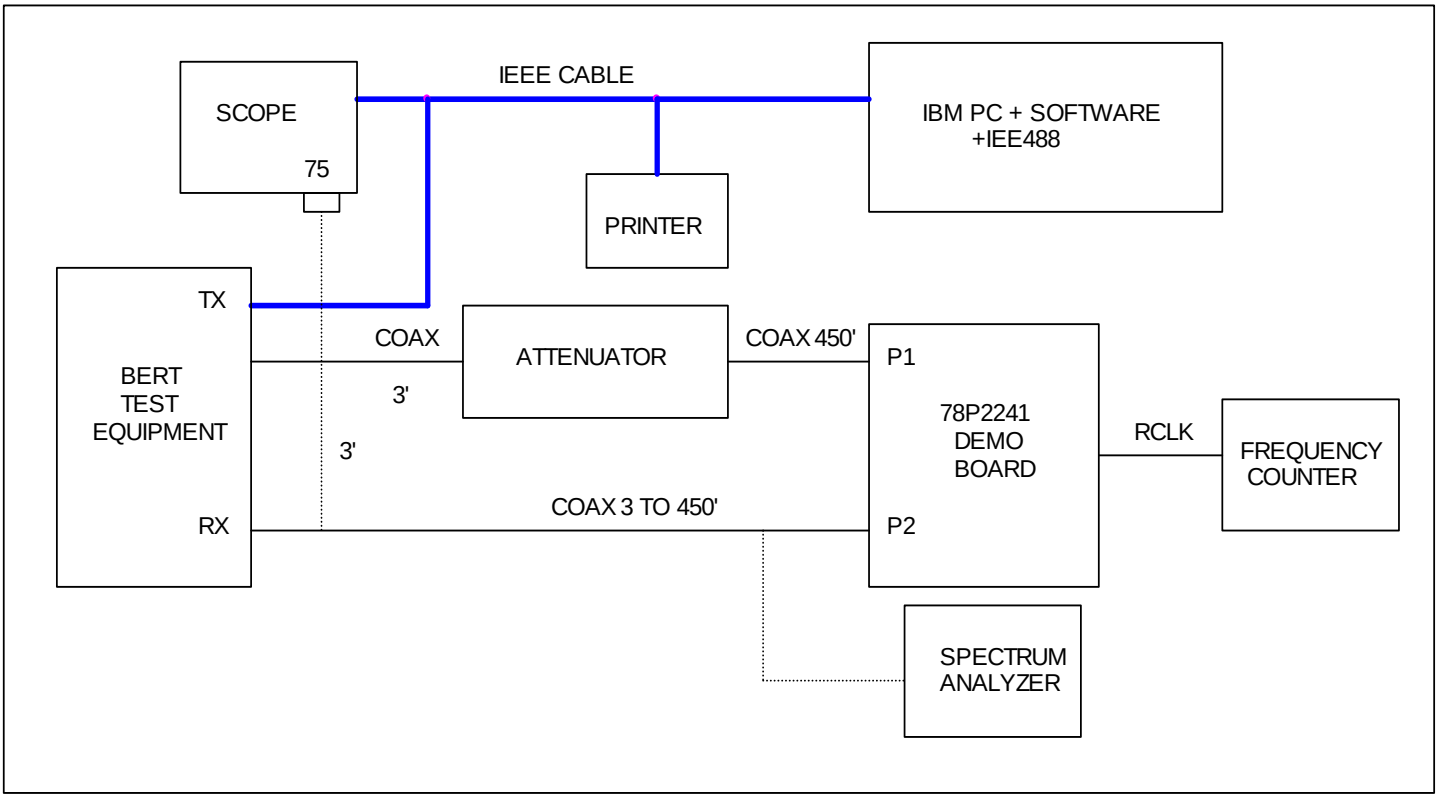


Figure 2. Test set up for performance testing

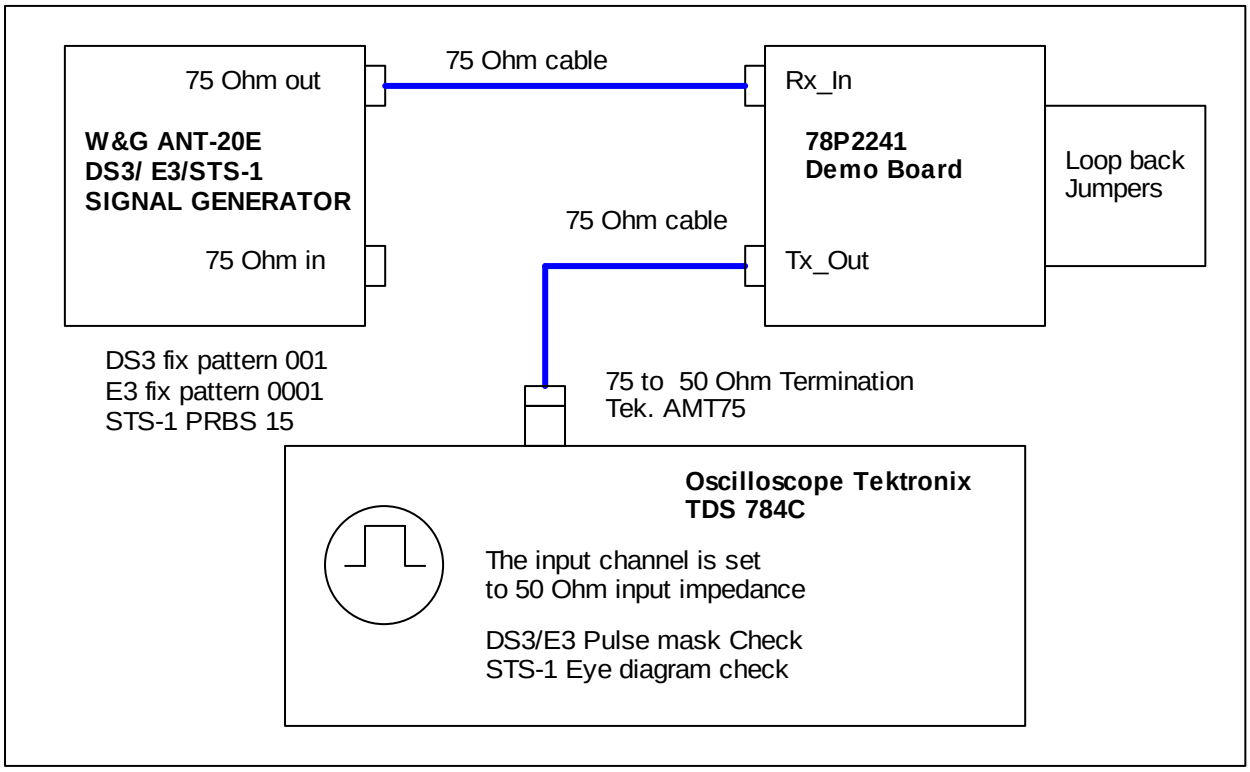


Figure 3. Test set up for pulse mask checking

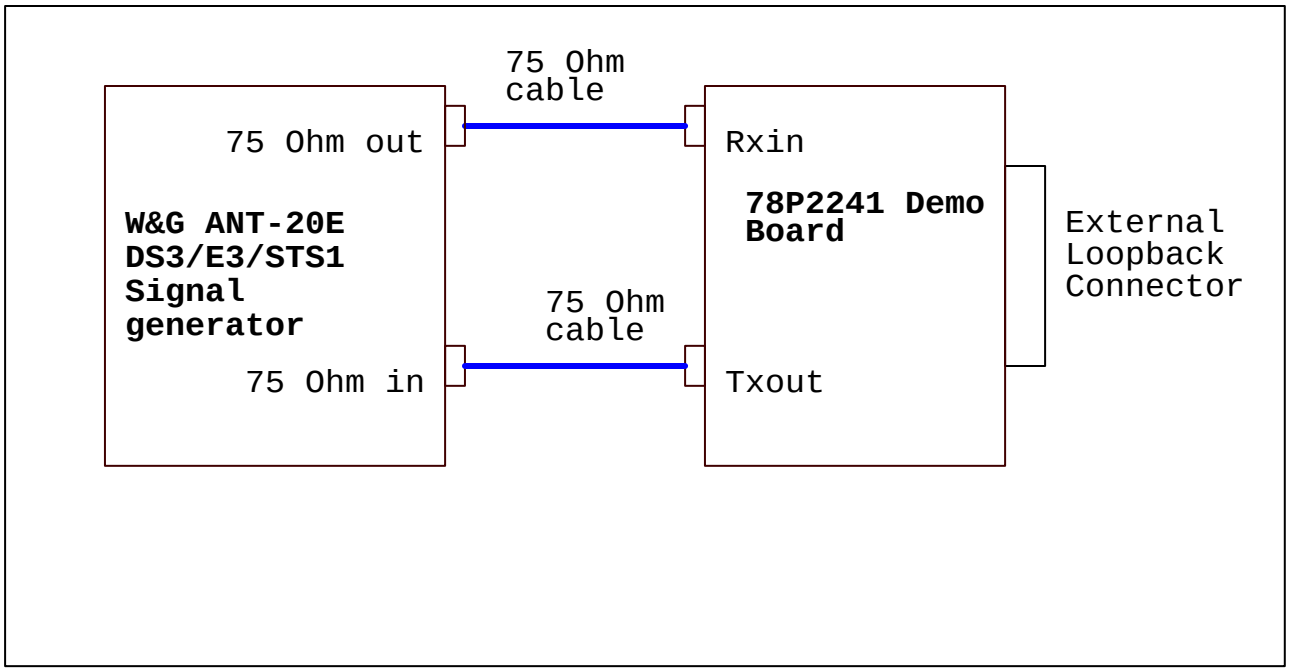


Figure 4. Test set up for Jitter Tolerance and Jitter Transfer Function

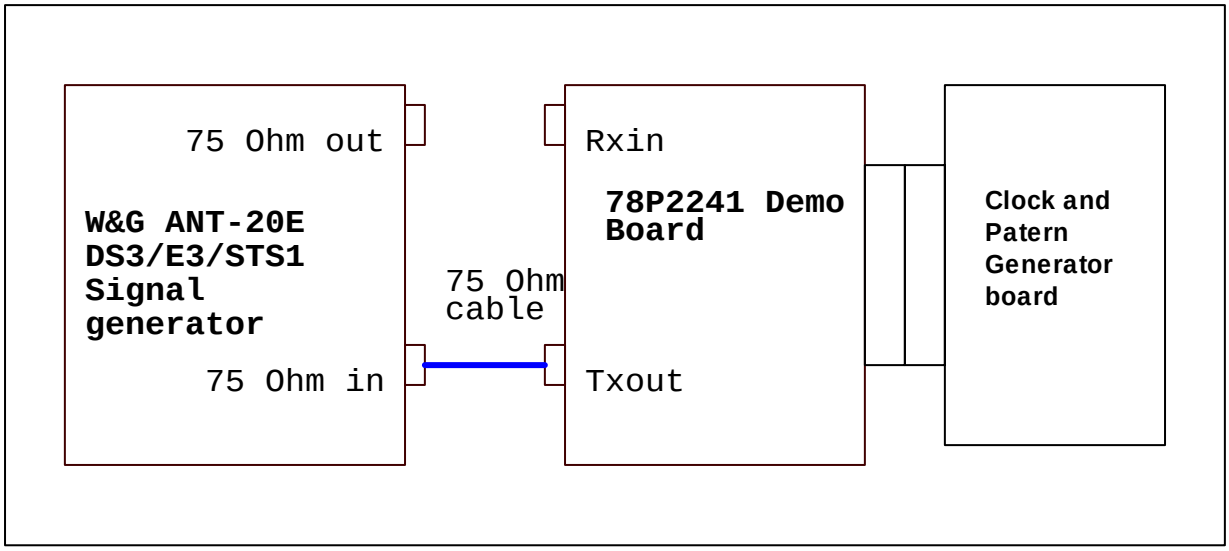


Figure 5. Test set up for Intrinsic Jitter measurement

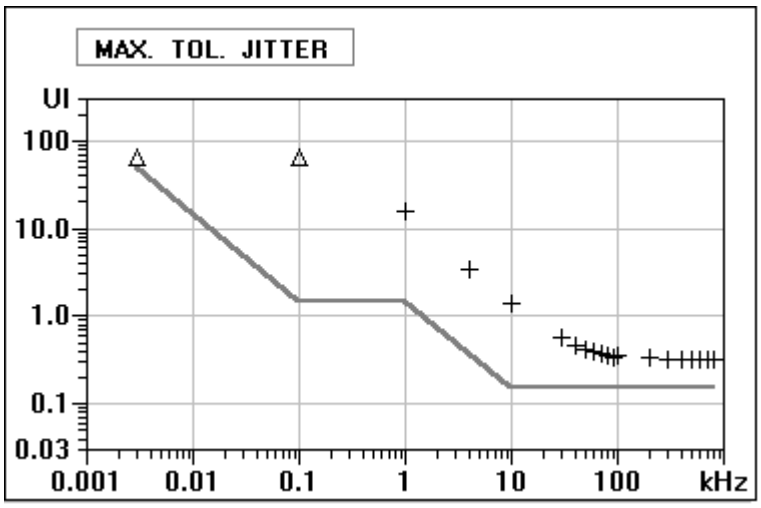


Figure 6. Jitter Tolerance Plot , E3 rate at 3V, 5.5V and 0 to 1035 Feet

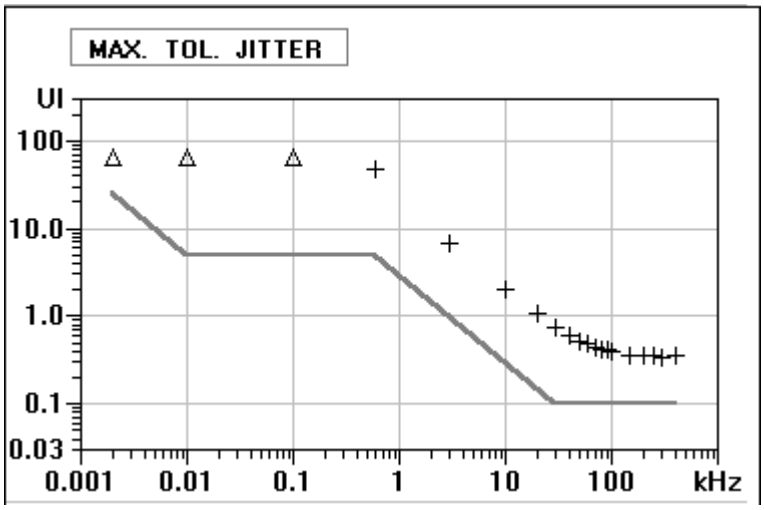


Figure 7. Jitter Tolerance Plot, DS3 rate at 3V, 5.5V and 0 to 450 Feet

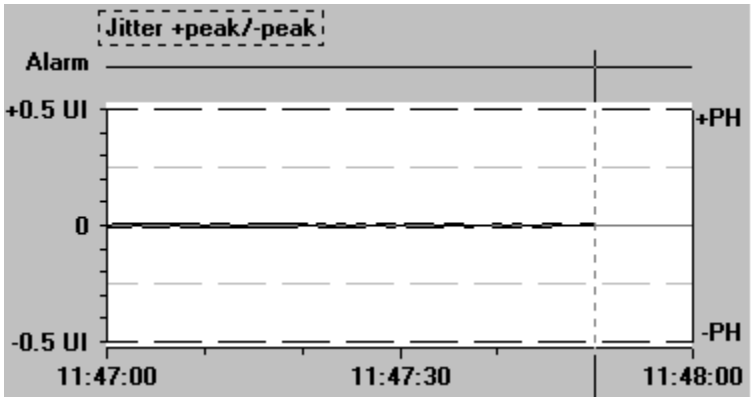


Figure 8. Intrinsic jitter peak to peak for all rates and supply voltages.

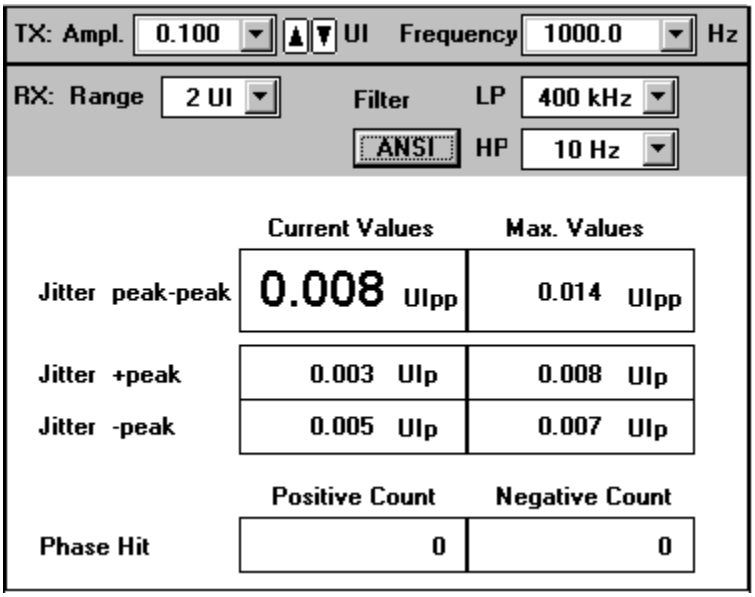


Figure 9. Intrinsic jitter table for all rates and supply voltages.

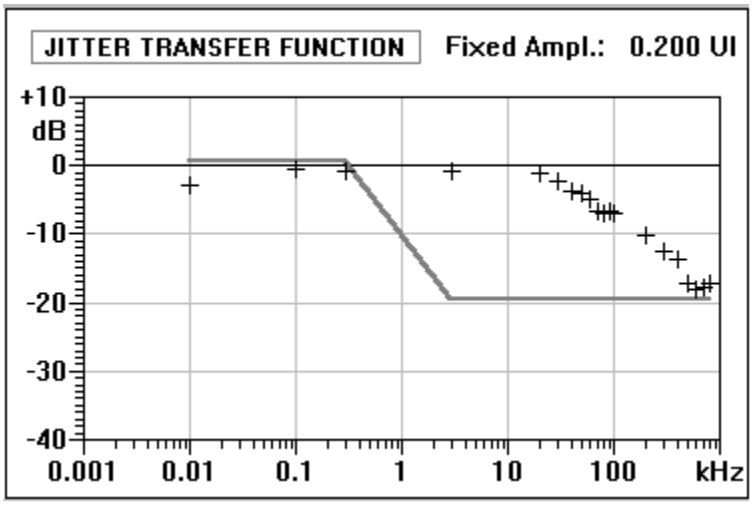


Figure 10. Jitter Transfer Function for all rates and supply voltages

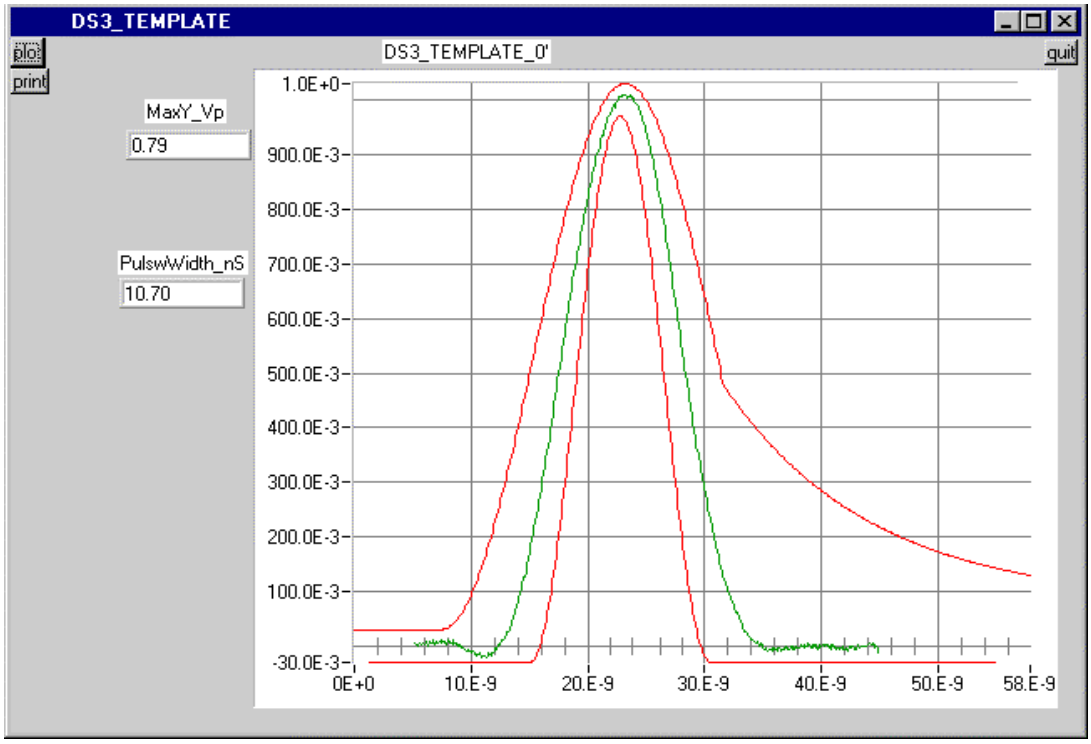


Figure 11. DS3 template at 0 feet of cable

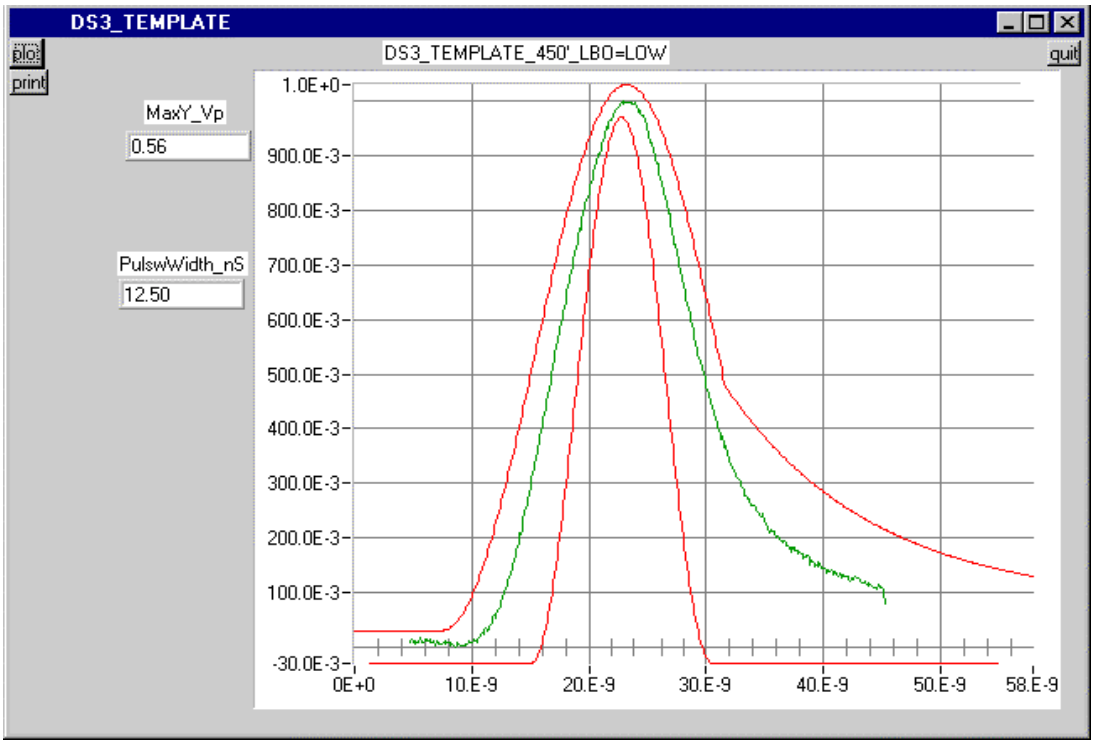


Figure 12. DS3 template at 450 feet of cable

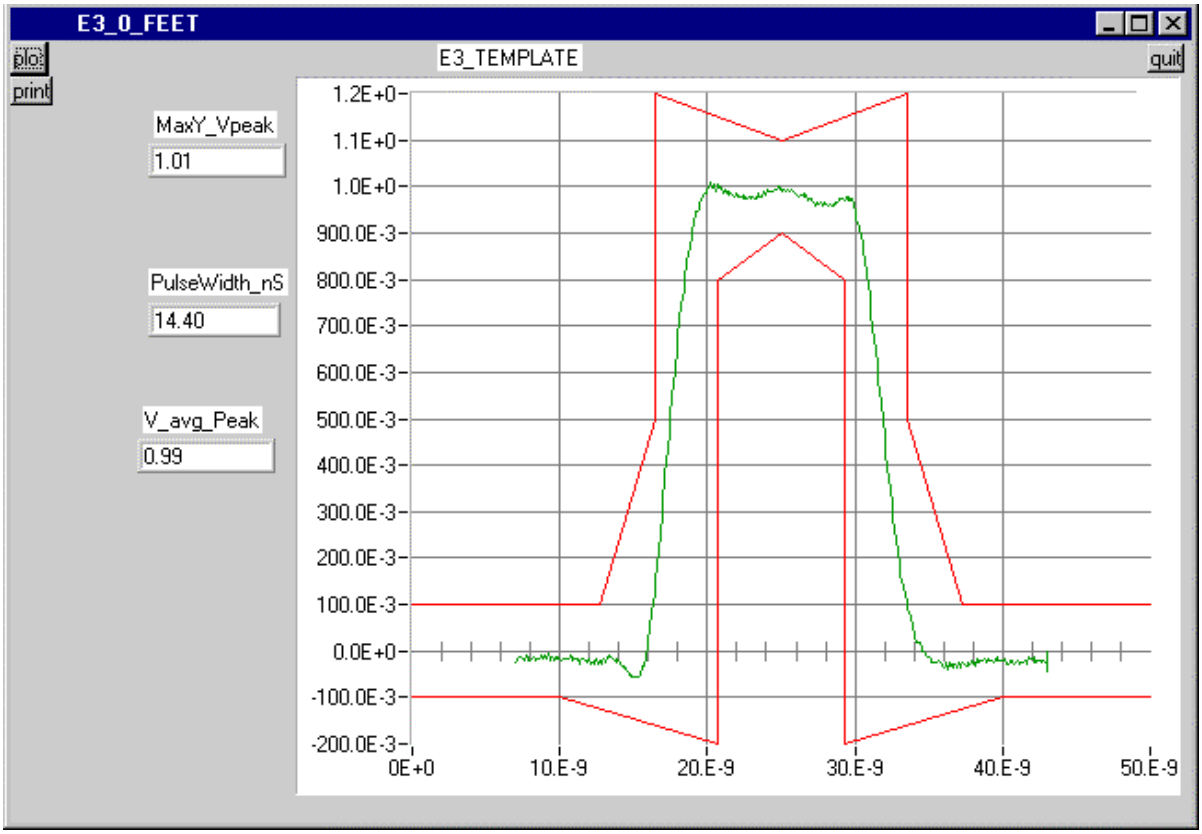


Figure 13. E3 template at 0 feet of cable

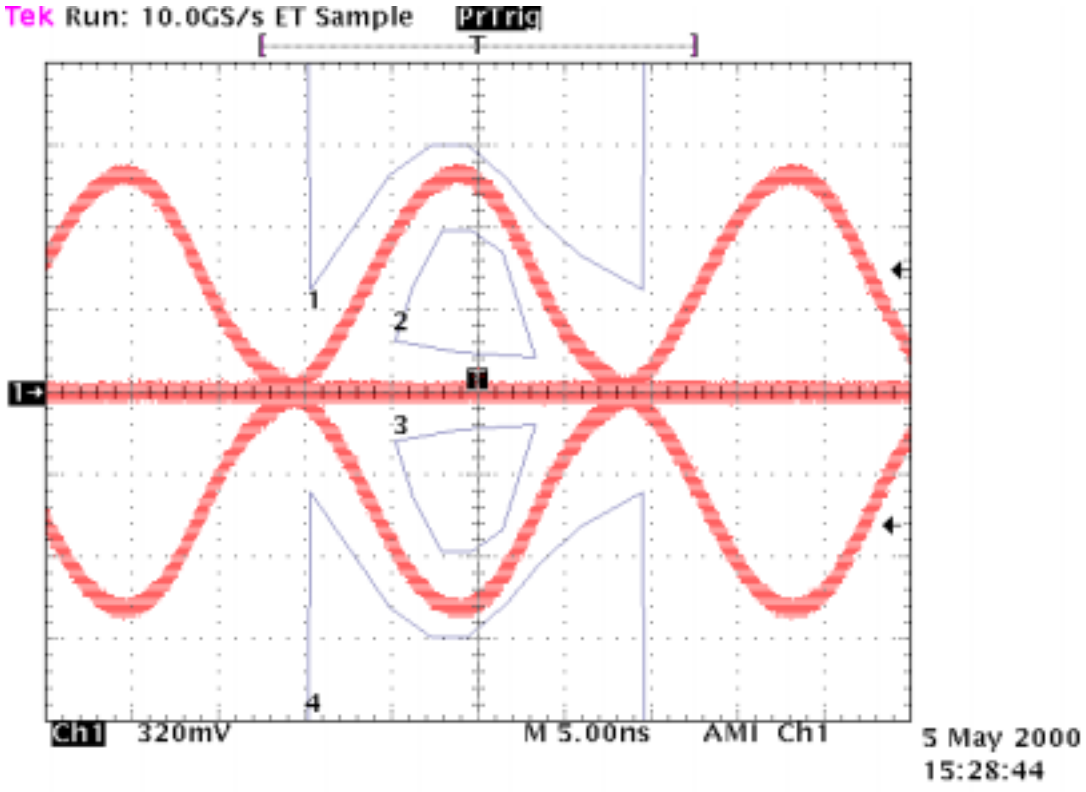


Figure 14. STS-1 Eye Diagram at 0 feet of cable

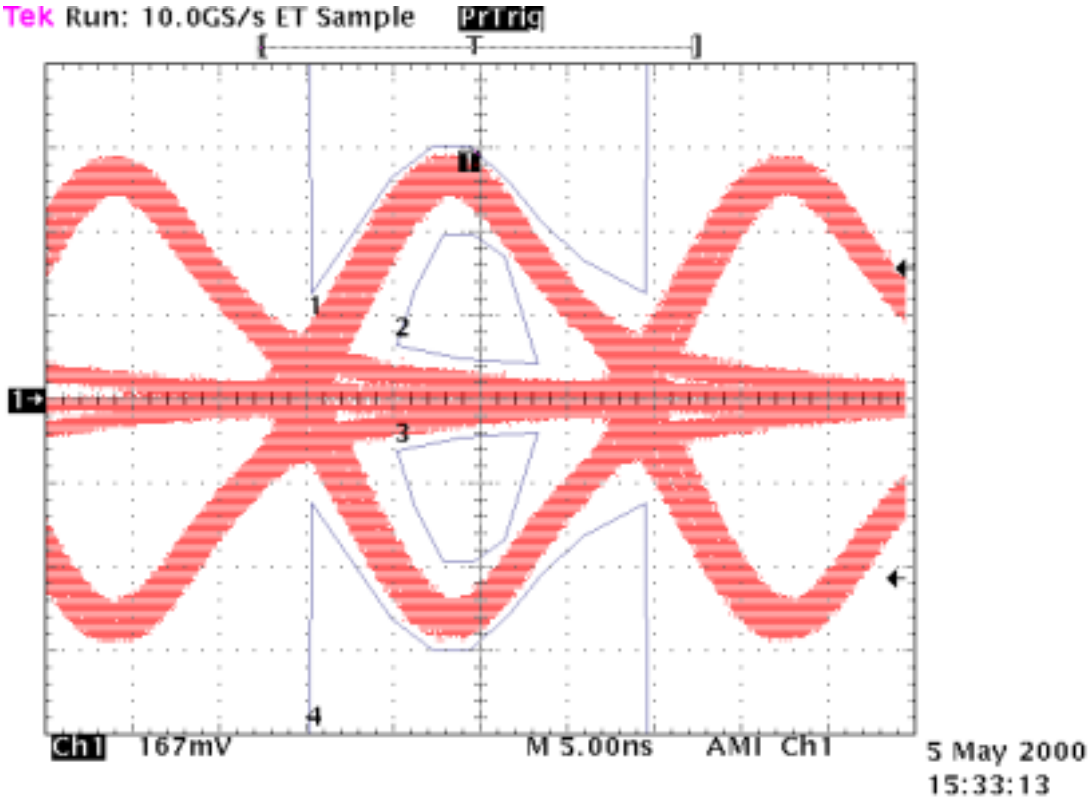


Figure 15. STS-1 Eye Diagram at 450 feet of cable LBO off.

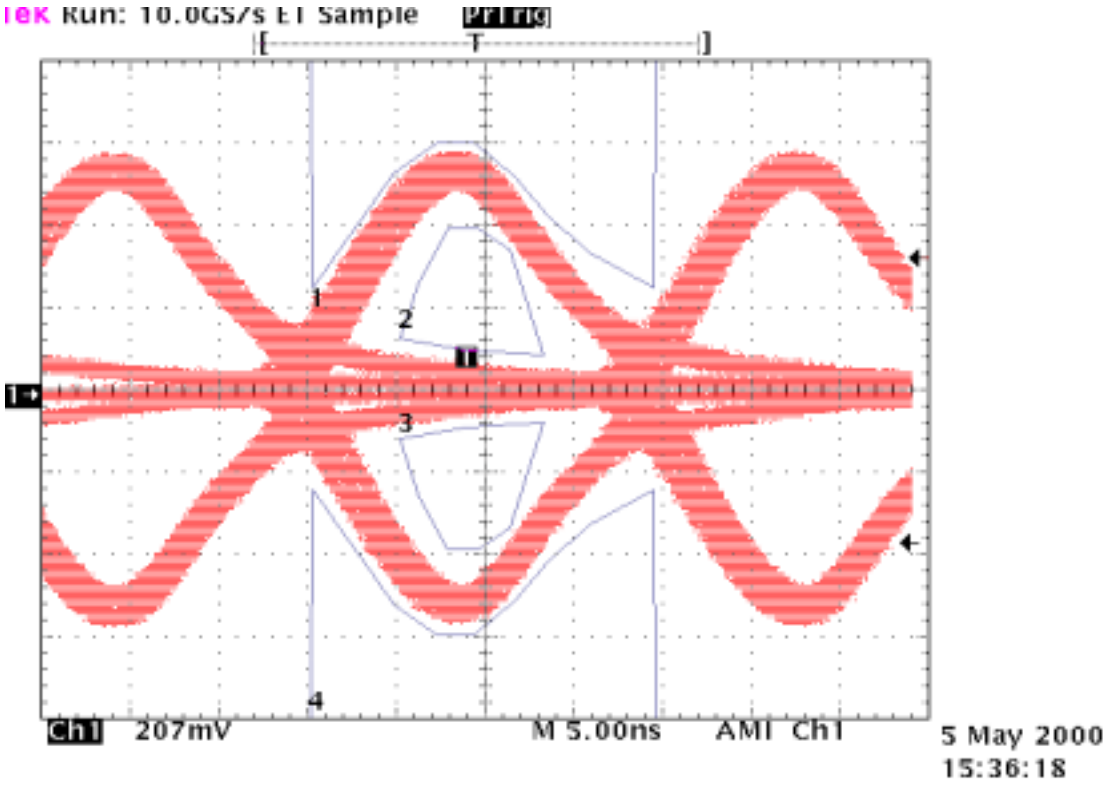


Figure 16. STS-1 Eye Diagram at 450 feet of cable LBO on.

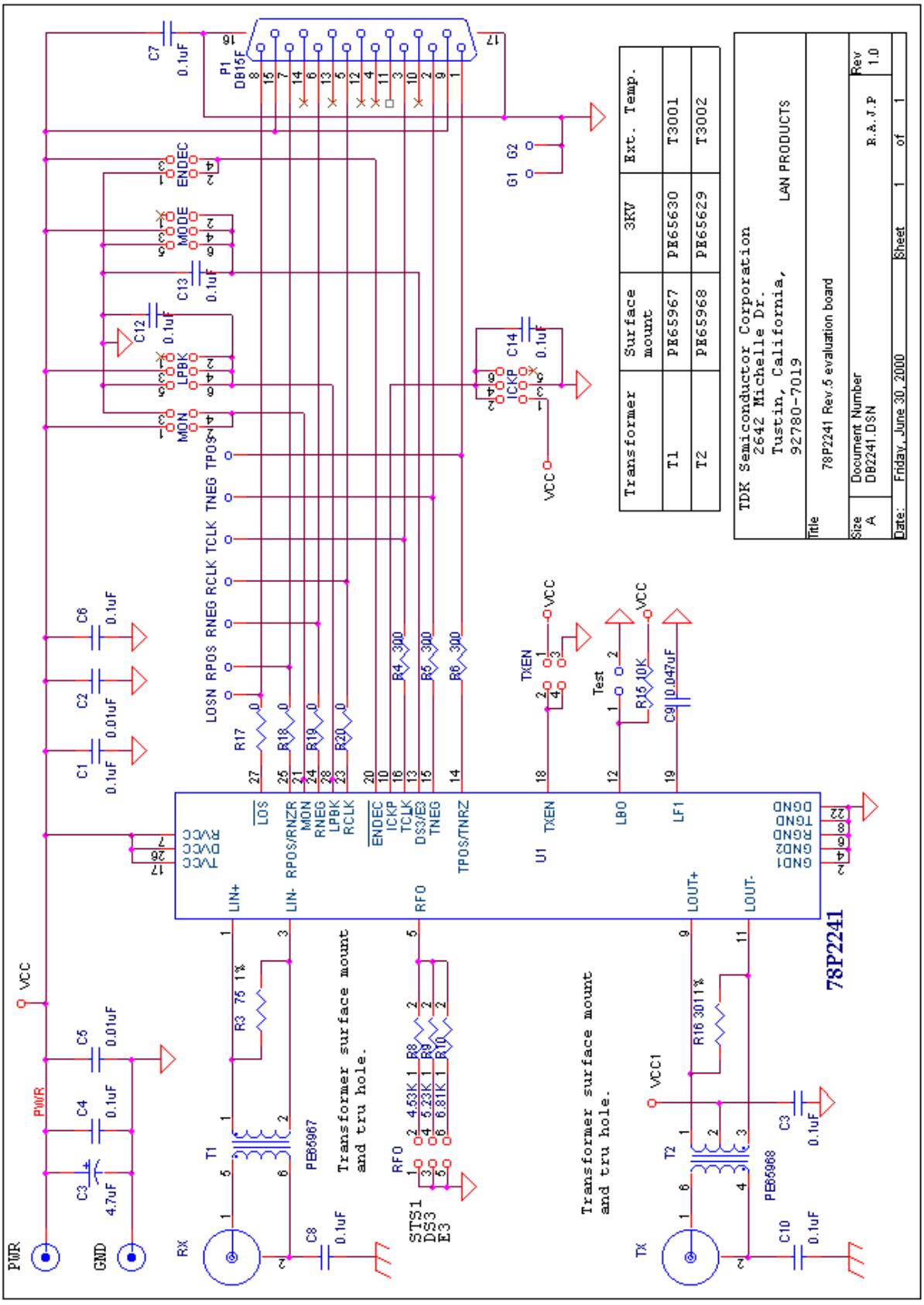


Figure 17. Demo Board Schematic of the 78P2241-PLCC

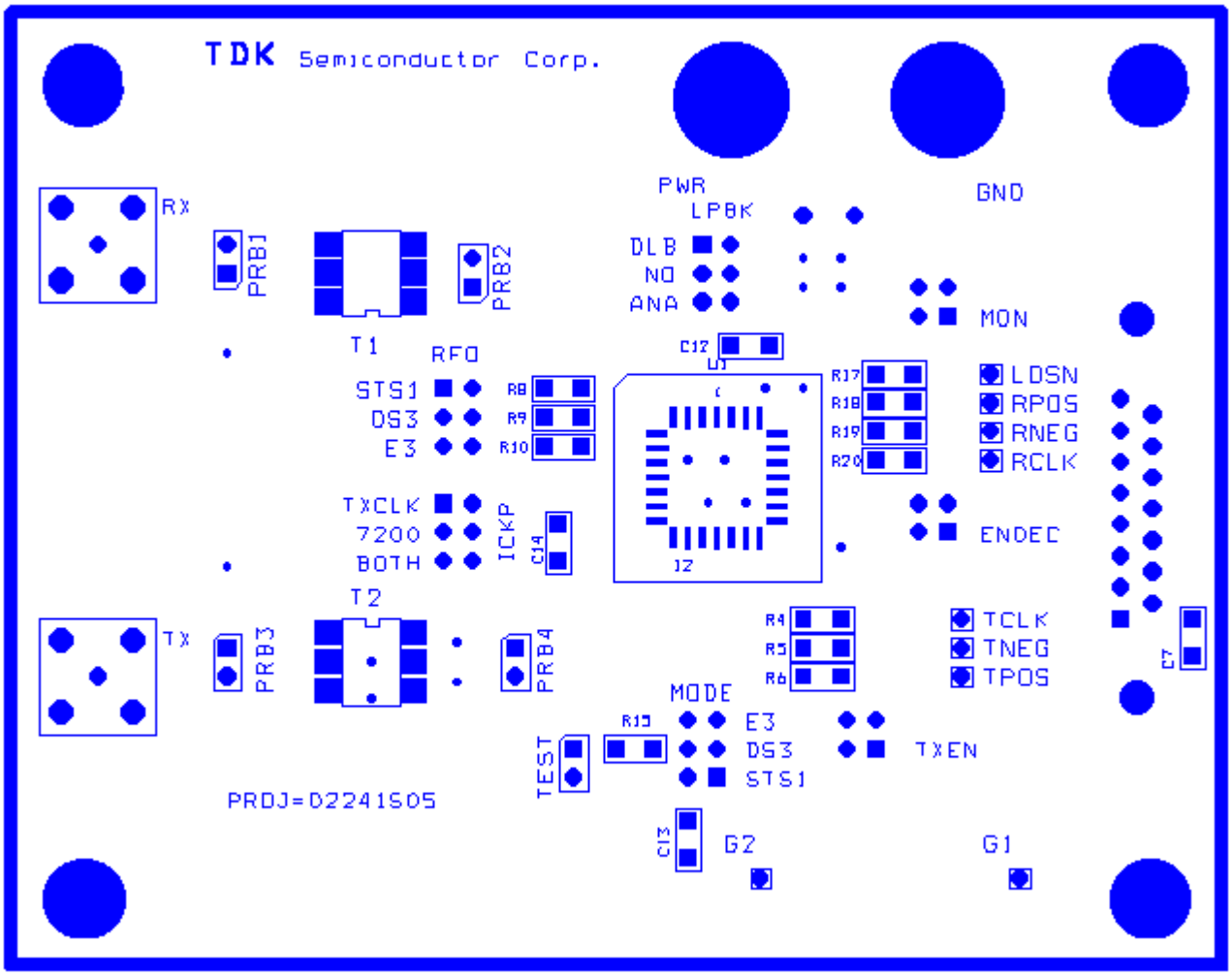


Figure 18 Top Silk Screen

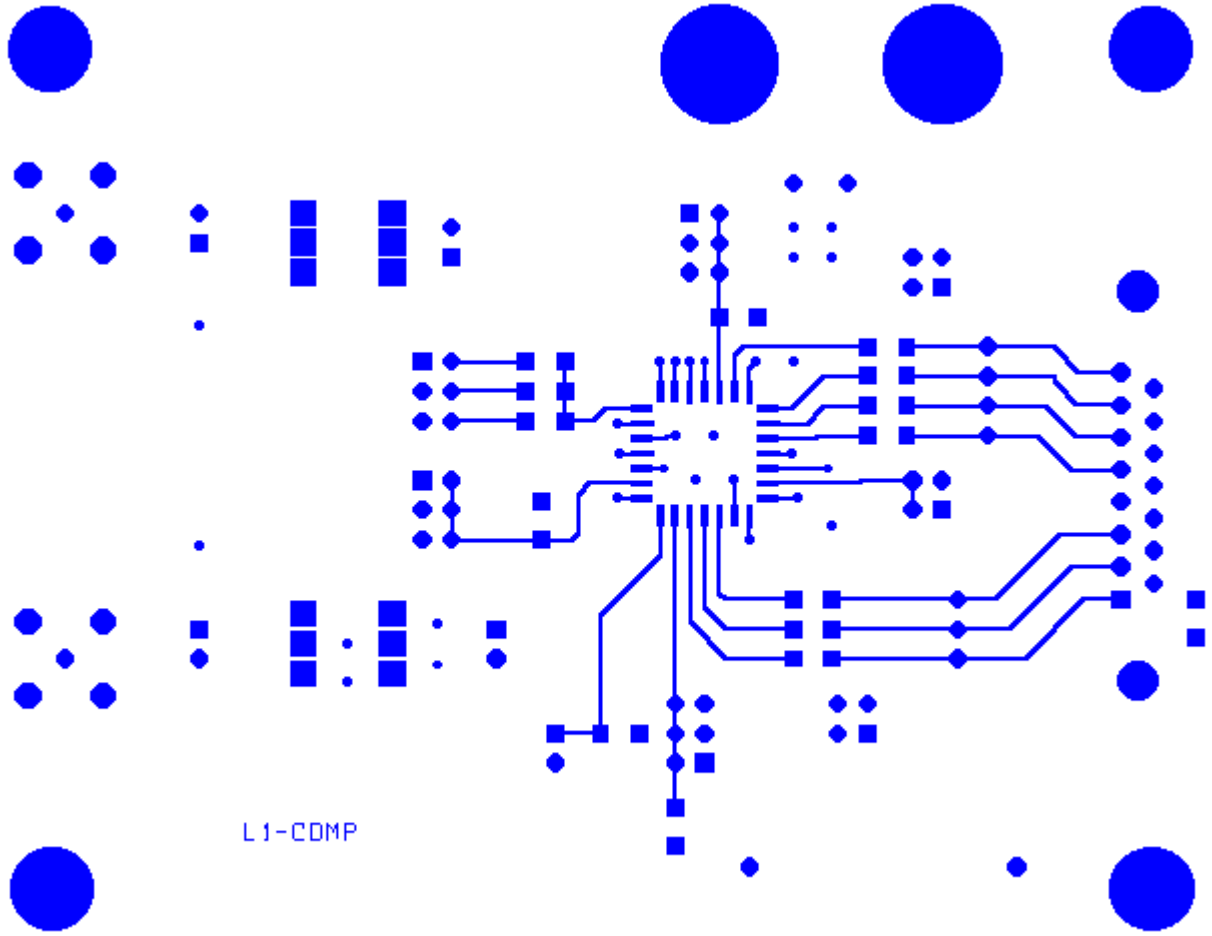


Figure 19. Layer 1 Top Signal Traces.

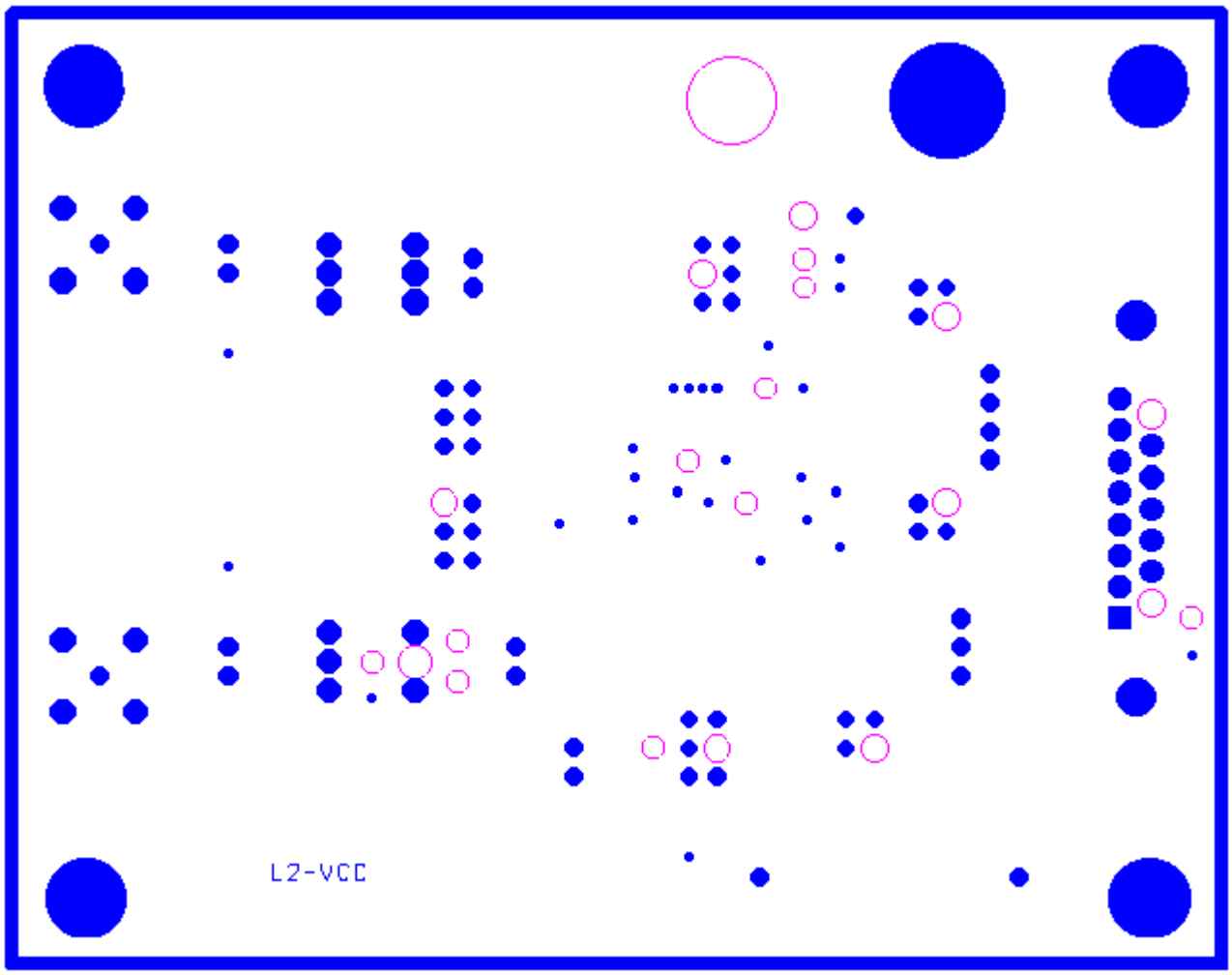


Figure 20. Layer 2 VCC plane.

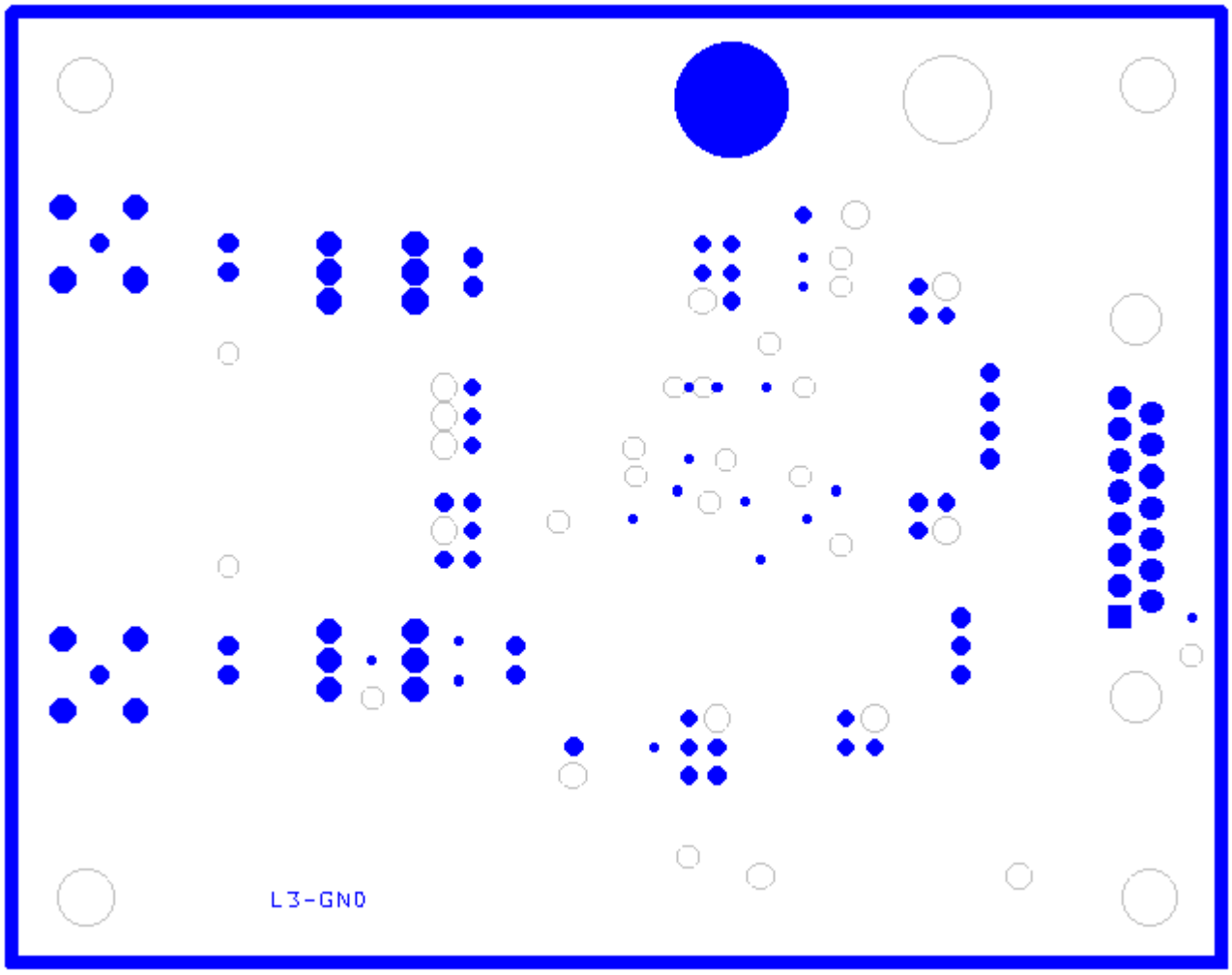


Figure 21. Layer 3 Ground Plane.

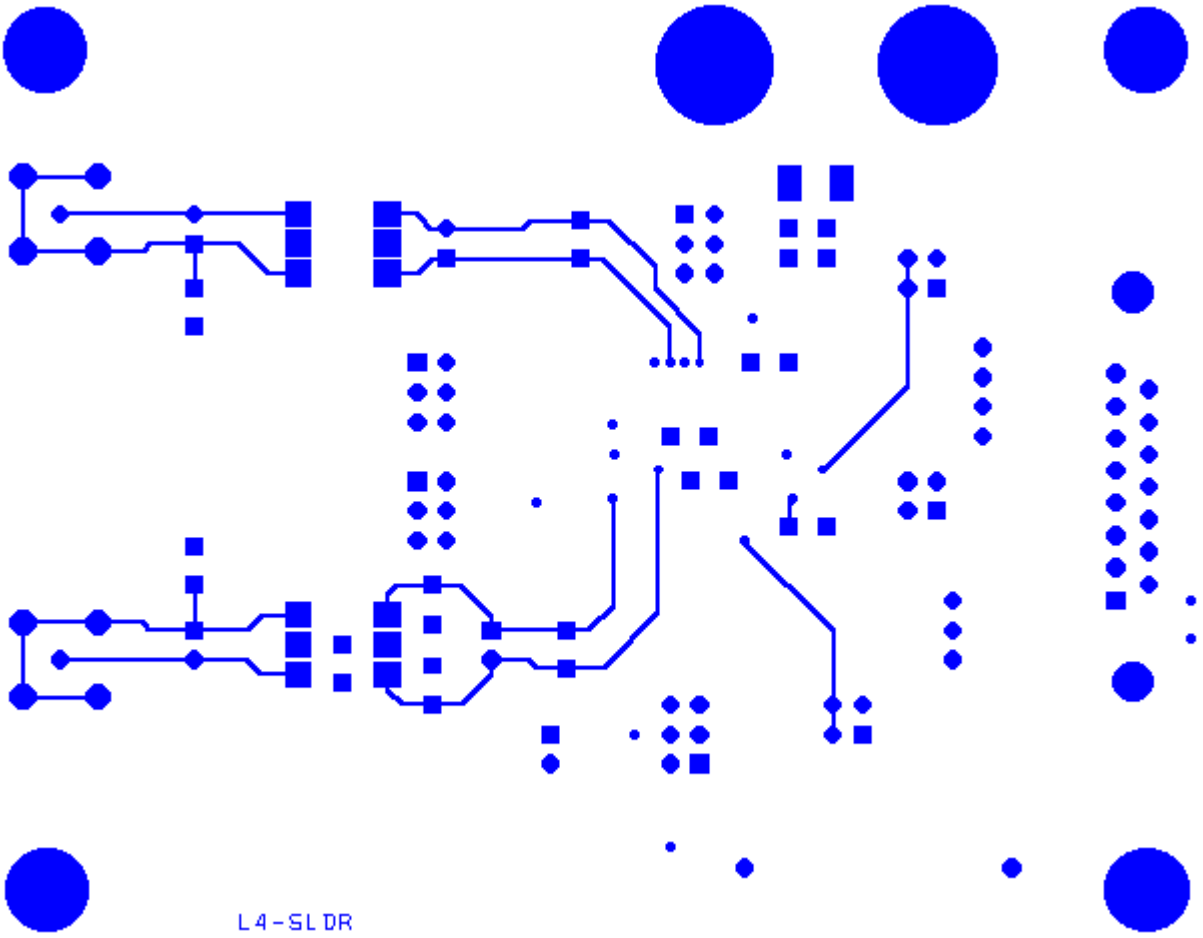


Figure 22. Layer 4 Bottom Traces.

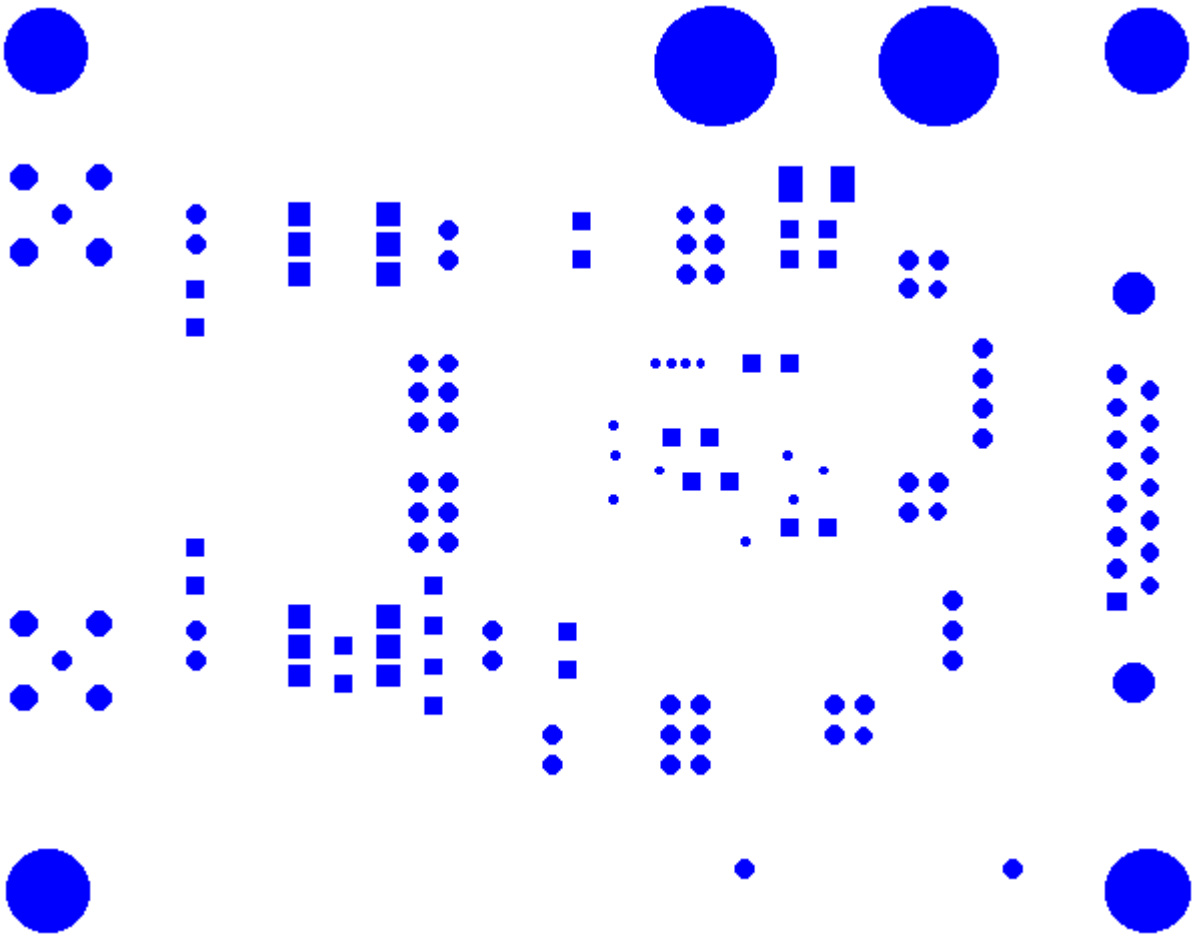


Figure 23. Assembly Drawing.

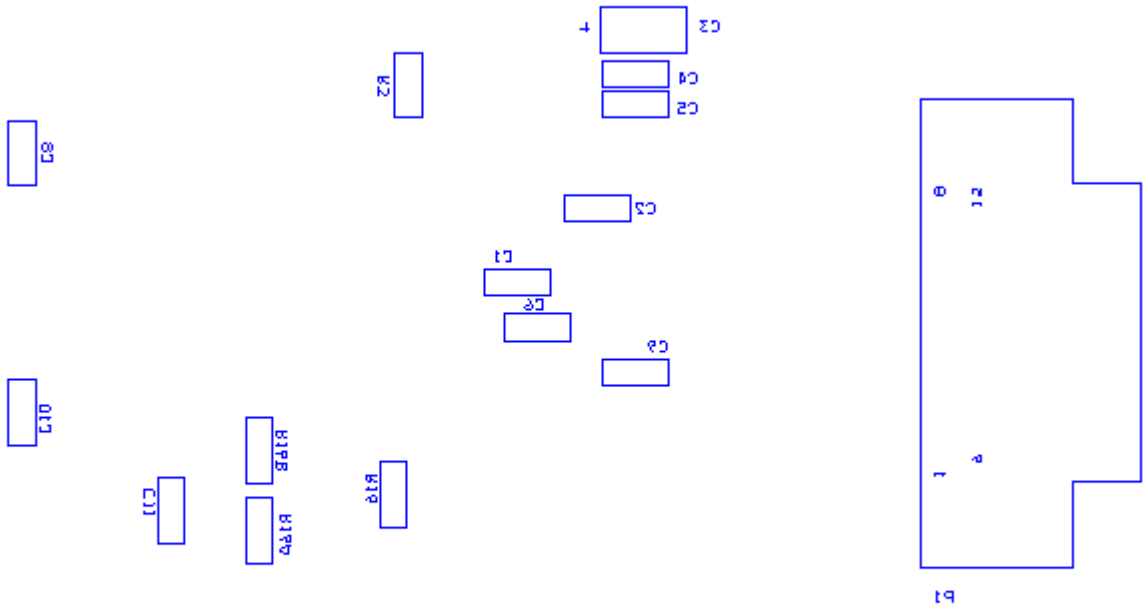


Figure 24. Bottom components.

78P2241 28-pin PLCC evaluation board
Revised: Monday, April 24, 2000
D2241S05 Revision: 1.0

TDK Semiconductor Corporation
2642 Michelle Dr. Tustin CA. USA
WAN PRODUCTS

Bill Of Materials

Item	Quantity	Reference	Part	Manufacturer	Part #	Size	PRECISION
1	8	C1,C4,C6,C7,C11, C12, C13, C14	0.1uF	TDK	C3216X7R1E104M	CC1206	20%
2	2	C5, C2	0.01uF	TDK	C3216X7R1E103M	CC1206	20%
3	1	C9	0.047uF	TDK	C3216X7R1E473K	CC1206	10%
4	1	C3	4.7uF	PANASONIC	ECS-T1EC475R	CC1812	20%
5	2	TX, RX	BNC 75Ω	AMPHENOL	31/5329		
6	4	R17, R18, R19, R20	0	PANASONIC	ERJ-8GEY0R00V	CC1206	5%
7	1	R3	75	PANASONIC	ERJ-8ENF75	CC1206	1%
8	3	R4, R5, R6	300	PANASONIC	ERJ-8GEYJ300	CC1206	5%
9	1	R16	301	PANASONIC	ERJ-8ENF301	CC1206	1%
10	1	R16	10K	PANASONIC	ERJ-8GEYJ10K	CC1206	5%
11	1	R8	4.53K	PANASONIC	ERJ-8ENF4.53K	CC1206	1%
12	1	R9	5.23K	PANASONIC	ERJ-8ENF5.23K	CC1206	1%
13	1	R10	6.81K	PANASONIC	ERJ-8ENF6.81K	CC1206	1%
14	1	T1	PE65968	PULSE	PE65968	SMT	3%
15	1	T2	PE65969	PULSE	PE65969	SMT	3%
16	1	U1	78P2241	TDK	78P2241-IH	28-PLCC	

Table 8. Bill Of Materials.