TDK SEMICONDUCTOR CORP.

78P7200L 28-pin PLCC Demo Board

APPLICATION NOTE

DECEMBER 2000

INTRODUCTION

The purposes of this application note are to explain the design of the demo board using a 78P7200L PLCC package, and how to properly evaluate the 78P7200L single Line Interface Unit.

78P7200L is a low power single chip DS3/E3/STS1 Line Interface Unit. Using the most advanced BiCMOS technology the 78P7200L operates at +5V or +3.3V. The product is available in both 28-pin PLCC and 48 pin TQFP packages.

This application note will demonstrate that the 78P7200L is pin and function compatible with the 78P7200 at +5V. The 78P7200L printed circuit board is designed to be the same as the 78P7200 demo board.

DESCRIPTION

The 78P7200L-demo board is designed to facilitate the evaluation of the 78P7200L single chip DS3/E3/STS-1 Line Interface Unit. The demo board includes all of the necessary discrete components for the interface to a coded AMI line. The on-board jumpers control the option pins of the IC including the new loop-back functions.

FEATURES

- Allows easy evaluation of the 78P7200L
- Includes all necessary external components
- Includes jumpers to control options
- Operates at DS3, E3 or STS-1 by changing proper jumpers and RFO resistor.
- The demoboard can be configured to operate at either +5V or +3.3V
- 4 layer PC board construction

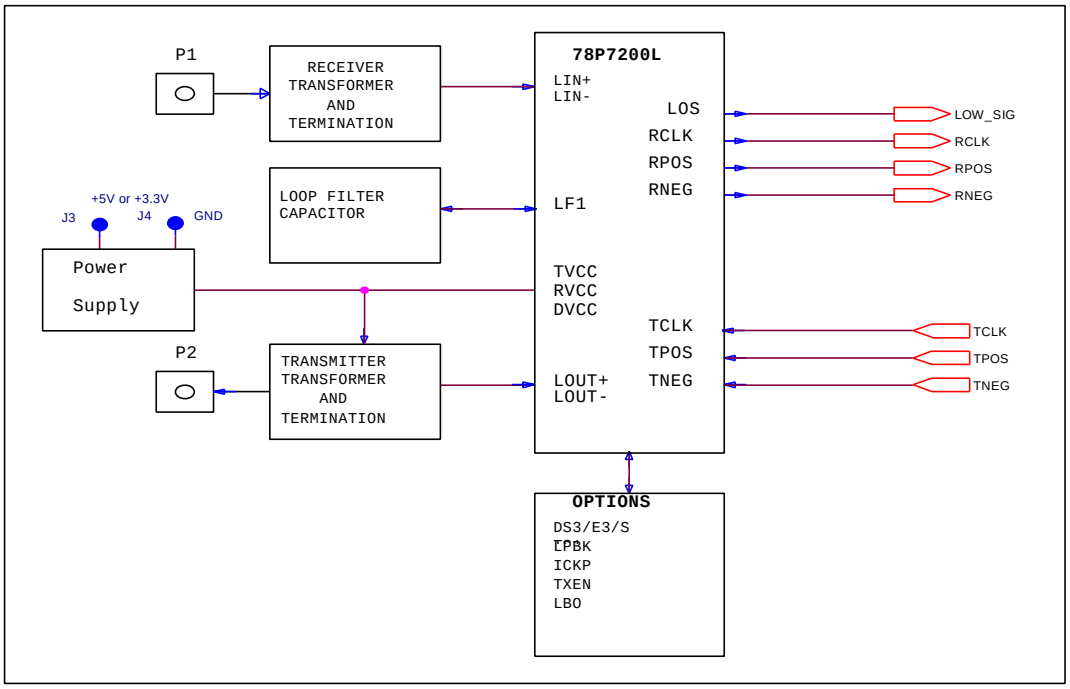

FIGURE 1: Demo Board block Diagram

POWER SUPPLY CONNECTION

The demo board is constructed as a four-layer PC board. The outer two planes carry the signals. The internal two layers are the ground and power supply planes. The power supply pins of the 78P7200L are connected directly to the supply planes.

RECEIVE SIGNAL PATH

The AMI input signal is connected to the BNC connector at P1. The maximum recommended distance of the demo board to a DSX3 cross-connect or a test equipment is 450 feet. The IC recovers clock, positive and negative data from the AMI signal, and it can handle added resistive attenuation. Table 1 shows the available receiver logic signals on the test points:

SIGNAL	
LOWSIG	TP5
RPOS	JP1_Left
RNEG	JP2_Left
RCLK	JP3_Left

Table 1. Receive Signals

The AMI input signal should be properly coded to prevent a long run of zero on the line. The proper code will limit the number of consecutive zeros to two or three depending on the speed. Table 2 shows the proper coding required by rate:

78P7200L RATE	SPEED Mbit/s	MAX zeros	CODE NAME
DS3	44.736	2	B3ZS
STS-1	51.840	2	B3ZS
E3	34.386	3	HDB3

Table 2. Coding names and rates

The AMI input signal to the IC can be monitored using a high impedance FET probe such as TEKTRONIX P4064 or HP 1141A.

The input signal is coupled through a 1:1 wide-band transformer. See Table 5 for a list of recommended transformers vendors.

The operation speed of the 78P7200L is controlled by changing the value of the resistor tied to RFO pin, pin 5. Table 3 shows the required external resistor (R5) for the different speeds.

Data Sheet ref.	RFO
Demo Board ref.	R5
Unit	KΩ
Tolerance	1%
DS3	5.23
STS-1	4.53
E3	6.81

Table 3: External Resistor List for Different Speeds

TRANSMIT SIGNAL PATH

The 78P7200L accepts CMOS level logical inputs (TCLK, TPOS and TNEG) and converts them to the proper AMI signals.

Table 4 shows the test points used for the transmitter.

SIGNAL	
TCLK	JP3_Right
TNEG	JP2_Right
TPOS	JP1_Right

Table 4. Transmitter signals.

The output pins of the 78P7200L, LOUT+ and LOUT- are connected to a 1:2CT wide-band transformer. See Table 5 for recommended transformers.

MANUFACTURER	PART NUMBER	PART NUMBER	COMMENTS
Reference	**T1, Receiver**	**T2, Transmitter**	
TDK	WBTT3.6-0340E	WBTT3.6-0401	Surface mount
PULSE	PE-65966	PE-65969	Through Hole
PULSE	PE-65967	PE-65968	Surface mount
PULSE	PE-68629	PE-68630	TH 3KV Isolation
PULSE	T3001	T3002	SMT Ext. Temp.
HALO	TD01-0406NE	TD07-0206NE	Through Hole
HALO	TG01-0406NS	TG07-0206NS	Surface mount
HALO	TD01-0456NE	TD07-0356NE	DIP Ext. Temp.
HALO	TG01-0456NS	TG07-0356NS	SMT Ext. Temp.

Table 5. Recommended Transformers and Vendors

The transmitter transformer center tap is connected to the positive supply. The objective is to meet a pulse template at any cable length up to the maximum of 450 feet. The generated AMI signal is available on the BNC connector, P2, and it can be monitored by using a high impedance probe, or via a 75 Ohm to 50 Ohm adapter (see Figure 3).

OPTION PINS CONTROL

E3 pin 13. This pin selects the mode the 78P7200L will operate in; the three selectable modes are DS3 (high), E3 (low) or STS-1 (floating).

TXEN pin 18. This input enables the transmitter drivers. When high, the part is in normal operation. When low, the outputs LOUT+ and LOUT- are in high impedance state, this feature is used connect two transmitters together and to save power when the drivers are not used.

ICKP pin 10. When this input is low, the data are presented at the output at the high to low transition of the clock, and the data are sampled at the input at the low to high transition of the clock. If pin 10 is high then transmit clock is inverted. If the pin 10 is floating then both received and transmit clocks are inverted.

LPBK pin 28. This input controls the two loop-backs. When pin 28 is high then the loop-back is not selected. Remote loop-back is selected when pin 28 is floating, this loops the receive data and receive clock pins to transmit data and clock inputs, receive data and clock are still present at the logic outputs. Local loop-back is selected when pin 28 is low. Both the LOUT+ and LOUT- are connected to LIN+ and LIN- such that the data present at the logic transmit inputs will be reflected at the receive logic outputs.

LBO pin 12. This input controls the amplitude of the output signal in DS3 and STS-1 mode. If the cable length is less than 225 feet this pin need to be high or floating. For all cable lengths higher than 225 feet this input should be low.

To ensure that the 78P7200L see a float condition, the input should sink less than 10 microampere. Consider that the input impedance of the input pin is between 15 and 20KOhm and the float voltage is 1.5V with a tolerance of 20%.

BOARD LAYOUT CONSIDERATIONS

When designing a system board for high-speed applications, there are several important factors to consider. This document contains a few recommendations that can help alleviate noise due to sub-optimal board layout around the LIU.

A possible layout approach is to use a different ground at the BNC connectors for noise immunity. The BNC connectors should be connected to frame ground. The component ground should be a plane that connects directly to the negative supply pin. This ground plane will carry all the return currents of the LIU logic. The frame ground at the BNC connectors should be isolated from the other grounds if possible. It is important that the grounds should be isolated from each other by placing a strip of area, which is void of copper in the ground plane underneath the primary of the transformers. See Figure 2.

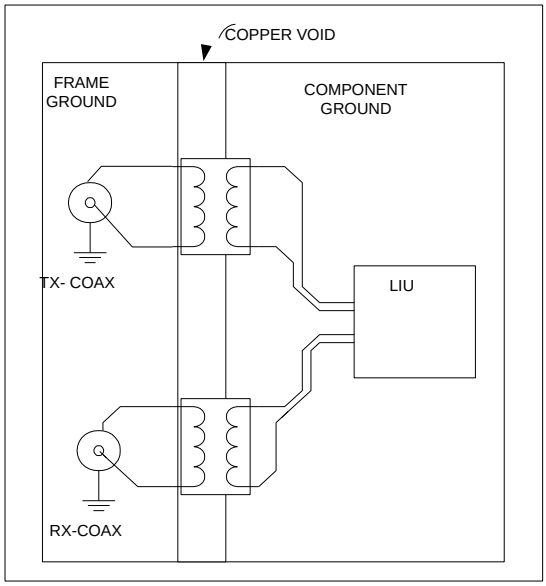

Figure 2. Two different ground areas

In some systems there is a requirement for a connection from the connector to the frame ground. In a situation where the coaxial cable being run near high disturbance sources and the far end being connected to a separate system with a separate ground reference, DC current and EMI generated AC currents may flow through the shield of the cable. In this case the layout should provide placement for components that connect the cable shield to the frame ground. These components can be completely removed for full isolation or include either capacitors or zero ohm resistors for direct connection to frame ground. The designer will need to perform different experiments to establish which option will satisfy his requirements best. A possible drawback with using zero Ohm resistors is the DC path between the far end and the near end, which may connect the two building grounds together. While there is an advantage of having the capacitors to cut the DC path; however, we have introduced AC impedance between the two grounds. In this case a capacitor value will have to be chosen depending on the predominant interference frequency. When the

cable shield is connected to the frame ground, the frame will need to be connected to an external ground source, such as a system chassis ground or earth ground, to dissipate the noise.

For the positive supply we recommend a plane that connects all the supply pins of the LIU. This supply plane should be connected with the lowest possible impedance to the major supply. It is advisable to void the positive supply under the coaxial connectors and the primary side of the transformers to avoid noise being coupled in the supply.

The differential termination resistors for the line-side input and output signals should be placed as close as possible to the chip. Also, the traces for each of the line-side differential pairs should be run as parallel, straight, and as close as possible to avoid any reflection caused by a variance in trace lengths between a differential pair. The traces should be kept on the top layer of the board, and the width of the traces should be adjusted to meet the characteristic impedance of the line. The preferred differential termination scheme is shown in Figure 3 below. The value of each resistor should equal one half of the total termination used for the pair, so that each half of the signal is seeing the correct termination value. The capacitor value should be 0.1uF.

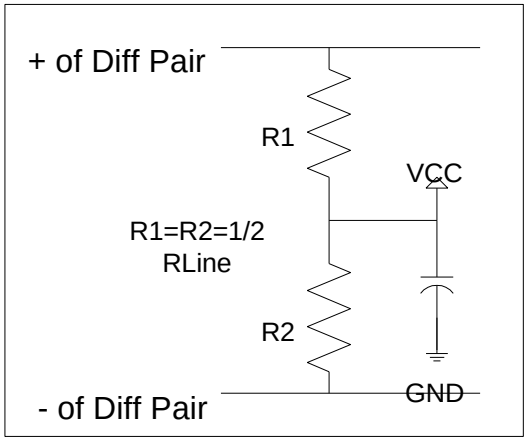

Figure 3. Recommended termination of a differential pair

Care should be taken when placing the RFO resistor. The RFO should be placed as close as possible to the chip and the trace to the resistor should remain on the top layer. Also, the LF capacitor should be placed close to the LIU.
To eliminate overshoot on the digital signals coming from the framer to the LIU, a series of 100 ohms resistors should be added to the TCLK, TPOS and TNEG signals. Placing a ground trace on each side of TCLK and RCLK will also help to reduce noise on the board.

For the LIU, decoupling capacitors should be implemented to help reduce noise. These capacitors should be located directly underneath the LIU on the bottom side of the board. The VCC and GND connections from the LIU should be made through vias, which are connected to the VCC and GND of the decoupling capacitors.

PERFORMING TESTS WITH DEMO BOARD

The general test setup using the demo board is show in figure 4. When remote loop back is enabled at pin 26 (floating), the receiver logical outputs (RCLK, RPOS, RNEG) connected to the transmitter logical inputs (TCLK, TPOS and TNEG). As a result, the received AMI signal is transmitted back to the test equipment. Monitoring bit error rate indicates the ability of the IC to receive and transmit the AMI signal without errors.

As show in Figure 5, 450 feet of 75 Ohm coaxial cable (type RG59B) plus resistive attenuation are used in the receive path to exercise the IC. The following tests are performed on the receiver.

BIT ERROR RATE TEST

The test equipment generates a pseudo-random pattern. This pattern is created using a shift register of N bits. A combination of 2**N-1 patterns of N bits is created in a random manner. This pattern is used to simulate live traffic on the AMI line. The following table shows the typical patterns to test the IC:

SPEED	RANDOM PATTERN	FIXED PATTERN
DS3	2**15-1	100100
STS-1	2**15-1	100100
E3	2**23-1	10001000

Table 6. Test patterns.

When running these patterns, the bit error ratio should be lower than 10^{-9}. The test is repeated for fixed patterns to exercise the IC for any pattern sensitivity.

JITTER TOLERANCE

Telecommunication equipment should be able to recover clock and correct data even if the AMI signal includes a certain amount of timing jitter. For this test, the test equipment adds jitter to the random AMI signal. For jitter at a set frequency, the jitter amplitude is slowly increased until bit errors are observed. This process is repeated at different frequencies. A plot of tolerated jitter amplitude vs. jitter frequency is made as show in Figures 8 and 9.

The system should tolerate jitter in excess of specified requirements. For bench test set up see Figure 7.

INTRINSIC JITTER

The jitter generated by the IC in the absence of any jitter on the transmitter logical input (TCLK, TPOS, TNEG) is minimal (see Figures 10 and 11). For the bench test set up see Figure 7.

JITTER TRANSFER FUNCTION

The IC should not cause any amplification of the system jitter, i.e., very small peaking should be observed in the jitter transfer function. This objective can be achieved by selecting the PLL filter components for an overdamped response. The test equipment adds jitter to the AMI signal received by the IC. Measuring the jitter transmitted by the IC in the remote loop back mode indicates the shape of the transfer function.

TRANSMITTER TESTS

The AMI pulse generated by the IC can be tested for its shape, amplitude and frequency contents over different lengths of cable. The demo board is usually placed in remote loop back this by leaving pin 28 floating. For bench test set up see Figure 5.

TRANSMITTER PULSE FREQUENCY CONTENTS

For an AMI signal with an “all ones” pattern, the transmitted signal should have a frequency spectrum with the main component at half of the bit rate. The signal power at the harmonics including the component at the bit rate should be at least 20 dB lower than the main component. A spectrum analyzer is used for this purpose. The measured power is for DS3 at 3.3V supply 4.9 dBm and the second harmonic is at most 35 dB lower, at 5.5 V. The supply output power is 5.2 dBm and the second harmonic is at most 35 dB lower.

TRANSMITTER PULSE AMPLITUDE

The pulse amplitude for a pattern of 100100… is measured at different cable lengths by connecting the end of the cable to the scope using a 75-Ohm adapter (PONOMA 4119 see figure 5). For E3 the transmitted pulse amplitude needs to be fairly exact (2Vp-p $\pm$ 10%) see figure 14. For DS3 and STS-1, the transmit amplitude may fall in a wide range of amplitudes from 0.72 to 1.7 Vp-p (see Figures 12 and 13). For STS-1 a pseudo random pattern is used and the output signal is matched against an Eye diagram as seen in Figures 15 and 16.

TRANSMITTER PULSE SHAPE

The shape of the signal at the end of a 75-Ohm cable is examined by comparing it to the published templates. The test setup is show in Figure 5. The program resident in the scope reads the transmitter waveform, scales it vertically, and plots it together with the published template masks. For DS3, the pulse shape should meet the mask for all cable lengths from zero to 450 feet. A typical pulse shape for the 78P7200L at the end of 450 feet of cable is show in Figure 12 and 13.

TRANSMITTER PULSE IMBALANCE

The AMI pulse generated by the IC includes pulses of both negative and positive polarities. Pulse imbalance is examined by inverting the negative pulse with the scope and overlaying it on a typical positive pulse. No significant imbalance is observed.

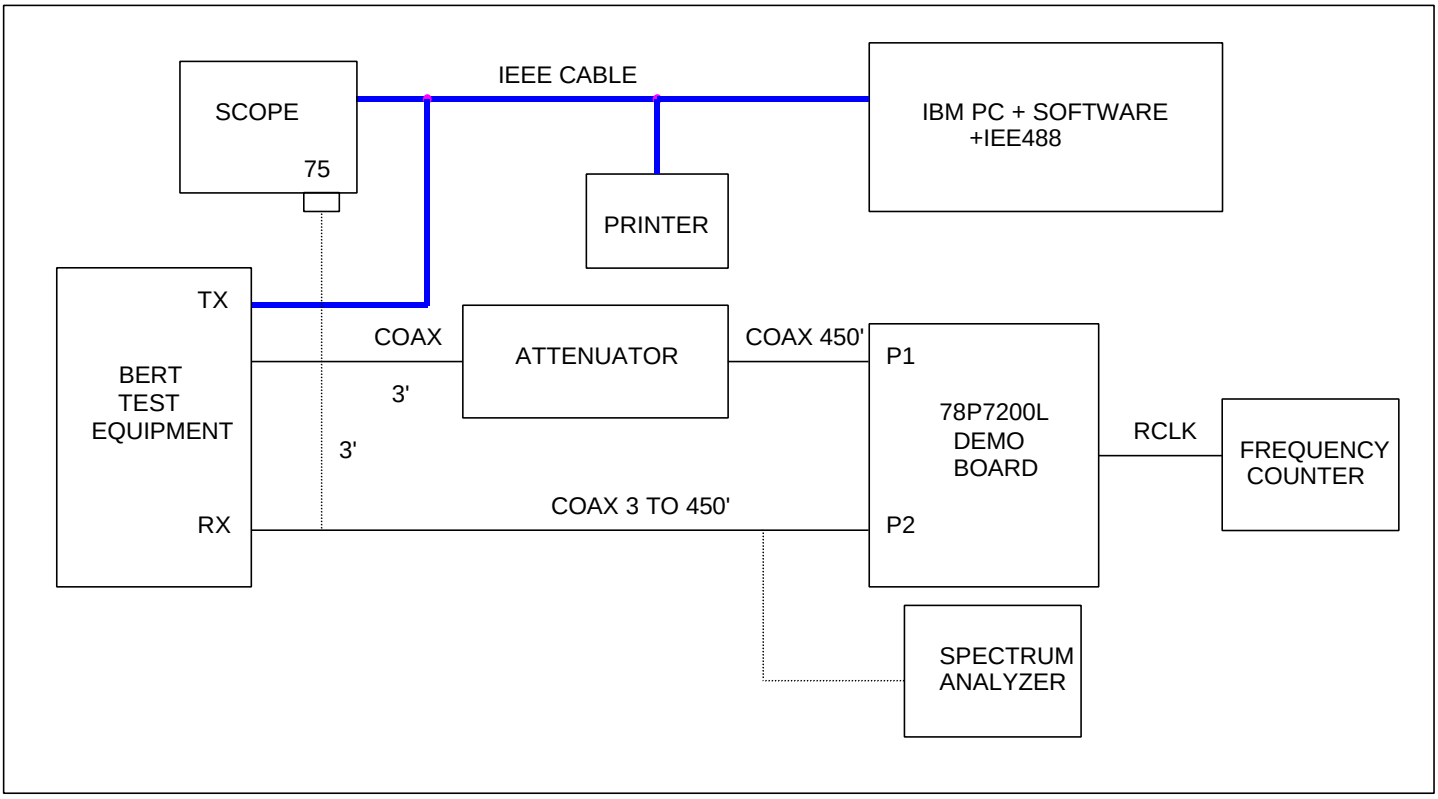

Figure 4. Test set up for performance testing

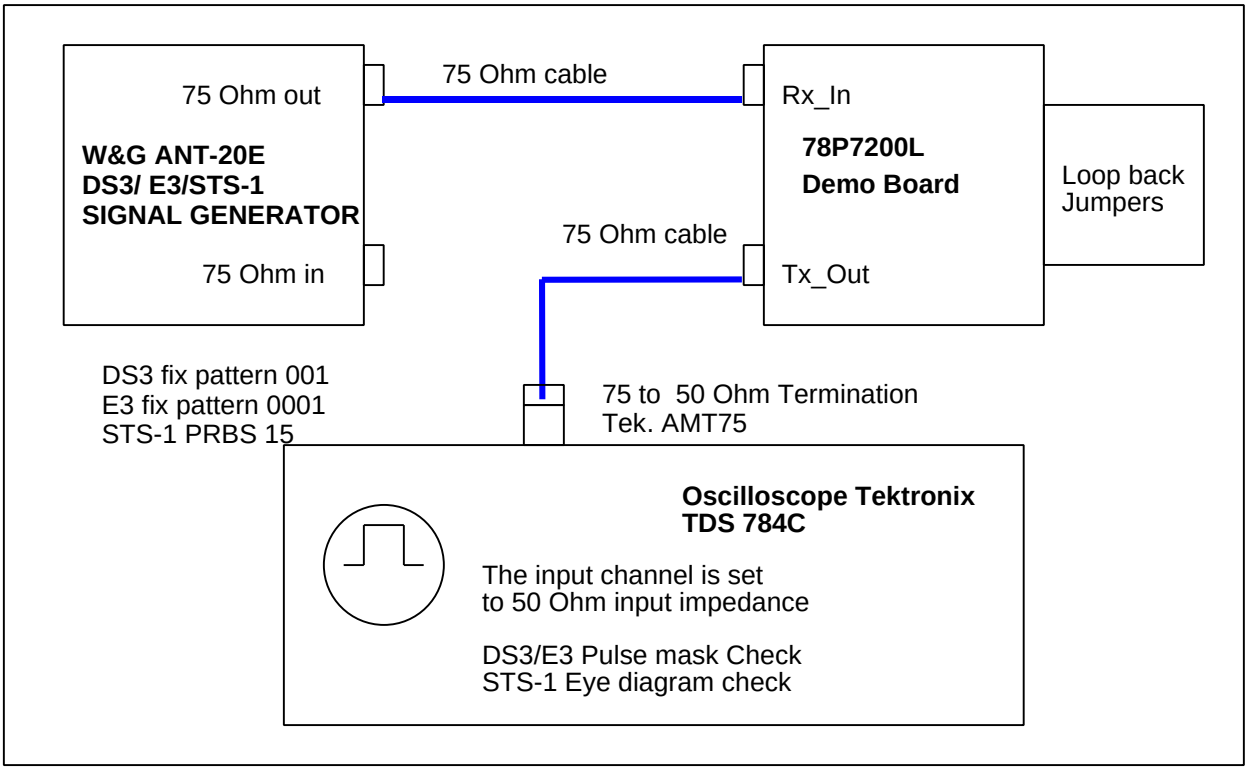

Figure 5. Test set up for pulse mask checking

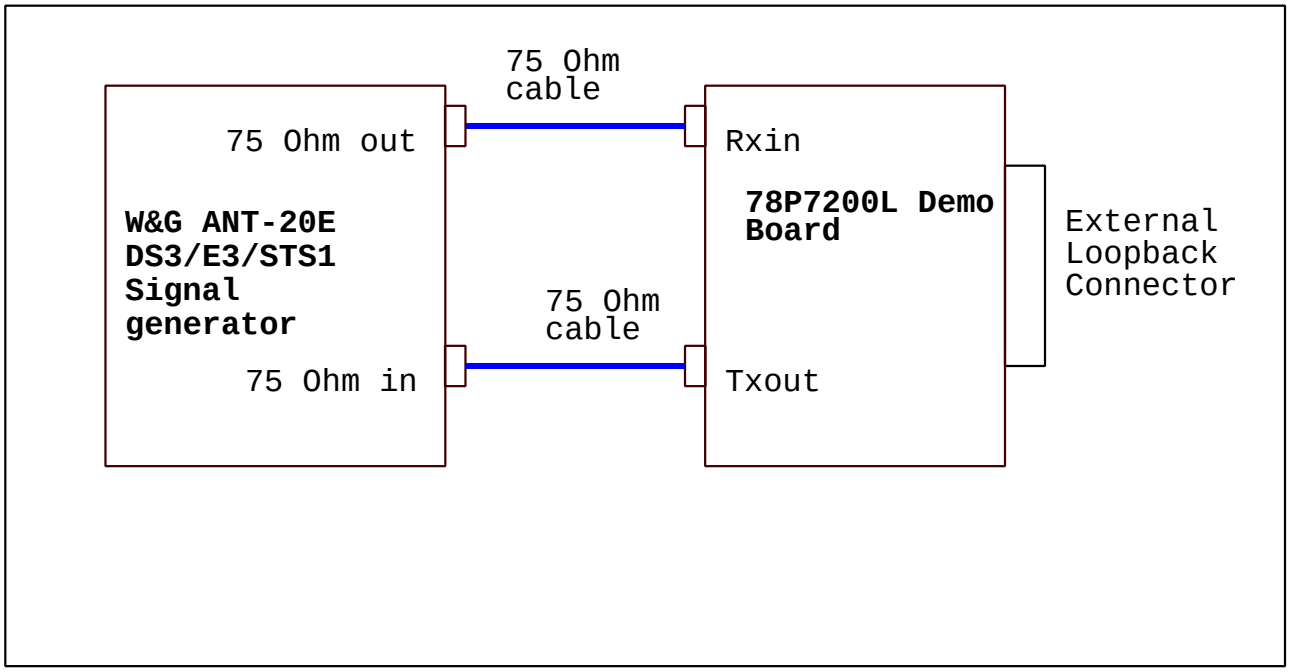

Figure 6. Test set up for Jitter Tolerance and Jitter Transfer Function

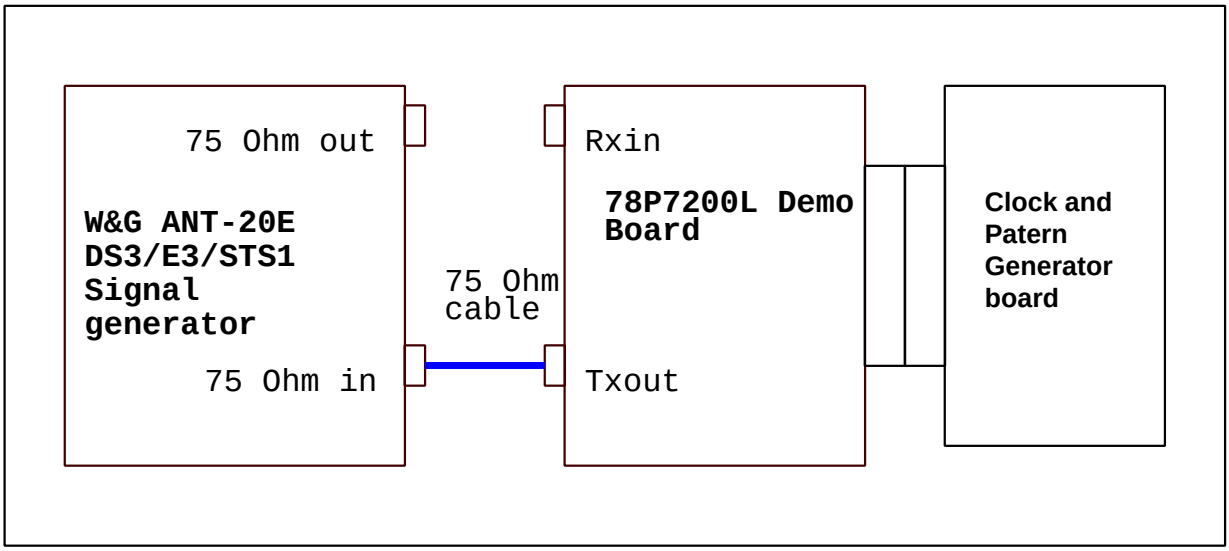

Figure 7. Test set up for Intrinsic Jitter measurement

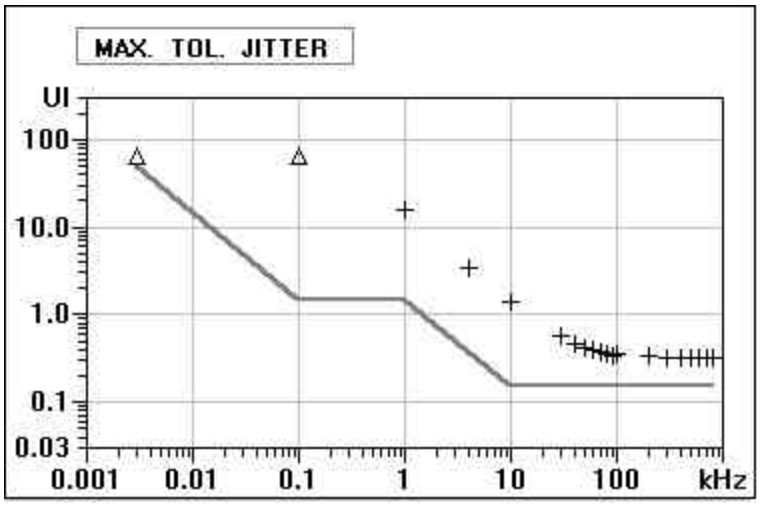

Figure 8. Jitter Tolerance Plot , E3 rate at 3V, 5.5V and 0 to 1035 Feet

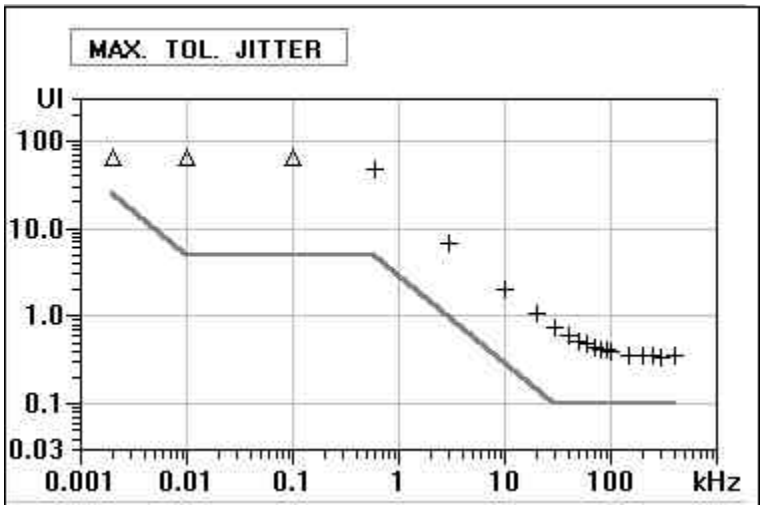

Figure 9. Jitter Tolerance Plot, DS3 rate at 3V, 5.5V and 0 to 450 Feet

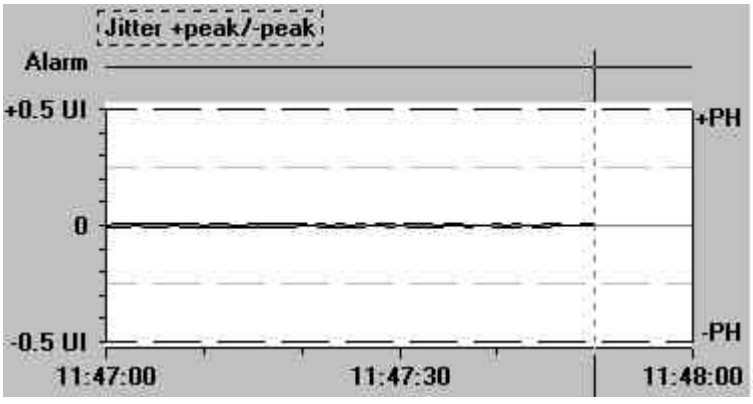

Figure 10. Intrinsic jitter peak to peak for all rates and supply voltages.

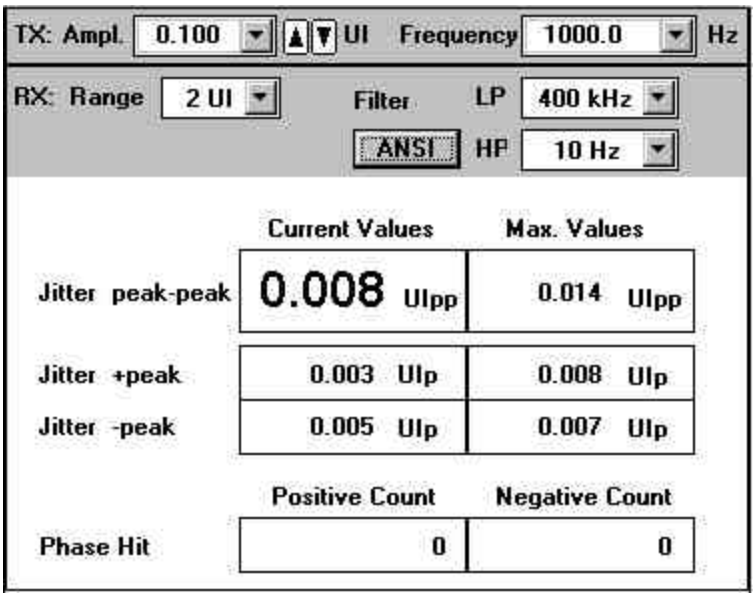

Figure 11. Intrinsic jitter table for all rates and supply voltages.

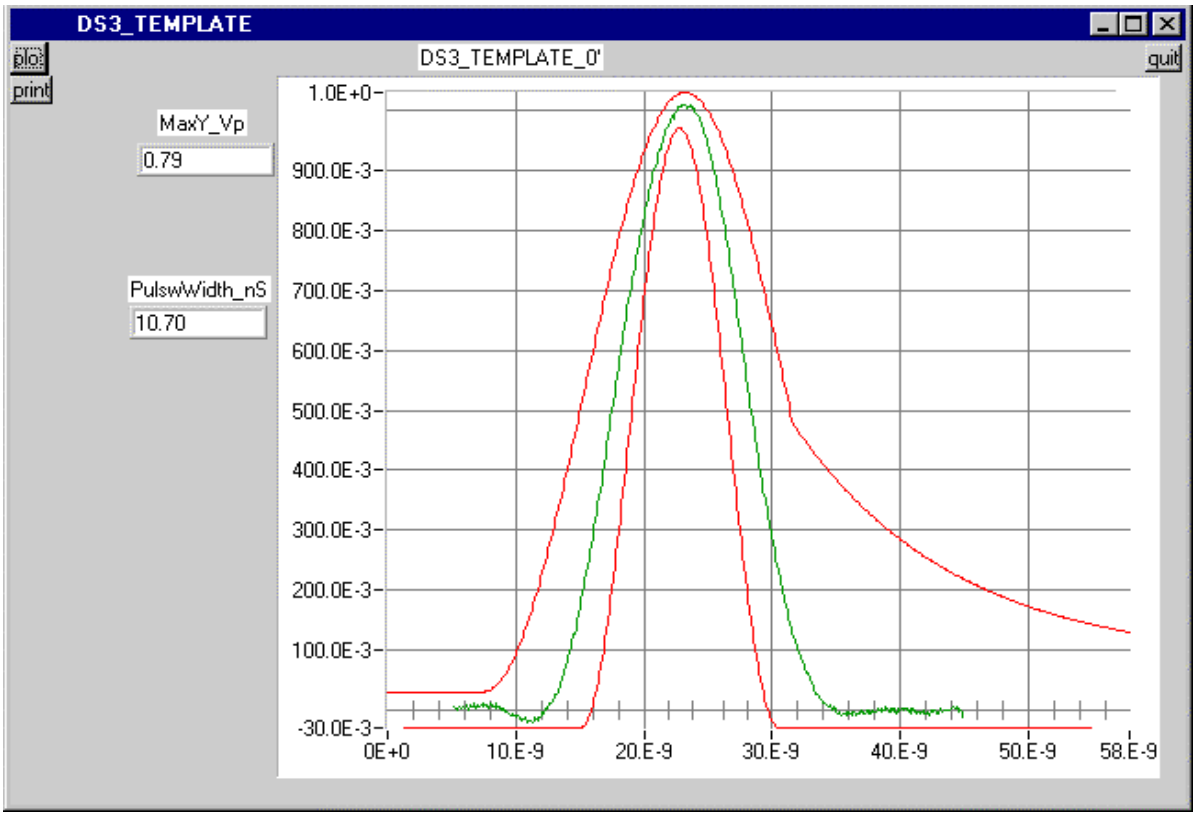

Figure 12. DS3 template at 0 feet of cable

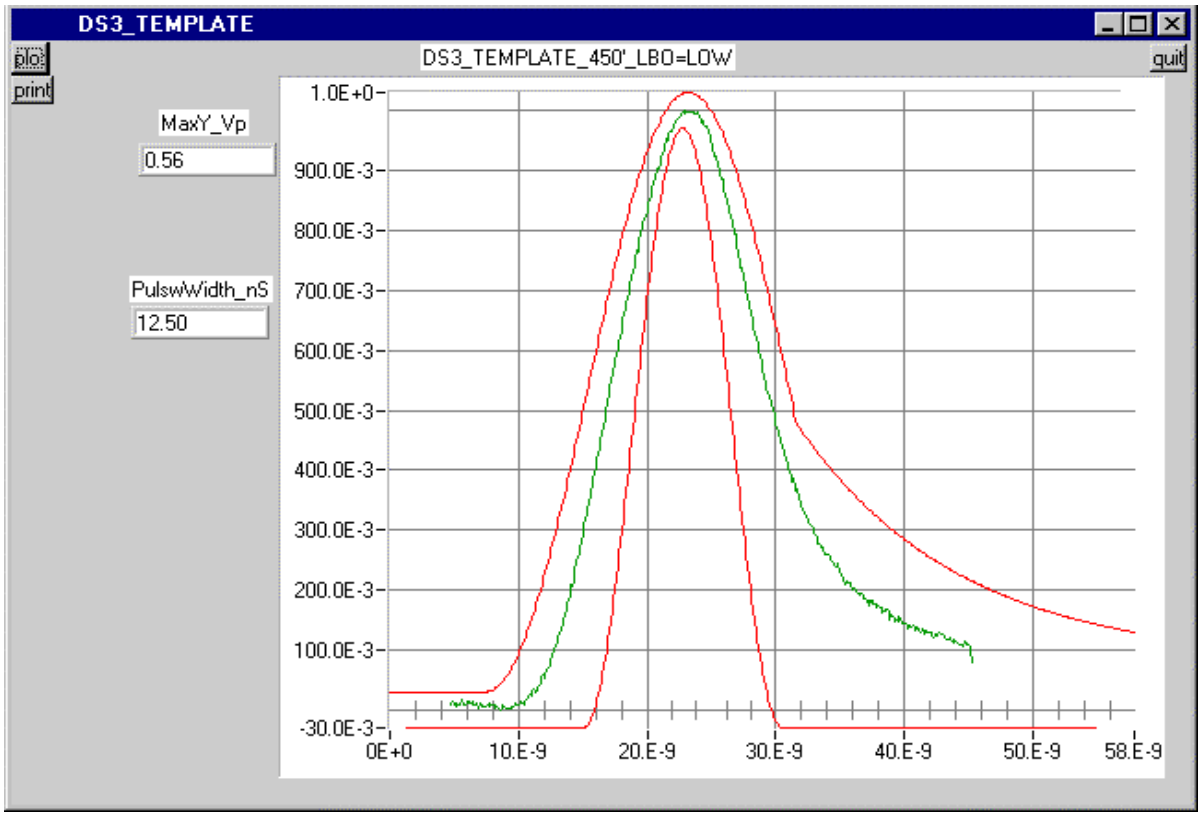

Figure 13. DS3 template at 450 feet of cable

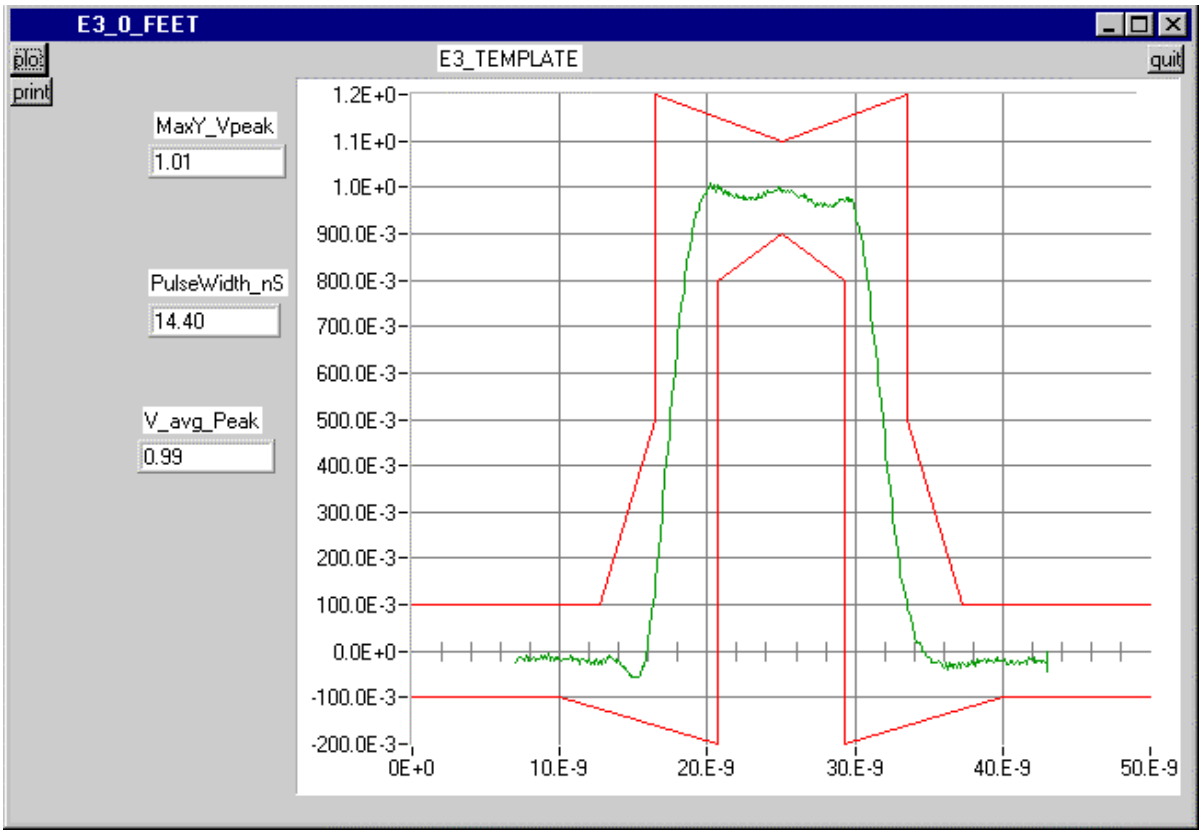

Figure 14. E3 template at 0 feet of cable

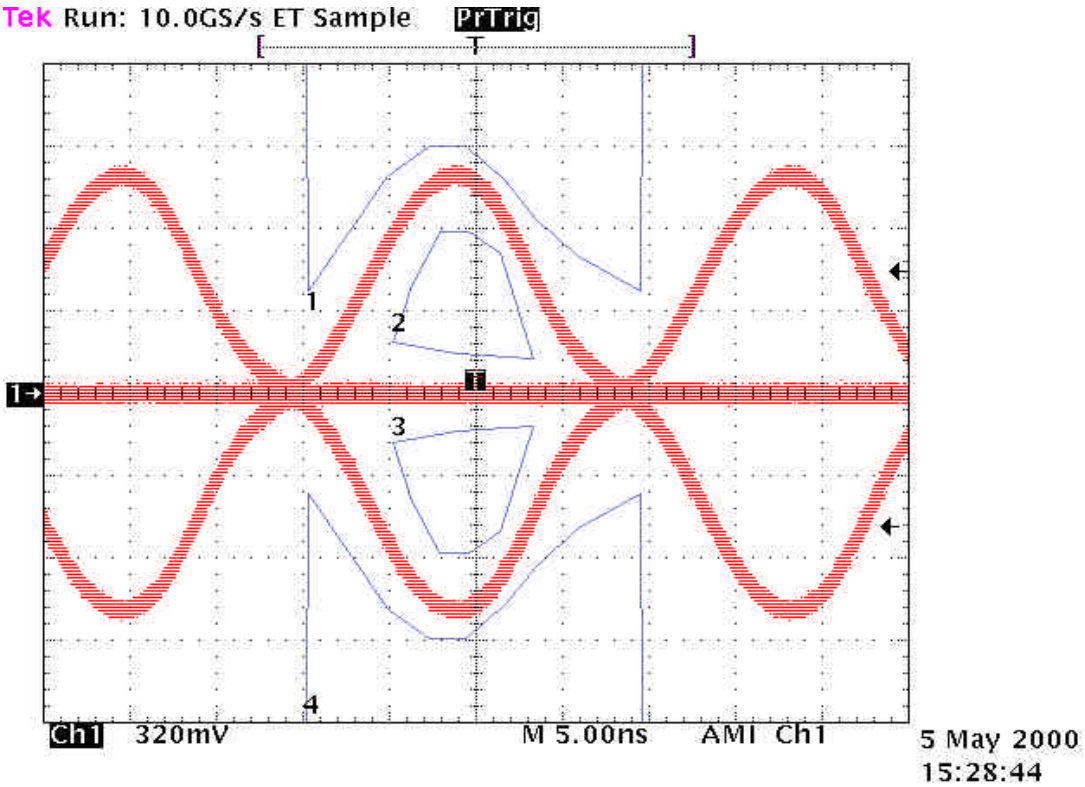

Figure 15. STS-1 Eye Diagram at 0 feet of cable

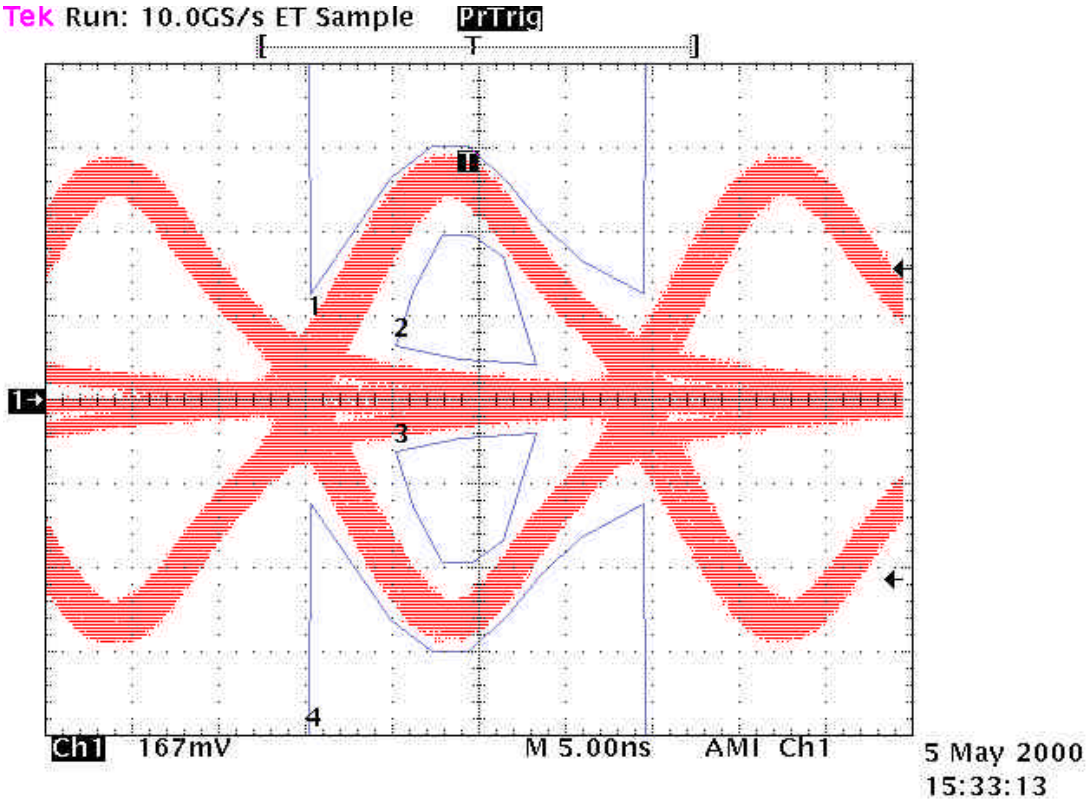

Figure 16. STS-1 Eye Diagram at 450 feet of cable LBO off.

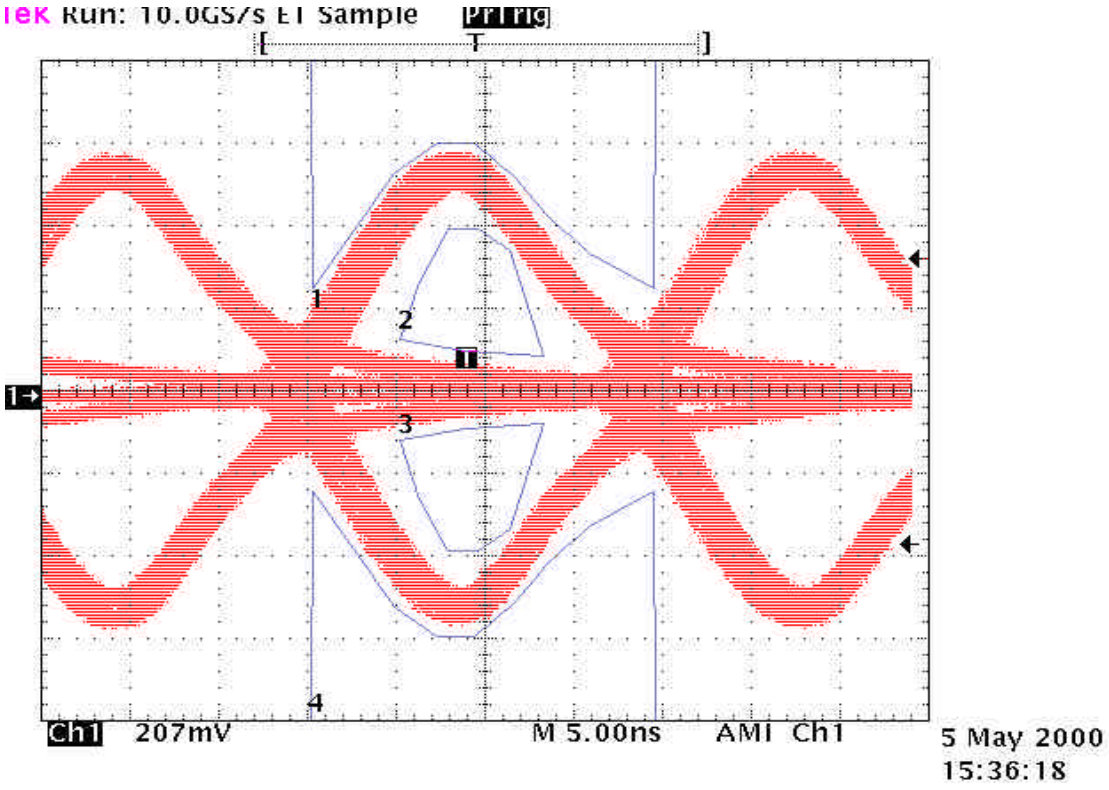

Figure 17. STS-1 Eye Diagram at 450 feet of cable LBO on.

SPEED	CABLE	S1-1	S1-2
DS3/STS1	L<225'	OPEN	OPEN
DS3/STS1	L>225'	CLOSED	OPEN
E3	All	CLOSED	CLOSED

COMPONENT	STS-1	DS3	E3
R5	4.53K	5.23K	6.81K

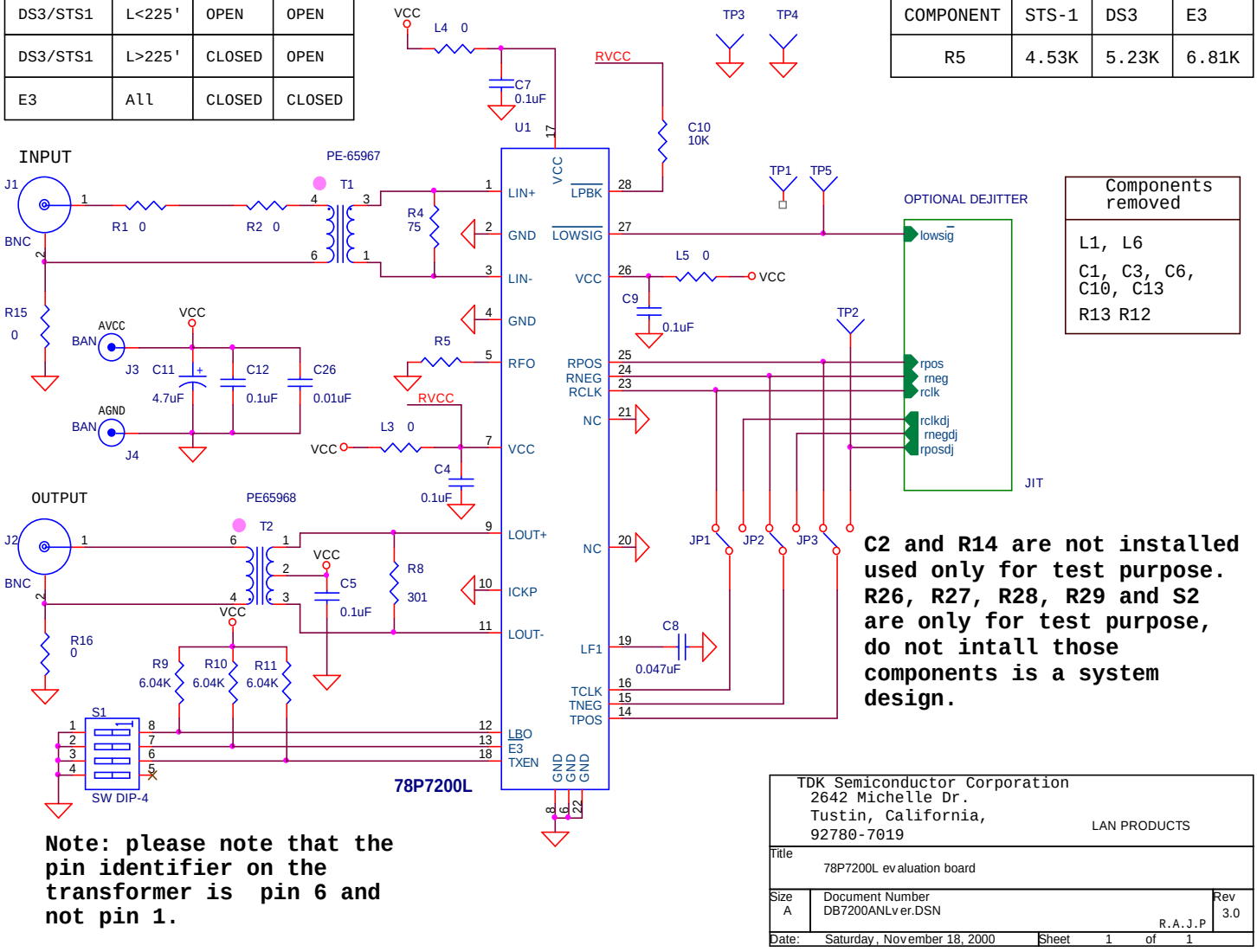

Figure 18. Demo Board Schematic of the 78P7200L-PLCC

78P7200L 28-pin PLCC evaluation board
Revised: Monday, April 24, 2000
Revision: 1.0

TDK Semiconductor Corporation
2642 Michelle Dr. Tustin CA. USA
WAN PRODUCTS

Bill Of Materials

Item	Quantity	Reference	Part	Manufacturer	Part #	Size	PRECISION
1	5	C4, C5, C7,C9,C12	0.1uF	TDK	C3216X7R1E104M	CC1206	20%
2	1	C26	0.01uF	TDK	C3216X7R1E103M	CC1206	20%
3	1	C8	0.047uF	TDK	C3216X7R1E473K	CC1206	10%
4	1	C11	4.7uF	PANASONIC	ECS-T1EC475R	CC1812	20%
5	2	J1, J2	BNC 75Ω	AMPHENOL	31/5329		
6	5	L3, L4, L5, R1, R2	0	PANASONIC	ERJ-8ENF0	CC1206	
7	1	R4	75	PANASONIC	ERJ-8ENF75	CC1206	1%
8	1	R8	301	PANASONIC	ERJ-8ENF301	CC1206	1%
9	4	R9,R10,R11,C10	10K	PANASONIC	ERJ-8GEYJ10K	CC1206	5%
10	1	R5a	4.53K	PANASONIC	ERJ-8ENF4.53K	CC1206	1%
11	1	R5b	5.23K	PANASONIC	ERJ-8ENF5.23K	CC1206	1%
12	1	R5c	6.81K	PANASONIC	ERJ-8ENF6.81K	CC1206	1%
13	1	T1	PE65968	PULSE	PE 65968	SMT	3%
14	1	T2	PE65969	PULSE	PE 65969	SMT	3%
15	1	U1	78P7200L	TDK	78P7200L-IH	28-PLCC	

Table 8. Bill Of Materials.