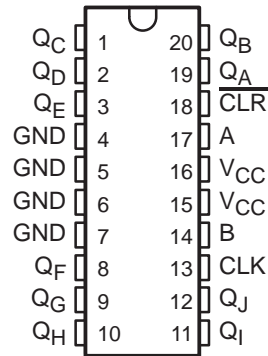


# 74ACT11898 10-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SCAS144 – OCTOBER 1990 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Fully Synchronous Data Transfers
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE  
(TOP VIEW)



## description

The 74ACT11898 features AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level on the rising edge of the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low provided the minimum setup and hold time requirements are met. Clocking occurs on the low-to-high transition of the clock input.

The 74ACT11898 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS				OUTPUTS			
$\overline{\text{CLR}}$	CLK	A	B	$Q_A$	$Q_B$	...	$Q_J$
L	X	X	X	L	L		L
H	L	X	X	$Q_{A0}$	$Q_{B0}$		$Q_{J0}$
H	$\uparrow$	H	H	H	$Q_{AN}$		$Q_{IN}$
H	$\uparrow$	L	X	L	$Q_{AN}$		$Q_{IN}$
H	$\uparrow$	X	L	L	$Q_{AN}$		$Q_{IN}$

H = high level (steady state)

X = irrelevant (any input, including transitions)

$\uparrow$  = transition from low to high level

$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{J0}$  = the level of  $Q_A$ ,  $Q_B$ ,  $Q_J$  respectively, before the indicated steady-state input conditions were established.

$Q_n$ ,  $Q_{in}$  = the level of  $Q_A$  or  $Q_J$  before the most recent  $\uparrow$  transition of the clock; indicates a one-bit shift.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

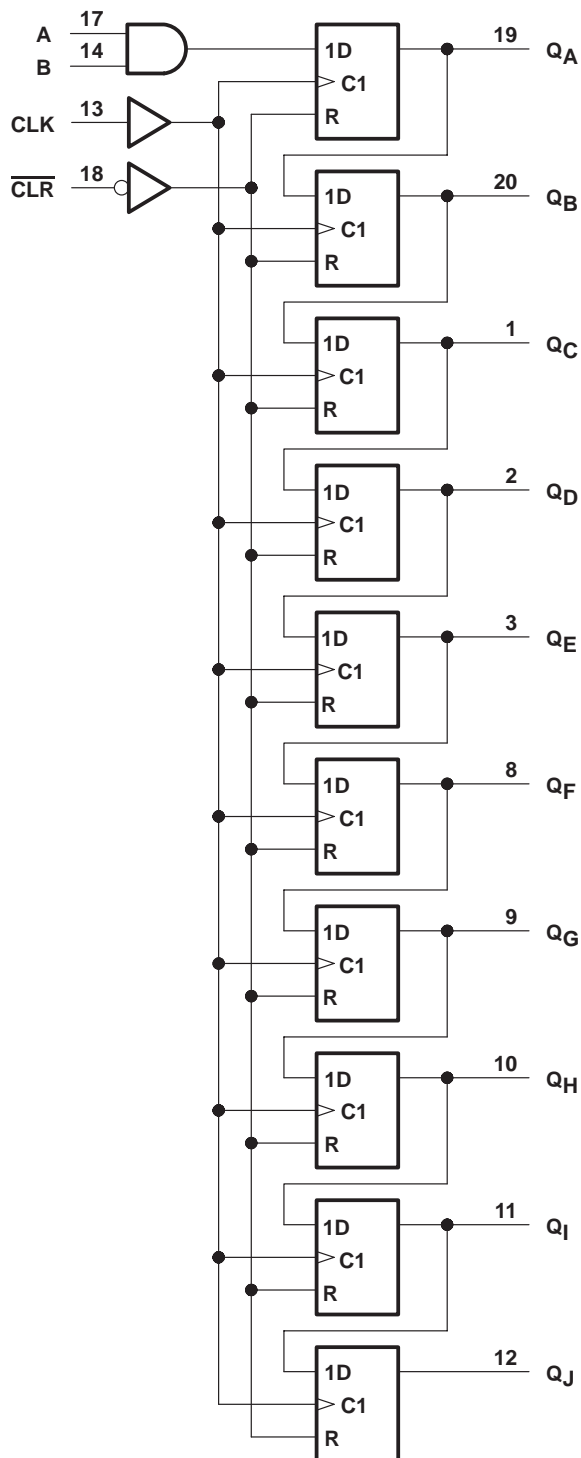


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1993, Texas Instruments Incorporated

## SCAS144 – OCTOBER 1990 – REVISED APRIL 1993

**logic diagram (positive logic)**



2-2

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND	±250 mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

**recommended operating conditions (see Note 2)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24	mA
$I_{OL}$	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	$I_{OH} = -75 \text{ mA}^\ddagger$	5.5 V				3.85		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	$I_{OL} = 24 \text{ mA}$	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	$I_{OL} = 75 \text{ mA}^\ddagger$	5.5 V					1.65	
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5	μA
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	μA
$\Delta I_{CC}^\S$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V			0.9		1	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		4				pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to  $V_{CC}$ .

# 74ACT11898

## 10-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SCAS144 – OCTOBER 1990 – REVISED APRIL 1993

**timing requirements over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
$f_{\text{clock}}$	Clock frequency		0	40	0	40	ns
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	4.5		4.5		ns
		CLK high or low	12.5		12.5		
$t_{\text{su}}$	Setup time before CLK $\uparrow$	Data	10		10		ns
		$\overline{\text{CLR}}$ inactive	1.5		1.5		
$t_h$	Hold time, data after CLK $\uparrow$		0		0		ns

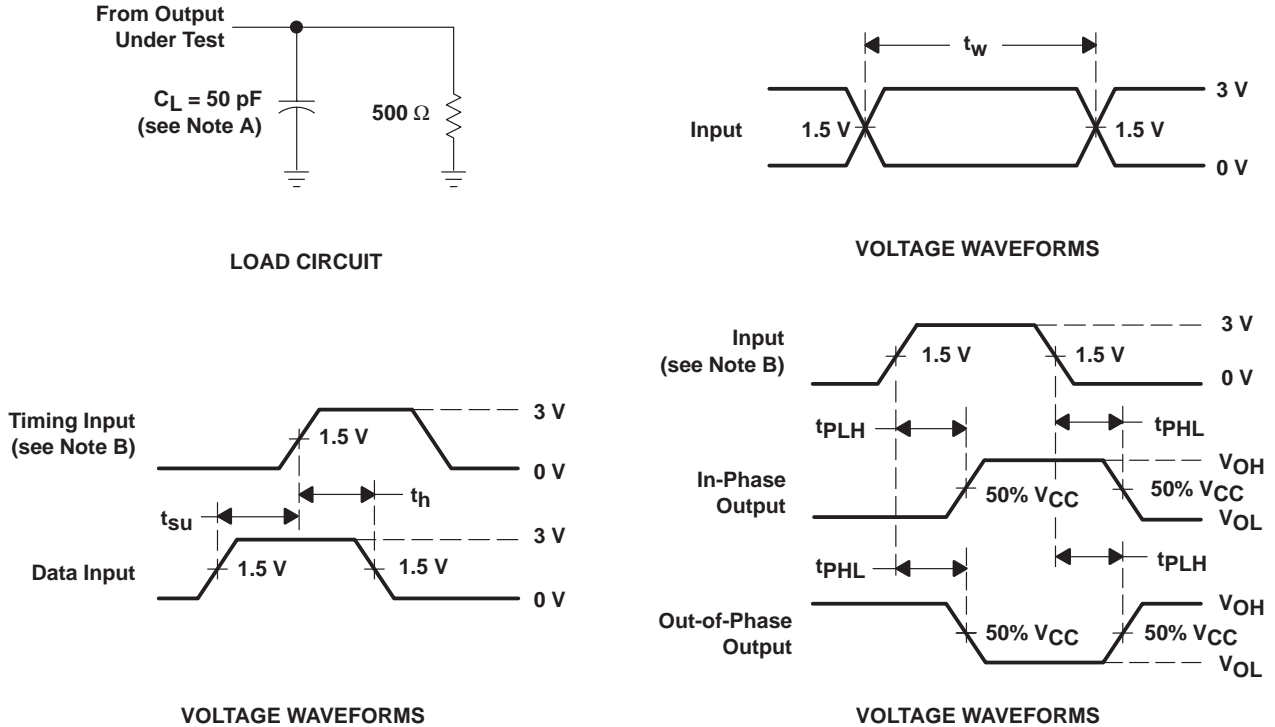
**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			20	65		40		MHz
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	4.6	6.7	11.1	3.8	12.1	ns
$t_{\text{PLH}}$	CLK	Any Q	4.1	5.5	8.8	2.7	9.7	ns
$t_{\text{PHL}}$			4.4	6.3	9.4	3.1	10.6	

**operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	117	pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .

C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.