TDK SEMICONDUCTOR CORP.

TSC 78Q8378
3V, 5V PC Card
Multi-function Ethernet Combo

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DESCRIPTION

The TSC 78Q8378 is a highly integrated Ethernet and peripheral port combo IC for use in Multi-function PC Card applications and can operate with a power supply of 3.3V or 5V. It is compliant with PC Card Standard (Multiple Function) as well as backwards compatible to PCMCIA 2.X specifications. It contains a Media Access Controller (MAC), a 10 Mbit/s Manchester encoder/decoder (ENDEC), a 10BaseT transceiver, a multi-function memory card bus interface (PC Card), a peripheral port interface, and an Attachment Unit Interface (AUI). This level of integration allows the user to implement a multi-function PC Card for 10BaseT and Fax/Modem by using the TSC 78Q8378, a modem chip set, external memory, and some passive components. The internal bus interface circuit allows connection to a Multi-function PC Card V3.0 bus without other external components. The PC Card bus decoding logic can be bypassed for connection to other bus types. The TSC 78Q8378 connects to twisted-pair media via line transformers through the on-chip transceiver circuit. Connections to other media such as coaxial cable is made through the AUI port to an external transceiver, such as the TSC 78Q8392L Ethernet Coax Transceiver.

The TSC 78Q8378 has a sophisticated power management capability with three different operating modes allowing the user to maximize power savings, making it ideal for use in PC Card applications. During normal operation, the IC monitors its own action and shuts down the circuits that are not being used, resulting in the lowest possible operating power. It also has a standby mode which leaves only the oscillator running, and a full shutdown mode which also turns off the oscillator.

An intelligent Buffer Manager is controlled by the host read, host write, receive and transmit pointers, and the TSC 78Q8378 manages the pointers internally without any host intervention. The device interleaves access to the buffer memory so that access from the host and from the network media seem to operate concurrently. Big and little endian byte orderings make for simple bus interface to all standard microprocessors.

The TSC 78Q8378 is available in a 120-lead thin quad flat pack (TQFP) and can operate with a power supply of 3.3 volts or 5 volts.

FEATURES

- **Single-chip solution for 10Base T/PC Card designs with a second peripheral interface**
- **Operation at 3.3V or 5V**
- **Register compatible to the TSC 78Q8373**
- **Programmable full duplex operation**
- **Integrated 10BaseT transceiver:**
  - **Programmable/automatic selection of twisted pair (RJ45) or AUI port**
  - **Receive polarity detection/correction on twisted-pair inputs**
- **Manchester Encoder/Decoder circuit**
- **AUI port for connection to 10Base-2/5 transceiver or AUI cable**
- **PC Card Standard (multiple function spec) V3.0 compliant.**
- **Protocol Controller compliant with IEEE 802.3 and Ethernet 2.0**
  - **Supports packet indication and ring indication functions**
- **Advanced Buffer Manager architecture:**
  - **Automatic management of all pointers**
  - **Allows "simultaneous" access to data in buffer memory by both the network and host**
  - **High-speed received packet skip**
- **Configurable Buffer Memory for design flexibility:**
  - **Two-bank transmit buffer in 2, 4, 8 or 16 Kbyte sizes**
  - **Ring-structure receive buffer from 4 to 62 Kbytes**
- **Software-configurable system bus structure:**
  - **Compatible with major microprecessors**
  - **8 or 16-bit wide data path communications with hosts**
  - **Supports both dual interrupt and shared interrupt schemes.**
  - **Configurable I/O base address for LAN and peripheral port functions with 10-bit address decode**

FEATURES (continued)

- External CIS memory support: Parallel EEPROM or Flash memory
- Power management options:
  - Intelligent power mode automatically shuts off unused circuitry
  - Standby mode reduces power while not in operation
  - Full shutdown mode offers maximum power savings
- Available in 120-lead TQFP package

FUNCTIONAL DESCRIPTION

The TSC 78Q8378 consists of six major blocks as shown in Figure 1.

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- Host/PC Card Interface
- Manchester ENDEC
- Twisted Pair Transceiver
- Power Management

BUFFER MANAGER

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration, this makes the TSC 78Q8378 a high performance LAN controller.

The buffer memory is divided into two portions: transmit memory portion and receive memory portion. The transmit memory portion can be partitioned into 2K, 4K, 8K or 16 Kbyte buffer sizes. There is only one transmit bank if a 2 KB transmit buffer size is selected. If the transmit buffer size is greater than 2 KB, then the transmit buffer is configured into two banks of equal size. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be transmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62 KB depending on the buffer memory configuration which has a range of 8K to 64 KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from 4 sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the TSC 78Q8378 will assert a 'not ready' handshake to the host while servicing the Transmitter and/or Receiver. The TSC 78Q8378 arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operations appear to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the TSC 78Q8378 can potentially be receiving data from the medium and loading it into the receive buffer (if the TSC 78Q8378 is in a loop back mode, if self-reception occurs or if the 8378 is in full duplex mode).

DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ANSI/IEEE 802-3 CSMA/CD protocol. It consists of a Transmitter, a Receiver and CRC logic (which is shared by both transmit and receive operations). Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

HOST/PC CARD INTERFACE

The Host Interface (HIF) provides connection to the host system. It consists of the various registers, DMA circuits and ready logic. Both word and byte interfaces are supported as well as big endian and little endian data ordering. Host access to the buffer memory is through BMR8 (and BMR9). Reading from BMR8 will read a byte or word from the receive buffer and writing to BMR8 will write a byte or word to the transmit buffer. The ready logic is capable of delaying host access to the buffer memory with a time-out mechanism. Both single and burst DMA transfer modes are supported.

PC CARD MULTI-FUNCTION INTERFACE

The PC Card interface has been extended to support multi-function card capability, in particular, LAN and Modem combination. The second peripheral port interface is a general purpose interface. Two additional features have been added to support modem functions. The ring indication function is available in the Status Change Register and a digital speaker signal is controlled through the TSC 78Q8378. Two sets of Function Configuration Registers (FCR) (used to be called Card Configuration Registers - CCR on a single function card) are provided so that each function can be configured independently. The chip includes the function of mapping and decoding the I/O range for the LAN registers and the peripheral port. The TSC 78Q8378 is also capable of handling multiple interrupts from two sources by saving the second interrupt and generating it later according to the PC card Multifunction specification.

It also supports decoding for the external CIS memory (both ROM and Flash types). The TSC 78Q8378 pinout has been defined to minimize criss-crossing connections to the PC Card connector. This allows for a cost effective 2-layer PCB design.

FULL DUPLEX OPERATION

The TSC 78Q8378 now includes support for Full Duplex operation (10 BaseT only), making the line throughput to 20 Mbit/s. In this mode, the collision detection, SQE generation and “natural” loopback of the TP transceiver are disabled.

MANCHESTER ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to either the twisted-pair transceiver block or to the Attachment Unit Interface (AUI) driver, depending on which block is

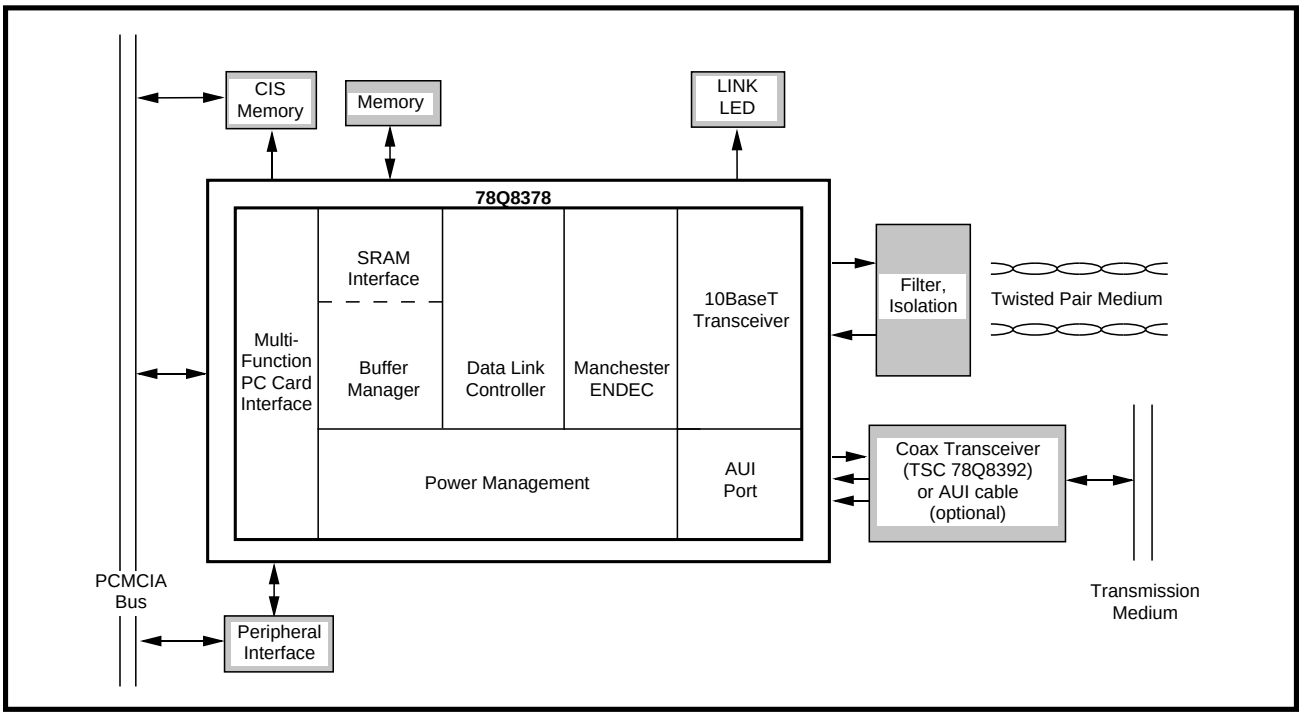


FIGURE 1: System Diagram

MANCHESTER ENDEC (continued)

active. The decoder section performs three functions: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at the end of reception and during idle to save power. Jitter of up to ±18 ns can be tolerated by the decoder. This block also translates a 10 MHz collision signal to a logic-level signal before sending it to the DLC block if the AUI port is selected.

TWISTED PAIR TRANSCEIVER

The on-chip Twisted Pair module consists of a number of functions. It has a smart squelch circuitry to determine valid data present on the differential receive inputs TPIP/TPIN. Its transmit and pre-distortion drivers connect to the twisted pair network via the summing resistors and transformer/filter. The link detector/ generator circuitry checks the integrity of the cable connecting the two twisted pair MAUs. Collision, jabber and SQE are also incorporated.

POWER MANAGEMENT

One very useful and important feature that the TSC 78Q8378 offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

Pin Assignment Table - 120-Pin TQFP

PIN #	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	A0	I	31	RD8	IO4	61	RA12	O4	91	DON	AO
2	A1	I	32	RD9	IO4	62	RA14	O4	92	DOP	AO
3	A2	I	33	RD10	IO4	63	$\overline{\text{RWE}}$	O4	93	VSSA	G
4	A3	I	34	RD11	IO4	64	RA13	O4	94	RBIAS	R
5	A4	I	35	RD12	IO4	65	RA8	O4	95	VDDA	P
6	A5	I	36	RD13	IO4	66	RA9	O4	96	TPIN	AI
7	A6	I	37	RD14	IO4	67	RA11	O4	97	TPIP	AI
8	A7	I	38	RD16	IO4	68	$\overline{\text{ROE}}$	O4	98	CIN	AI
9	VDDIO	P	39	VSSIO	G	69	RA15	O4	99	CIP	AI
10	A8	I	40	RD0	IO4	70	VSSIO	G	100	DIN	AI
11	A9	I	41	RD1	IO4	71	OSCI	CI	101	DIP	AI
12	FCRA	I	42	RD2	IO4	72	OSCO	O	102	VSSC	G
13	VSSC	G	43	RD3	IO4	73	VDDC	P	103	VDDC	P
14	$\overline{\text{WE}}$	I	44	RD4	IO4	74	$\overline{\text{MCS}}$	O4	104	LEDLT	OD16
15	$\overline{\text{IOWR}}$	I	46	RD5	IO4	75	$\overline{\text{MPD}}$	O4	105	$\overline{\text{CISCS}}$	O4
16	$\overline{\text{IORD}}$	I	46	RD6	IO4	76	MPD	O4	108	D10	IO4
17	$\overline{\text{OE}}$	I	47	RD7	IO4	77	$\overline{\text{MRST}}$	O4	107	D2	IO4
18	$\overline{\text{CE2}}$	I	48	VSSIO	G	78	MRST	O4	108	D9	IO4
19	$\overline{\text{CE1}}$	I	49	$\overline{\text{RCS0}}$	O4	79	MRI	SI	109	D1	IO4
20	VSSIO	G	50	$\overline{\text{RCS1}}$	O4	80	MSI	SI	110	D8	IO4
21	D15	IO4	51	VDDIO	P	81	MINT	I	111	D0	IO4
22	D14	IO4	52	RA10	O4	82	MRDY	I	112	VSSIO	G
23	D7	IO4	53	RA0	O4	83	CB	O4	113	$\overline{\text{IOIS16}}$	04
24	D13	IO4	54	RA1	O4	84	RRST	O4	114	$\overline{\text{STSCHG}}$	O4
25	D6	IO4	55	RA2	O4	85	VSST	G	115	$\overline{\text{SPKR}}$	O4
26	D12	IO4	56	RA3	O4	86	TPDN	AO	116	$\overline{\text{REG}}$	I
27	D5	IO4	57	RA4	O4	87	TPDP	AO	117	$\overline{\text{INPACK}}$	O4
28	D11	IO4	58	RA5	O4	88	TPON	AO	118	$\overline{\text{WAIT}}$	O4
29	D4	IO4	59	RA6	O4	89	TPOP	AO	119	RESET	SI
30	D3	IO4	60	RA7	O4	90	VDDT	P	120	$\overline{\text{IREQ}}$	O4

Legend:

TYPE	Description	TYPE	Description	TYPE	Description
I	Input (TTL level)	O4	Output with IOL = 4 mA	P, G	Power Ground
CI	CMOS level Input	OD16	Output Open Drain with IOL = 16 mA	R	Resistor to analog ground (20K ± 1%)
SI	Schmitt trigger Input	IO4	Input (TTL level) & Output with IOL = 4 mA		
AI	Analog Input	AO	Analog Output		

PIN DESCRIPTION

HOST BUS INTERFACE - PC CARD BUS

NAME	TYPE	DESCRIPTION
RESET	–	RESET (hardware). Active high. This pin resets the internal LAN function and the modem function by asserting MRST and $\overline{\text{MRST}}$. It also clears the Function Configuration Registers (FCR) including the EnFn bits in the Configuration Option Registers (COR) of both functions thus placing the TSC 78Q8378 in an unconfigured (Memory-Only Interface) state.
$\overline{\text{IOWR}}$	I	I/O WRITE. This pin is an active low input that enables a write operation by the host to the TSC 78Q8378 internal LAN registers or the modem function. The $\overline{\text{REG}}$ signal and at least one of $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ must also be active for the I/O write to take place. The TSC 78Q8378 will not respond to the $\overline{\text{IOWR}}$ signal until it has been configured for I/O operation by the host.
$\overline{\text{IORD}}$	–	I/O READ. This is an active low input that enables a read operation by the host from the TSC 78Q8378 LAN registers as well as from the modem function. The $\overline{\text{REG}}$ signal and at least one of $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ must also be active for the I/O read to take place. The TSC 78Q8378 will not respond to the $\overline{\text{IORD}}$ signal until it has been configured for I/O operation by the host.
$\overline{\text{CE1}}$, $\overline{\text{CE2}}$	I	CHIP ENABLE. An active low, input signals as the chip select for the TSC 78Q8378. The $\overline{\text{CE1}}$ enables the even-numbered-address bytes and the $\overline{\text{CE2}}$ enables the odd-numbered-address bytes. The $\overline{\text{CE2}}$ is only used by the LAN function when it is programmed in word mode and not used for attribute memory access.
FCRA	–	FUNCTION CONFIGURATION REGISTER ADDRESS. This pin connects to the PC Card higher address bit. A high (together with $\overline{\text{REG}}$ activation) on this pin selects the internal FCR (Function Configuration Registers) and a low selects the external CIS (Card Information Structure) memory.
$\overline{\text{OE}}$	I	OUTPUT ENABLE. An active low, input signal used to read data from the internal FCR (Function Configuration Registers) and from the external CIS Attribute Memory (through the activation of $\overline{\text{CISCS}}$). This pin needs also to be connected to the output enable of the external memory.
$\overline{\text{WE}}$	I	WRITE ENABLE. An active low, input signal used to write data to the internal FCR (Function Configuration Registers) and to the external CIS Attribute Memory (through the activation of $\overline{\text{CISCS}}$). This pin needs also to be connected to the write enable of the external memory.
$\overline{\text{REG}}$	–	ATTRIBUTE MEMORY SELECT. When this signal is active (low), it signifies access from or to the Attribute Memory (if $\overline{\text{OE}}$ or $\overline{\text{WE}}$ are active) or the I/O space (if $\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ are active). Attribute Memory is generally used to record card capacity and other configuration and attribute information. This includes the standardized FCR (Function Configuration Registers) which is located internal to the TSC 78Q8378. When Attribute Memory is accessed, only data signals D[0:7] are valid and signals D[8:15] shall be ignored.
A[0:9]	–	ADDRESS BUS. Used for Function Configuration Registers (FCR) selection, CIS memory selection and I/O decoding of both functions.

HOST BUS INTERFACE - PC CARD BUS (continued)

The following output signals are inactive (high) until the TSC 78Q8378 is configured for I/O mode.

PIN	TYPE	DESCRIPTION
D[0:15]	I/O	DATA BUS. A bi-directional, tri-state bus. The combinations of $\overline{CE1}$, $\overline{CE2}$ and A0 control the portion of the bus that is being utilized. A[0:3] and RBNK1,0 (DLCR7<3:2>) select the set of internal registers for access.
$\overline{WAIT}$	O	WAIT. An active low output that is asserted to delay completion of the current I/O read or write operation. It is only used by the LAN function and not by the modem function. This signal will only be active after the TSC 78Q8378 is configured for I/O mode.
$\overline{INPACK}$	O	INPUT ACKNOWLEDGE. This active low output signal is asserted when the TSC 78Q8378 is selected and it can respond to an I/O read cycle requested by the host. This signal is used by the host to control the enable of any input data buffer between the card and the CPU. This signal will only be active after the TSC 78Q8378 is configured for I/O mode.
$\overline{IOIS16}$	O	I/O IS 16 BIT. This active low output signal is asserted when the TSC 78Q8378 LAN function is configured for word transfer to indicate to the host that it is capable of 16-bit access. For modem function access, this pin remains high. This signal will only be active after the TSC 78Q8378 is configured for I/O mode.
$\overline{IREQ}$	O	INTERRUPT REQUEST. This signal is available only after the TSC 78Q8378 is configured for I/O mode. The TSC 78Q8378 supports multiple functions interrupt scheme as outlined by the PC Card Multiple Function Spec and both Pulsed-and Level-Mode Interrupt as selected by the LevIREQ register bit in the COR (Configuration Operation Register).
$\overline{SPKR}$	O	SPEAKER. This signal is held inactive (i.e., high) until the TSC 78Q8378 is configured for I/O mode. It provides a single-amplitude, on-off, binary audio waveform intended to drive the host's loudspeaker. This signal is used by the modem function only and the source is from the MSI pin.
$\overline{STSCHG}$	O	STATUS CHANGE. Used to alert the host to changes in the RRdy bit in the PRR (Pin Replacement Register) or the RIEvt or PIEvt bits in the IOER (I/O Event Register).

PIN DESCRIPTION (continued)

MODEM INTERFACE (SECOND PERIPHERAL PORT)

The following signals are active only after the modem EnFn bit in the COR (Configuration Option Register) has been set.

PIN	TYPE	DESCRIPTION
$\overline{MCS}$	O	MODEM CHIP SELECT. This signal is asserted whenever a modem address range is decoded.
$\overline{MINT}$	I	MODEM INTERRUPT. This modem interrupt is combined with the internal LAN interrupt according to the PCMCIA Multiple Function Spec and passed to $\overline{IREQ}$ pin.
MRST, $\overline{MRST}$	O	MODEM RESET. These signals are asserted (both polarity) when there is a hardware reset or a software reset through the modem SRESET bit in the COR (Configuration Option Register).
MPD, $\overline{MPD}$	O	MODEM POWER DOWN. Both polarity outputs are provided to reflect the modem PwrDwn bit in the CSR (Configuration and Status Register).
MRDY	I	MODEM READY. A low indicates that the modem is not ready. This signal is not intended to delay the completion of an I/O cycle. In fact, no wait state is provided for modem access. This signal is reflected in the RRdy bit in the modem PRR (Pin Replacement Register).
MSI	I	MODEM SPEAKER INPUT. This pin is qualified with the modem Audio bit in the CSR (Configuration and Status Register) to produce the inverted $\overline{SPKR}$ output.
MRI	I	MODEM RING INPUT. This pin is used to indicate ringing. This signal is latched into the RIEvt bit in the IOER (I/O Event Register).

CIS MEMORY (1 PIN)

$\overline{CISCS}$	O	CARD INFORMATION STRUCTURE (CIS) CHIP SELECT. Active low signal which indicates that the current cycle is from or to the external CIS Attribute memory. The CIS memory address and data bus connect directly to the PC Card bus and the output enable and write enable pins connect to the $\overline{OE}$ and $\overline{WE}$ pins. When the WP bit (BMR12 < 3 >) is set, writing to the CIS memory is prevented.

BUFFER MEMORY INTERFACE

$\overline{RCS0}$, $\overline{RCS1}$	O	RAM CHIP SELECT. $\overline{RCS0}$ and $\overline{RCS1}$ are active low chip select lines for the SRAM with $\overline{RCS0}$ as the least significant byte.
ROE	O	RAM OUTPUT ENABLE. Active low. This is the output enable asserted by the TSC 78Q8378 during buffer memory read cycles for the SRAM.
RWE	O	RAM WRITE ENABLE. Active low. This is the write enable asserted by the TSC 78Q8378 during buffer memory write cycles for the SRAM.
RD[0:15]	I/O	RAM DATA BUS. This is the data bus between the TSC 78Q8378 and the buffer memory. It can be configured for byte or word transfer depending on register bit RBYTE (DLCR6 <4>) RAM BYTE. For word transfers, the ordering of the most and least significant byte is defined by the register bit, INTLMOT (DLCR7 <0>). In PC Card bus mode, this data bus is only 8 bits wide (RD[0:7]).
RA[0:15]	O	RAM ADDRESS BUS. Addresses up to 64 KByte of SRAM buffer memory.

NETWORK ATTACHMENT UNIT INTERFACE

PIN	TYPE	DESCRIPTION
DON, DOP	O	TRANSMIT DATA NEGATIVE and POSITIVE. Differential outputs to external transceiver for transmission.
DIN, DIP	I	RECEIVE DATA NEGATIVE and POSITIVE. Manchester differential inputs from external transceiver for reception.
CIN, CIP	I	COLLISION DETECT NEGATIVE and POSITIVE. When an externally connected transceiver detects a collision on the medium, these differential inputs are driven by a 10 MHz signal.
RBIAS	-	EXTERNAL RESISTOR. External biasing resistor. Connect to 20 kΩ ±1% to AGND.

NETWORK TWISTED-PAIR MEDIUM INTERFACE

TPON, TPOP	O	TWISTED-PAIR OUTPUT NEGATIVE and POSITIVE. Driver outputs to twisted-pair medium. Must be summed together with TPDN and TPDP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPDN, TPDP	O	TWISTED-PAIR DELAYED NEGATIVE and POSITIVE. Delayed (50 ns) driver outputs to twisted-pair medium. Must be summed together with TPON and TPOP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPIN, TPIP	I	TWISTED-PAIR INPUT NEGATIVE and POSITIVE. Inputs from twisted-pair medium.

DEVICE POWER

VDD	P	POWER SUPPLY. A +5V DC (±5%) or +3.3 VDC (±0.3V) supply is required.
GND	P	SYSTEM GROUND.
AVDD	P	ANALOG VDD. The analog VDD pin required by the internal AUI and twisted-pair circuits is to be connected to a different VDD path from the digital VDD. A +5V DC (±5%) or +3.3 VDC (±0.3V) supply is required.
AGND	P	ANALOG GROUND. The analog ground required by the internal encoder/decoder is to be connected to a separate GND path from the digital GND.

CRYSTAL OSCILLATOR

OSCI	I	OSCILLATOR IN. Connection for one side of the 20 MHz crystal or an input for an external 20 MHz clock source.
OSCO	O	OSCILLATOR OUT. Connection for other side of the 20 MHz crystal. Left unconnected if an external clock is used.

PIN DESCRIPTION (continued)

MISCELLANEOUS

NAME	TYPE	DESCRIPTION
CB	O	CONTROL BIT. A complement of the internal register bit, DLCR4 < 2 >, which is used to activate any external hardware.
LEDLT	O	LED LINK, TRANSMIT. Connect to LED with current limiting resistor to VDD. LED is on during link up and off during link down. During link up (when LED is on), a transmission will blink off the LED temporarily to indicate activity. This feature is available only for the twisted pair interface.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Supply voltage, Vdd	-0.5 to 6.0V
Input voltage, Vin	-0.5 to Vdd + 0.5V
Output voltage, Vout	-0.5 to Vdd + 0.5V
Storage temperature, Tstg	-55 to 150°C
Lead temperature (max 10 sec soldering), Tl	250°C max

DC CHARACTERISTICS (Ta = 0 to 70°C, Vd-d = 5V ±5%, 5V Values)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Low level input voltage	Vil	TTL inputs				0.8	V
		OSCI pin				1.6	V
		Schmitt inputs				1.1	V
High level input voltage	Vih	TTL inputs		2.2			V
		OSCI pin		3.8			V
		Schmitt inputs		3.5			V
Pull down current (RESET pin)	Ipd			13		50	µA
Low level output voltage	Vol	Rated Iol		0		0.4	V
High level output voltage	Voh	Rated Ioh		2.4		Vdd	V
Low level output current	Iol	Pin types O4, IO4, IO4U	Vdd = 5V	4			mA
(with Vol = 0.4V)		Pin type O8,	Vdd = 5V	8			mA
		Pin type OD16	Vdd = 5V	16			mA
High level output current	Ioh	Pin types O4 IO4, IO4U	Vdd = 5V	-4			mA
(with Voh = 2.4V)		Pin type O8	Vdd = 5V	-8			mA
Leakage current (input/output)	Il			-10		10	µA
Supply current	Idd	Fully active(1)				40	mA
		Idle				30	mA
Power down supply current	Ipwrdn	Osc. on				10	mA
		Osc. off				200	µA

NOTE: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS (Ta = 0 to 70°C, Vdd = 3.3V ±0.3V, 3V Values)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Low level input voltage	Vil	TTL inputs			0.8	V
		OSCI pin			0.7	V
		Schmitt inputs			0.4	V
High level input voltage	Vih	TTL inputs	2			V
		OSCI pin	2.1			V
		Schmitt inputs	2.4			V
Pull down current (RESET pin)	Ipd		5		28	µA
Low level output voltage	Vol	Rated Iol	0		0.4	V
High level output voltage	Voh	Rated Ioh	2.4		Vdd	V
Low level output current	Iol	Pin types O4, IO4, IO4U Vdd = 3.3V	2.4			mA
(with Vol = 0.4V)		Pin type O8 Vdd = 3.3V	4.9			mA
		Pin type OD16 Vdd = 3.3V	9.8			mA
High level output current	Ioh	Pin types O4, IO4, IO4U Vdd = 3.3V	-1.5			mA
(with Voh = 2.4V)		Pin type O8 Vdd = 3.3V	-3			mA
Leakage current (input/output)	Il		-10		10	µA
Supply current	Idd	Fully active(1)			28	mA
		Idle			20	mA
Power down supply current	Ipwrdn	Osc. on			6	mA
		Osc. off			100	µA

Note: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

AUI CHARACTERISTICS
(VDD = 5V ± 5%, 3.3 ± 0.3V, Vss = 0V, Ta = 0°C to +70°C)

Low Output Voltage for DOP, DON Vaol	Rext = 20 kΩ Rl = 78Ω	Vdd-1.5		Vdd-0.75	V
High Output Voltage for DOP, DON Vaoh	Rext = 20 kΩ Rl = 78Ω	Vdd-0.55		Vdd	V
DOP, DON Output Current Iao	Rext = 20 kΩ	8		14	mA

AUI CHARACTERISTICS (continued)
(VDD = 5V ± 5%, 3.3 ± 0.3V, Vss = 0V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DIP, DIN, CIP, CIN Open Circuit Input Voltage (bias) Valb	Vdd = 5V ± 5%	2.45		3.33	V
	Vdd = 3.3 ± 0.3V	2.13		2.88	V
DIP, DIN, CIP, CIN Diff Squelch Threshold Vasq		-300		-120	mV
DOP, DON Diff Idle Output Vadi	Rl = 78Ω	-40		40	mV
DOP, DON Diff Peak Output Vadv	Rext = 20 kΩ Rl = 78Ω	620		1100	mV
DOP, DON Output Resistance Rao				75	Ω

TWISTED PAIR
(VDD = 5V ± 5%, Ta = 0°C to +70°C)

TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.45		3.33	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 5V	-3.1		3.1	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	300		585	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-585		-300	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		180		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-180		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	120		300	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-300		-120	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		100		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-100		mV
TPOP, TPON High Output Voltage Vtoh	I = 32 mA	Vdd_{TP} -0.44		Vdd_{TP}	V

TWISTED PAIR (continued)
(VDD = 5V ± 5%, Ta = 0°C to +70°C)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TPOP, TPON Low Output Voltage Vtol	I = 32 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN High Voltage Vtdh	I = 16 mA	Vddtp -0.44		Vddtp	V
TPDP, TPDN Low Voltage Vtdl	I = 16 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN Output Resistance Rtd				27	Ω
TPOP, TPON Output Resistance Rto				13.5	Ω

NOTE 1: Sine wave at 2 MHz, 5 MHz and 7 MHz
NOTE 2: Sine wave : 5 MHz ≤ *f* ≤ 10 MHz

TWISTED PAIR
(VDD = 3.3 ± 0.3V, Ta = 0°C to +70°C)

TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.13		2.88	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 3.3V	-2.2		2.2	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	210		410	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-410		-210	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		130		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-130		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	90		210	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-210		-90	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		70		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-70		mV

TWISTED PAIR (continued)
(VDD = 3.3 ± 0.3V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPOP, TPON High Output Voltage Vtoh	I = 50 mA	Vdd_{TP} -0.3		Vdd_{TP}	V
TPOP, TPON Low Output Voltage Vtol	I = 50 mA	Vss_{TP}		Vss_{TP} +0.3	V
TPDP, TPDN High Voltage Vtdh	I = 25 mA	Vdd_{TP} -0.3		Vdd_{TP}	V
TPDP, TPDN Low Voltage Vtdl	I = 25 mA	Vss_{TP}		Vss_{TP} +0.3	V
TPDP, TPDN Output Resistance Rtd				12	Ω
TPOP, TPON Output Resistance Rto				6	Ω

NOTE 1: Sine wave at 2 MHz, 5 MHz and 7 MHz
NOTE 2: Sine wave: 5 MHz ≤ *f* ≤ 10 MHz

TRANSFORMER RATIO:

5V OPERATION		3.3V OPERATION	
RX	TX	RX	TX
1:1	1:1	1:1.4 (step down)	1:1.4 (step down)

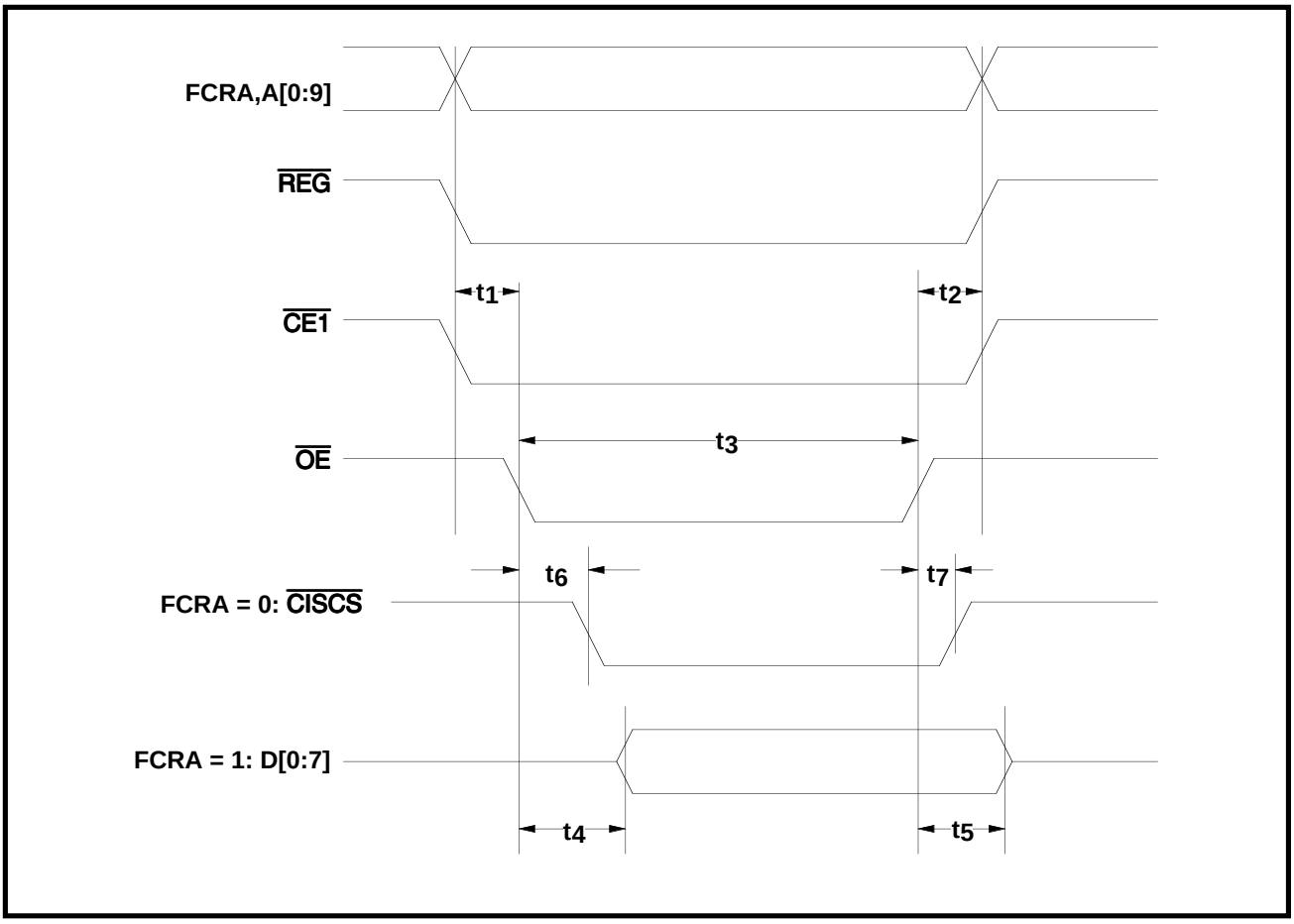


FIGURE 2: Attribute Memory Read Cycle

Unless otherwise stated, the following conditions apply to the remaining timing tables:
Ta = 0°C to + 70°C, Vdd = 5 ± 5%, Vdd = 3.3V ± 0.3V

TABLE 1: Attribute Memory Read Cycle (Refer to Figure 2)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
FCRA, A[0:9] Valid to $\overline{OE}$ low; $\overline{REG}$, $\overline{CE1}$ low to $\overline{OE}$ low	t_1		0			ns
$\overline{OE}$ high to A[0:9], FCRA invalid; $\overline{OE}$ high to $\overline{REG}$, $\overline{CE1}$ high	t_2		0			ns
$\overline{OE}$ low pulse width	t_3		45			ns
$\overline{OE}$ low to D[0:7] valid	t_4				50	ns
$\overline{OE}$ high to D[0:7] invalid (data hold)	t_5		5			ns
$\overline{OE}$ low to $\overline{CISCS}$ low	t_6				25	ns
$\overline{OE}$ high to $\overline{CISCS}$ high	t_7				25	ns

TABLE 2: Attribute Memory Write Cycle (Refer to Figure 3)

FCRA, A[0:9] Valid to $\overline{WE}$ low; $\overline{REG}$, $\overline{CE1}$ low to $\overline{WE}$ low	t_1		0			ns
$\overline{WE}$ high to A[0:9], FCRA invalid; $\overline{WE}$ high to $\overline{REG}$, $\overline{CE1}$ high	t_2		0			ns
$\overline{WE}$ low pulse width	t_3		45			ns
D[0:7] valid to $\overline{WE}$ high (data setup)	t_4		15			ns
$\overline{WE}$ high to D[0:7] invalid (data hold)	t_5		10			ns
$\overline{WE}$ low to $\overline{CISCS}$ low	t_6				25	ns
$\overline{WE}$ high to $\overline{CISCS}$ high	t_7				25	ns

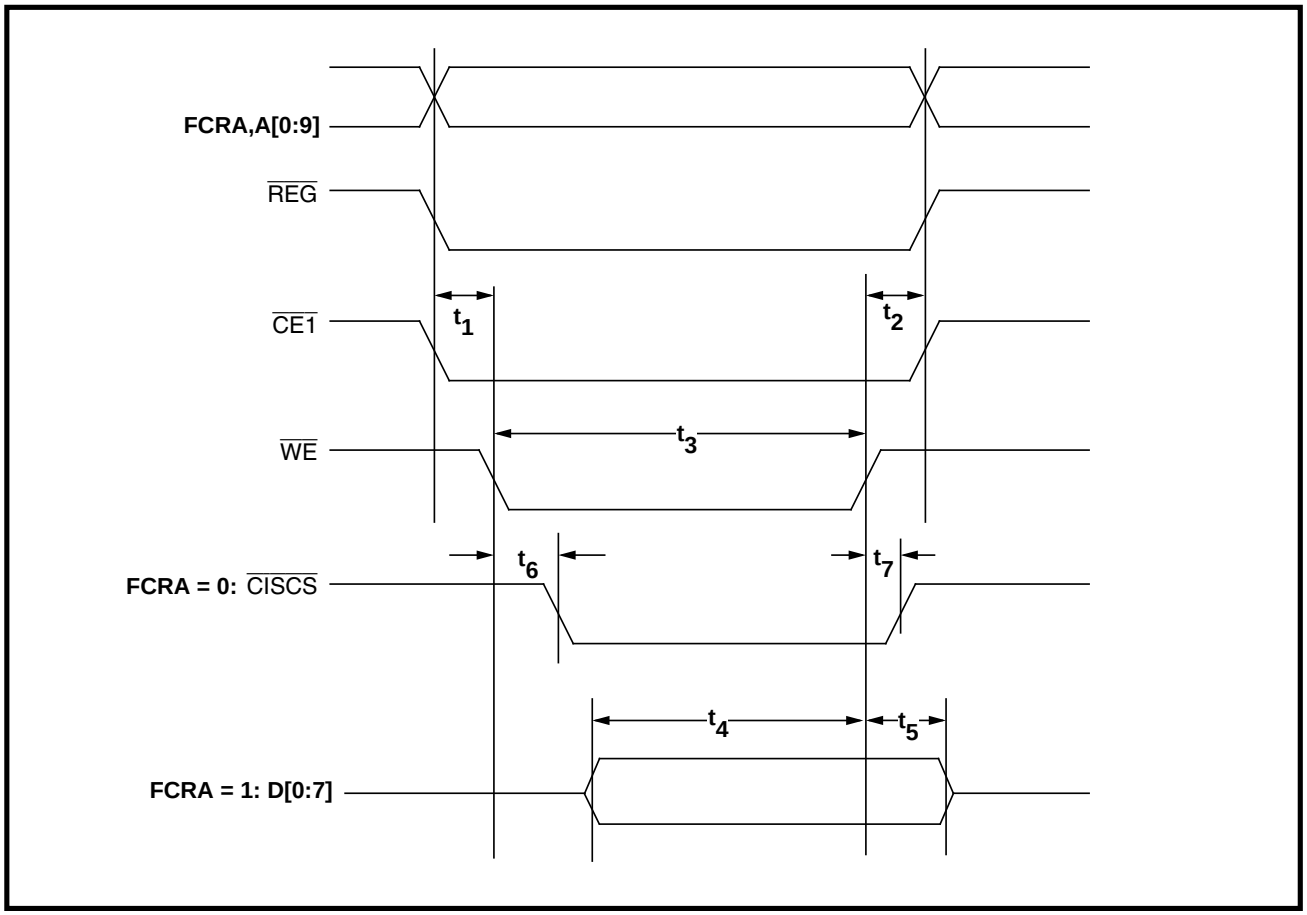


FIGURE 3: Attribute Memory Write Cycle

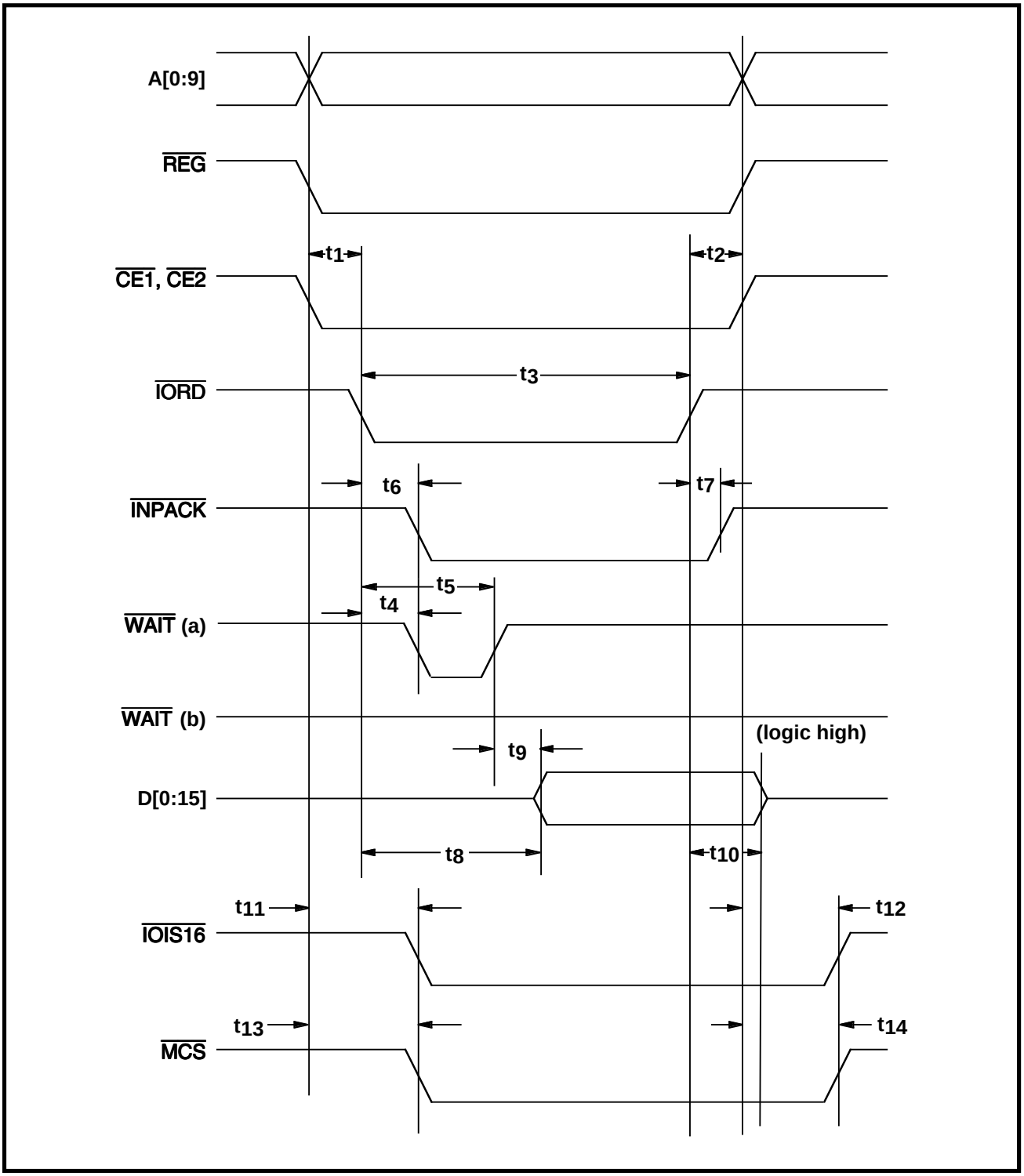


FIGURE 4: I/O Read Cycle

ELECTRICAL SPECIFICATIONS (continued)

TABLE 3: I/O Read Cycle (Refer to Figure 4)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
A[0:9] valid to $\overline{\text{IORD}}$ LOW; $\overline{\text{REG}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ low to $\overline{\text{IORD}}$ low	t_1		0			ns
$\overline{\text{IORD}}$ high to A[0:9] invalid; $\overline{\text{IORD}}$ high to $\overline{\text{REG}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ high	t_2		0			ns
$\overline{\text{IORD}}$ low pulse width	t_3		45			ns
$\overline{\text{IORD}}$ low to $\overline{\text{WAIT}}$ low	t_4	Port busy (a)	0		40	ns
$\overline{\text{IORD}}$ low to $\overline{\text{WAIT}}$ high(1)	t_5	Port busy (a)			350	ns
$\overline{\text{IORD}}$ low to $\overline{\text{INPACK}}$ low	t_6				25	ns
$\overline{\text{IORD}}$ high to $\overline{\text{INPACK}}$ high	t_7				25	ns
$\overline{\text{IORD}}$ low to D[0:15] valid	t_8	Register access (b)			70	ns
$\overline{\text{WAIT}}$ high to D[0:15] valid	t_9	Port busy (a)			5	ns
$\overline{\text{IORD}}$ high to D[0:15] invalid (data hold)	t_{10}		5			ns
A[0:9] valid to $\overline{\text{IOIS16}}$ low; $\overline{\text{REG}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ low to $\overline{\text{IOIS16}}$ low	t_{11}				30	ns
A[0:9] invalid to $\overline{\text{IOIS16}}$ high; $\overline{\text{REG}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ high to $\overline{\text{IOIS16}}$ high	t_{12}				30	ns
A[0:9] valid to $\overline{\text{MCS}}$ low	t_{13}				30	ns
A[0:9] invalid to $\overline{\text{MCS}}$ high	t_{14}				30	ns

NOTE: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 μs max for host read error.

(a) For Buffer Memory Port when port is busy.

(b) For register or port is not busy.

TABLE 4: I/O Write Cycle (Refer to Figure 5)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
A[0:9] valid to $\overline{IOWR}$ LOW; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ low to $\overline{IORD}$ low	t_1		0			ns
$\overline{IOWR}$ high to A[0:9] invalid; $\overline{IOWR}$ high to $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ high	t_2		0			ns
$\overline{IOWR}$ low pulse width	t_3		45			ns
$\overline{IOWR}$ low to $\overline{WAIT}$ low	t_4	Port busy (a)	0		40	ns
$\overline{IOWR}$ low to $\overline{WAIT}$ high(1)	t_5	Port busy (a)			350	ns
D[0:15] valid to $\overline{IOWR}$ high (data setup)	t_6		15			ns
$\overline{IOWR}$ high to D[0:15] invalid (data hold)	t_7		10			ns
A[0:9] valid to $\overline{IOIS16}$ low	t_8				30	ns
A[0:9] invalid to $\overline{IOIS16}$ high	t_9				30	ns
A[0:9] valid to $\overline{MCS}$ low	t_{10}				30	ns
A[0:9] invalid to $\overline{MCS}$ high	t_{11}				30	ns

NOTE: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host write error.

(a) For Buffer Memory Port when port is busy.

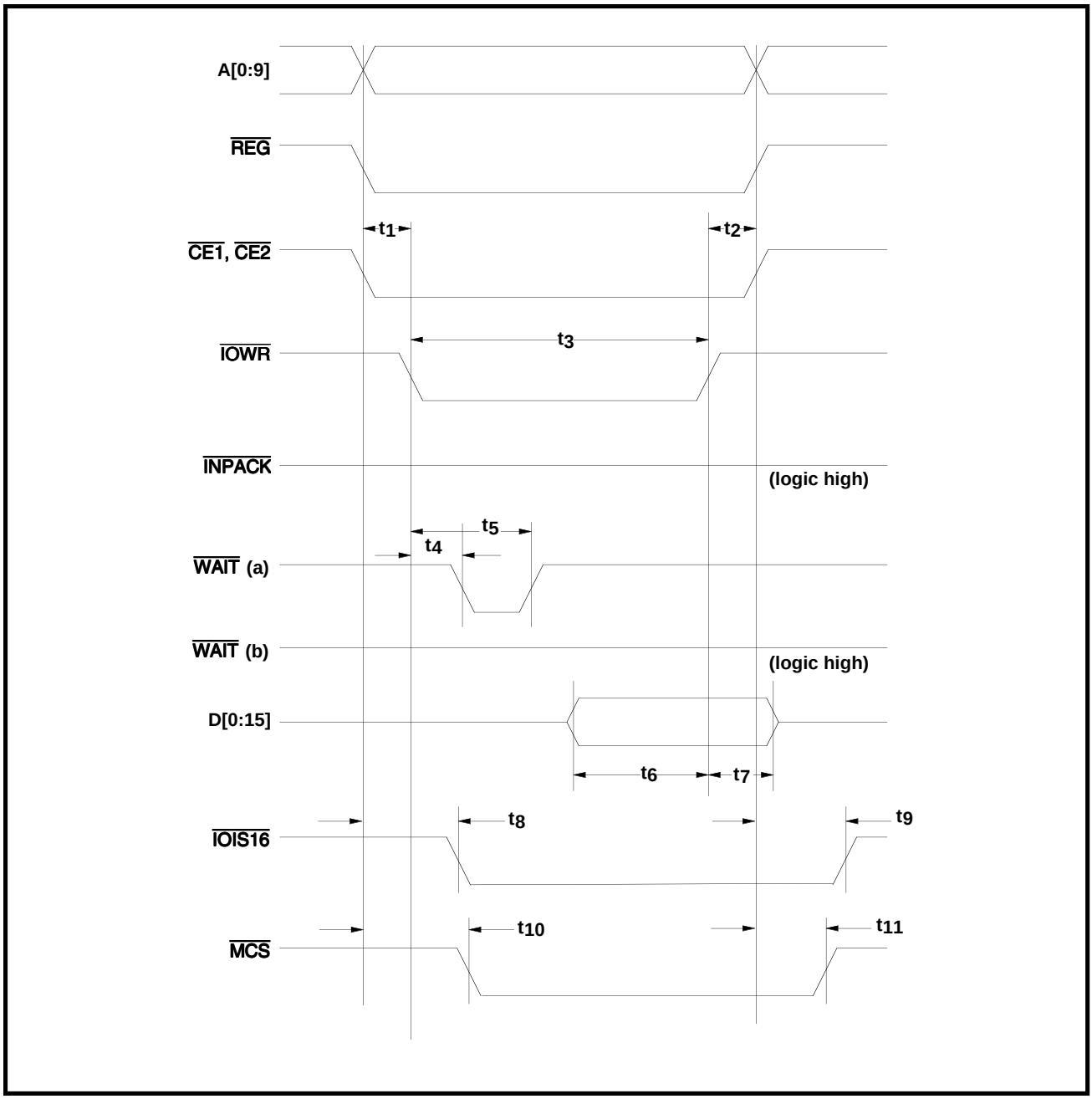


FIGURE 5: I/O Write Cycle

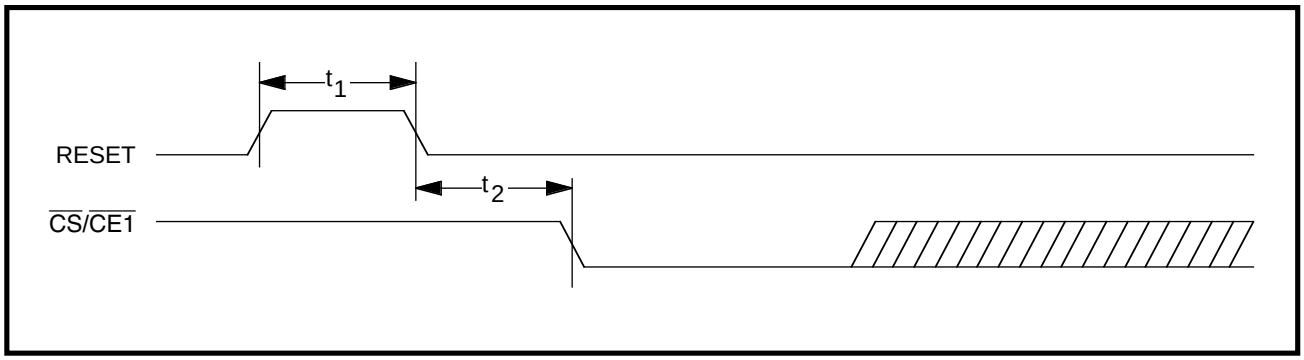


FIGURE 6: RESET Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 5: RESET Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
RESET pulse width t_1		500			ns
RESET low to first $\overline{CS}/\overline{CE1}$ low t_2		800			ns

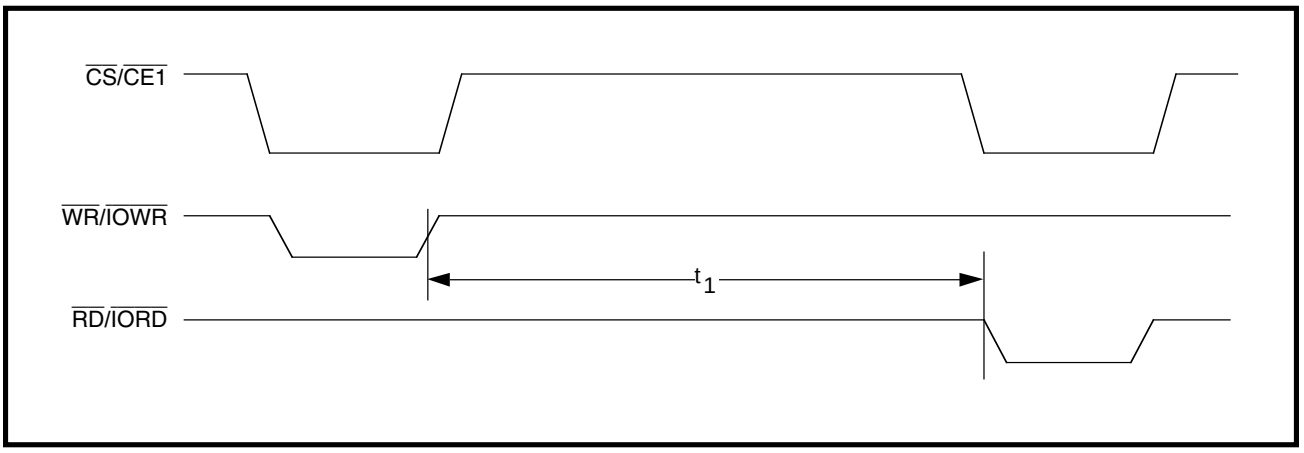


FIGURE 7: Skip Packet Timing

TABLE 6: Skip Packet Timing

Writing Skip Packet high to next Buffer Memory Port read t_1		200			ns

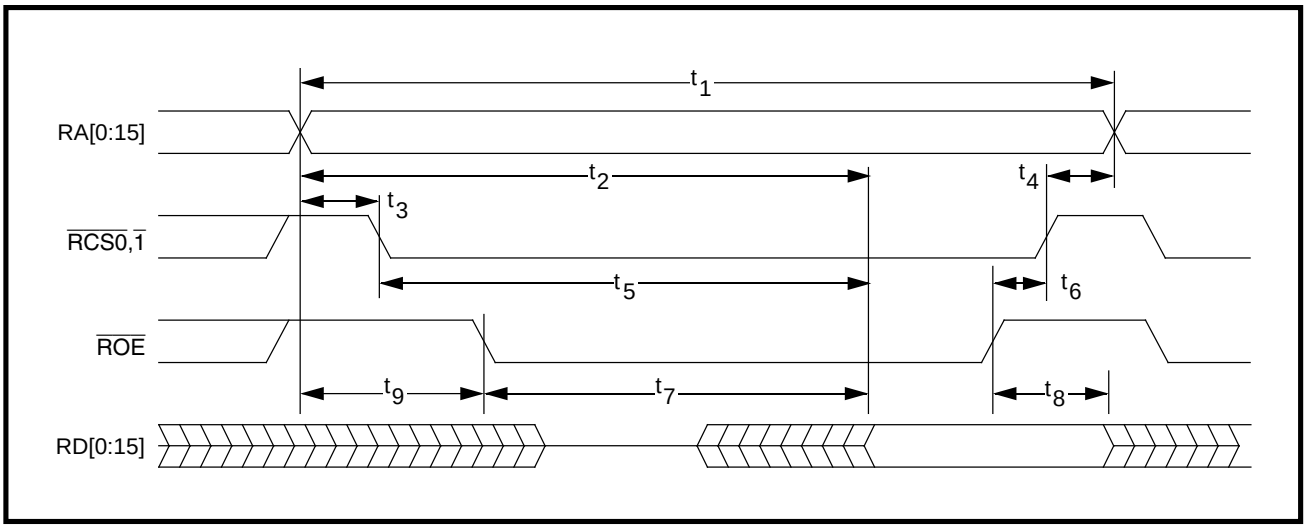


FIGURE 8: SRAM Read Timing

TABLE 7: SRAM Read Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Read cycle	t_1	RAMSP = 1	95			ns
		RAMSP = 0	145			ns
Address access time	t_2	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
Address valid to $\overline{RCS0,1}$ low	t_3				8	ns
$\overline{RCS0,1}$ high to address invalid	t_4		0			ns
Chip select access time	t_5	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
$\overline{ROE}$ high to $\overline{RCS0,1}$ high	t_6		0		8	ns
Output enable access time	t_7	RAMSP = 1			50	ns
		RAMSP = 0			100	ns
Data hold time	t_8		0			ns
Address valid to $\overline{ROE}$ low	t_9				30	ns

NOTE: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

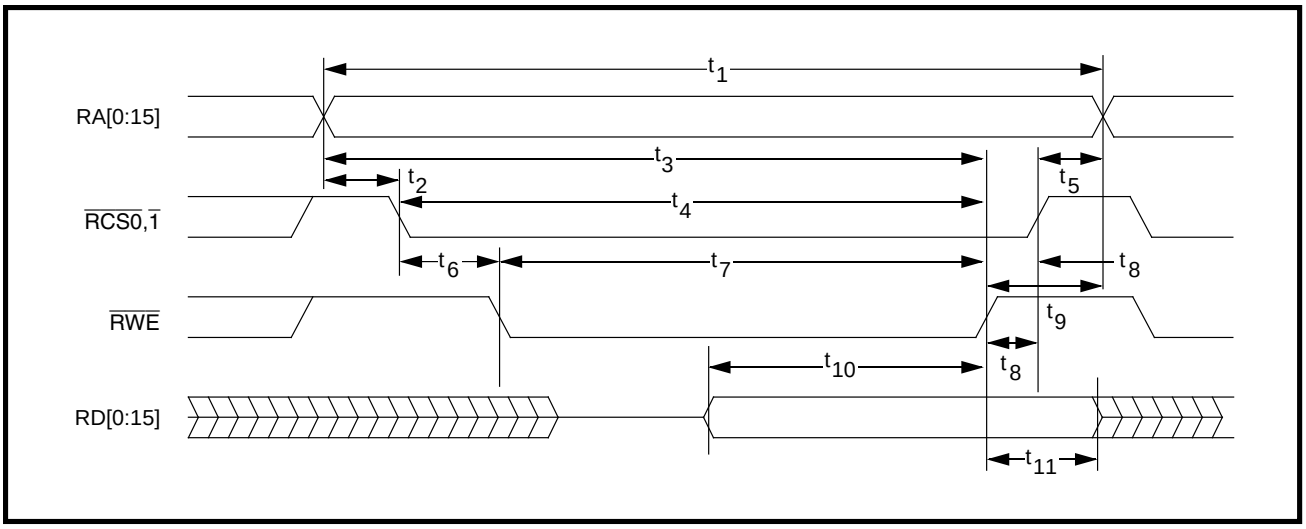


FIGURE 9: SRAM Write Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 8: SRAM Write Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Write Cycle	t_1	RAMSP = 1	95			ns
		RAMSP= 0	145			ns
Address Valid to $\overline{RCS0,1}$ low	t_2				8	ns
Address Valid to $\overline{RWE}$ high	t_3	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ high	t_4	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ high to Address Invalid	t_5		0			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ low	t_6		0			ns
$\overline{RWE}$ Pulse Width	t_7	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RWE}$ high to $\overline{RCS0,1}$ high	t_8		0			ns
$\overline{RWE}$ high to Address Invalid	t_9		10			ns
Data Setup Time	t_{10}	RAMSP = 1	40			ns
		RAMSP = 0	90			ns
Data Hold Time	t_{11}		20			ns

NOTE: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

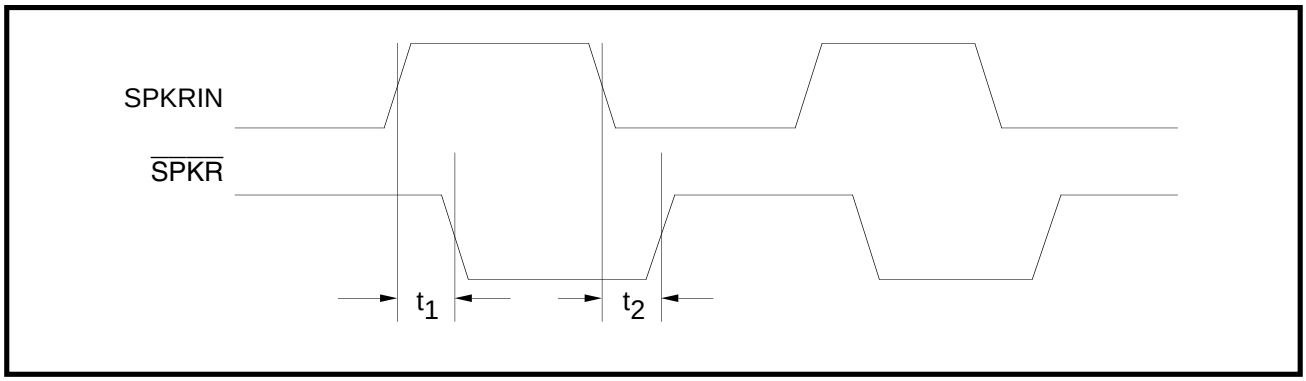


FIGURE 10: Speaker Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 9: Speaker Timing (Refer to Figure 10)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SPKR high to low propagation delay t_1	Vdd = 5V			25	ns
	Vdd = 3.3V			30	ns
SPKR low to high propagation delay t_2	Vdd = 5V			25	ns
	Vdd = 3.3V			30	ns

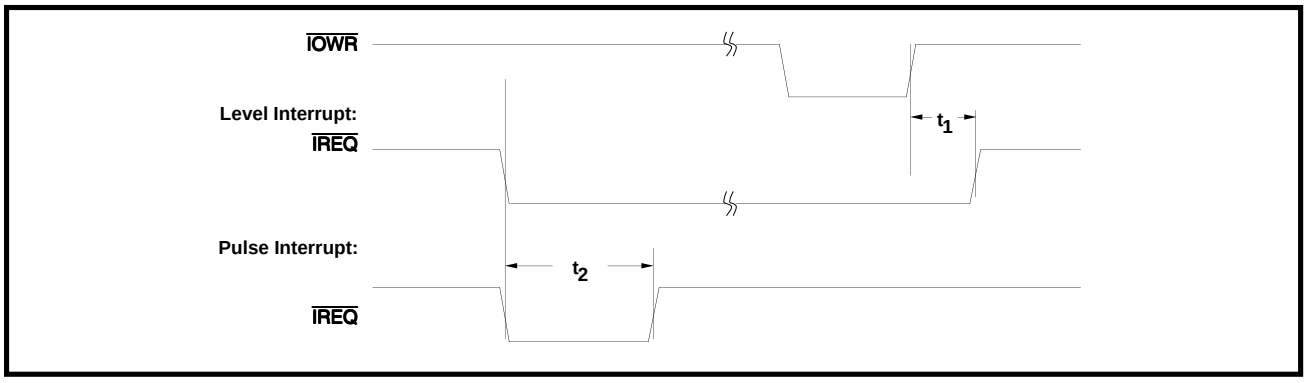


FIGURE 11: Single Interrupt Timing

TABLE 10: Single Interrupt Timing (Refer to Figure 11)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{IREQ}$		level interrupt			85	ns
signal clearing delay by $\overline{IOWR}$	t_1					
$\overline{IREQ}$ low pulse width	t_2	pulse interrupt	750		850	ns

NOTE: Intrack bit (CSR[0]) must be set to 0 for both functions for single interrupt mode.

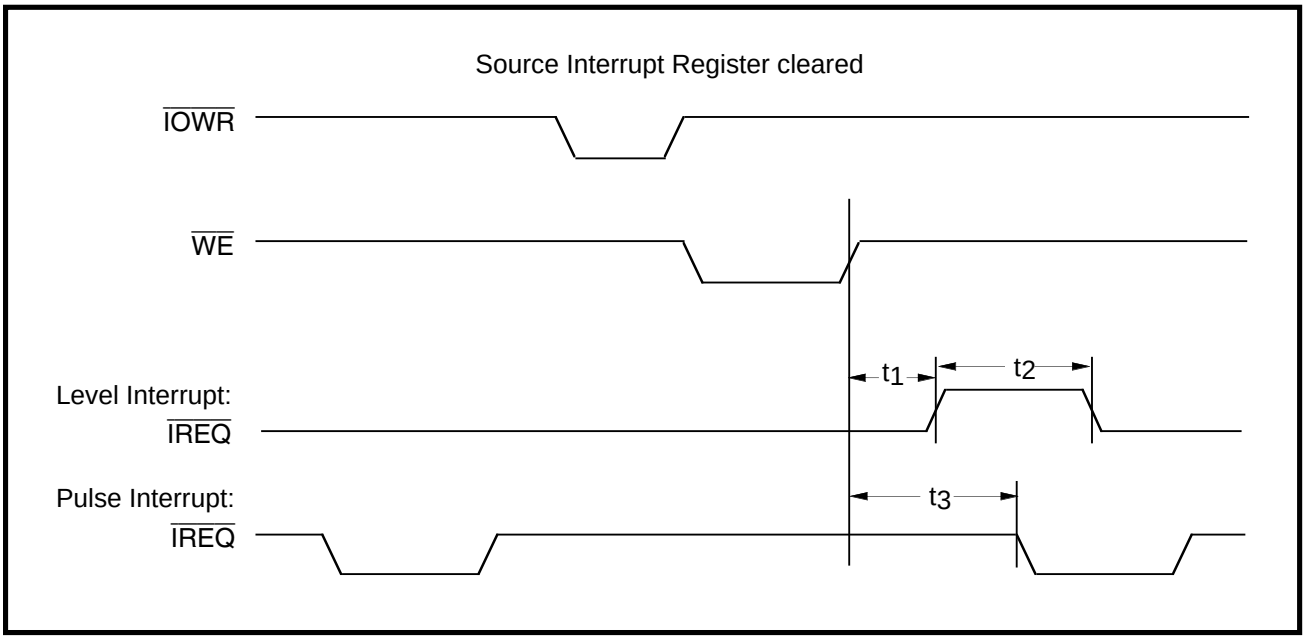


FIGURE 12: Shared Interrupt

TABLE 11: Shared Interrupt (Refer to Figure 12)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{IREQ}$ signal clearing delay by $\overline{WE}$	t_1	Level interrupt			40	ns
Back to back level interrupt inactive time	t_2	Pending level interrupt	750		850	ns
Pulse interrupt assertion delay	t_3	Pending Pulse interrupt	750		850	ns

NOTE: 1. Intrack bit (CSR[0]) must be set to 1 & Dintr bit (CORb[3]) to 0 for shared interrupt mode.
2. $\overline{IREQ}$ can only be cleared by host write 0 to intr bit (COR[1]) after clearing the interrupt source registers, DLCR1 or DLCR2.

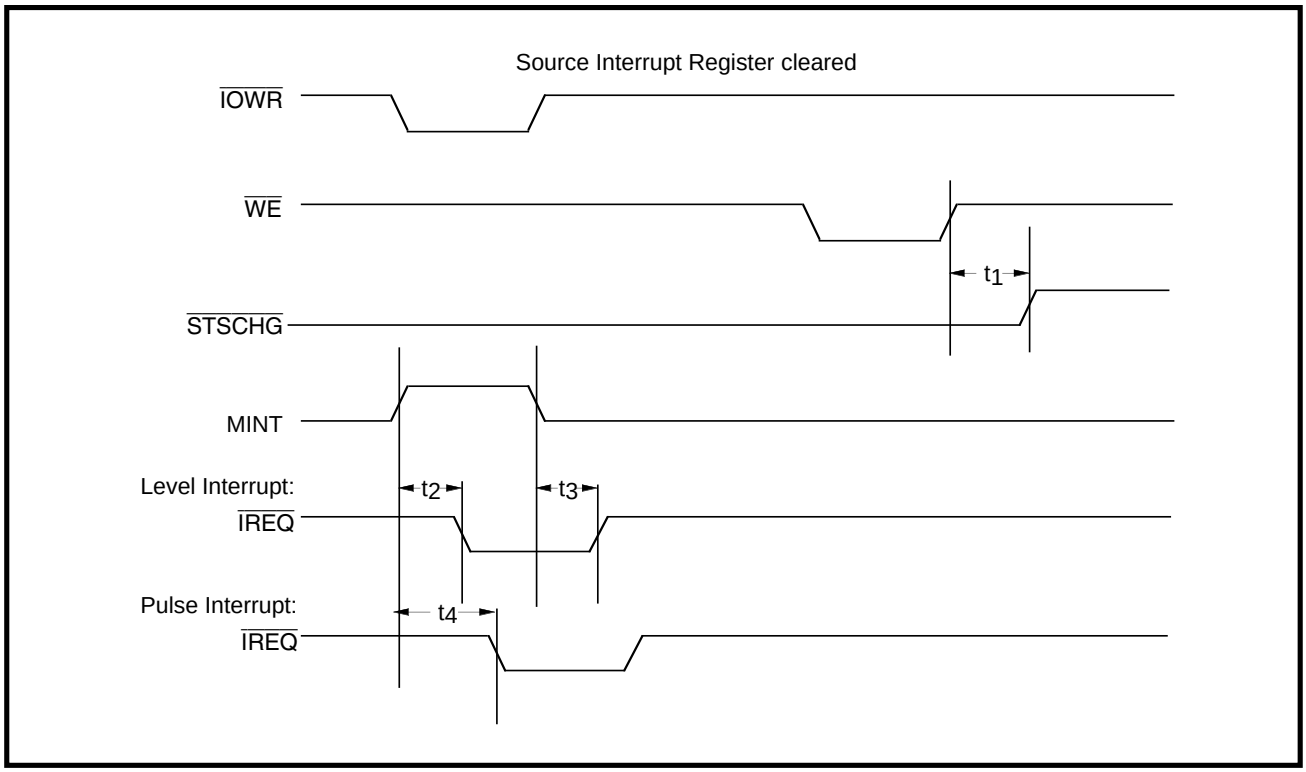


FIGURE 13: Dual Interrupt

ELECTRICAL SPECIFICATIONS (continued)

TABLE 12: Dual Interrupt (Refer to Figure 13)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$\overline{\text{STSCHG}}$ clearing delay for $\overline{\text{WE}}$	t_1				40	ns
Mint high to $\overline{\text{IREQ}}$ low	t_2	Level interrupt			55	ns
Mint low to $\overline{\text{IREQ}}$ high	t_3	Level interrupt			55	ns
Mint high to $\overline{\text{IREQ}}$ low	t_4	Pulse interrupt			55	ns

NOTE: 1. $\overline{\text{STSCHG}}$ can be cleared by writing 08H into PRRb register after clearing interrupt source registers.
2. Dintr bit (CORb[3]) must be set to high & Intrack bit (CSRb[0]) to low for dual interrupt mode.

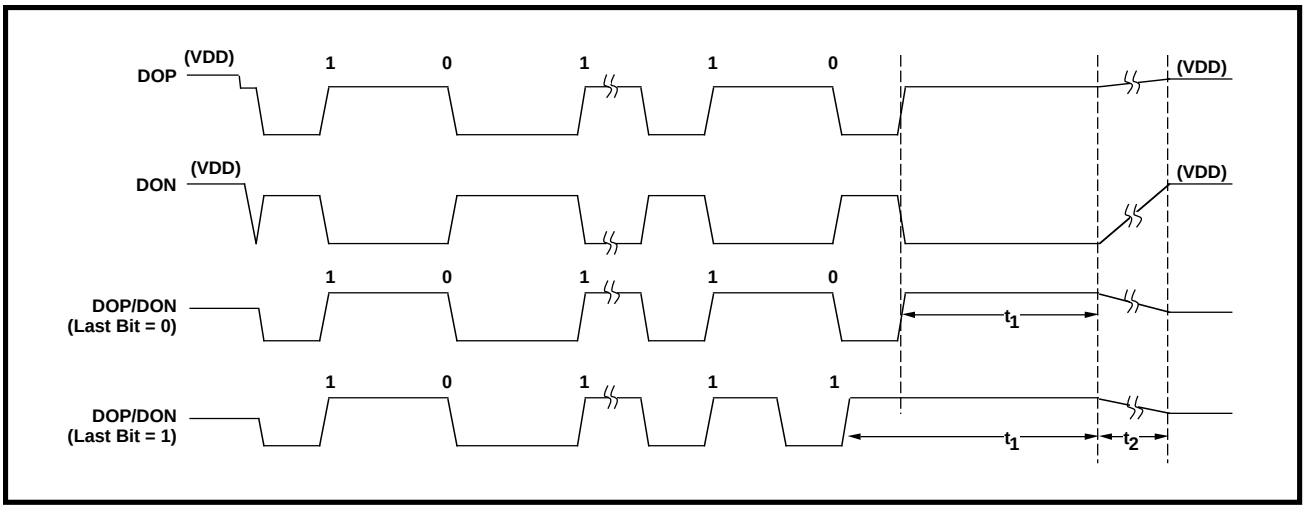


FIGURE 14: Transmit Timing (AUI)

TABLE 13: Transmit Timing (AUI)

DOP/DON end-of-packet delimiter	t_1		200			ns
DOP/DON line voltage transition	t_2				8	µs

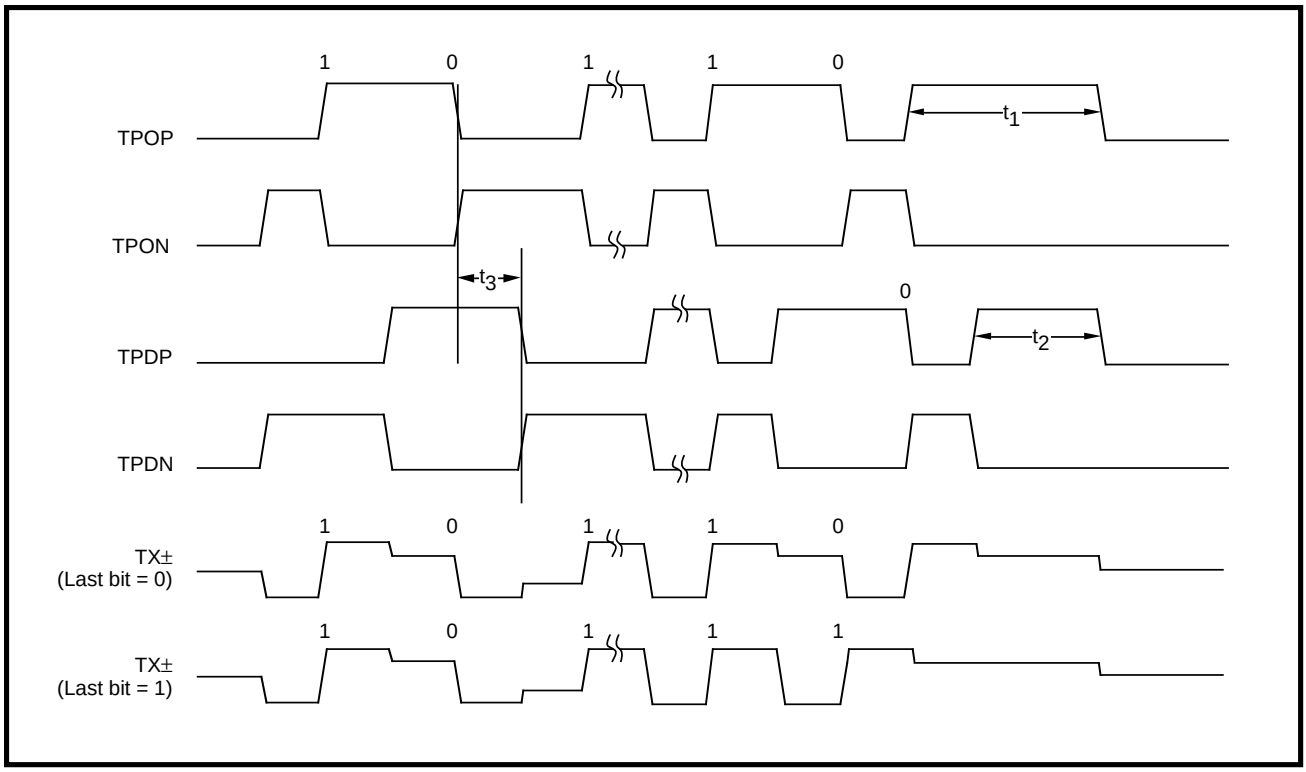


FIGURE 15: Transmit Timing (TP)

ELECTRICAL SPECIFICATIONS (continued)

TABLE 14: Transmit Timing (TP)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TPOP/TPON end-of-packet delimiter t_1		250			ns
TPDP/TPDN end-of-packet delimiter t_2		200			ns
TPOP to TPDP and TPON to TPDN delay t_3			50		ns

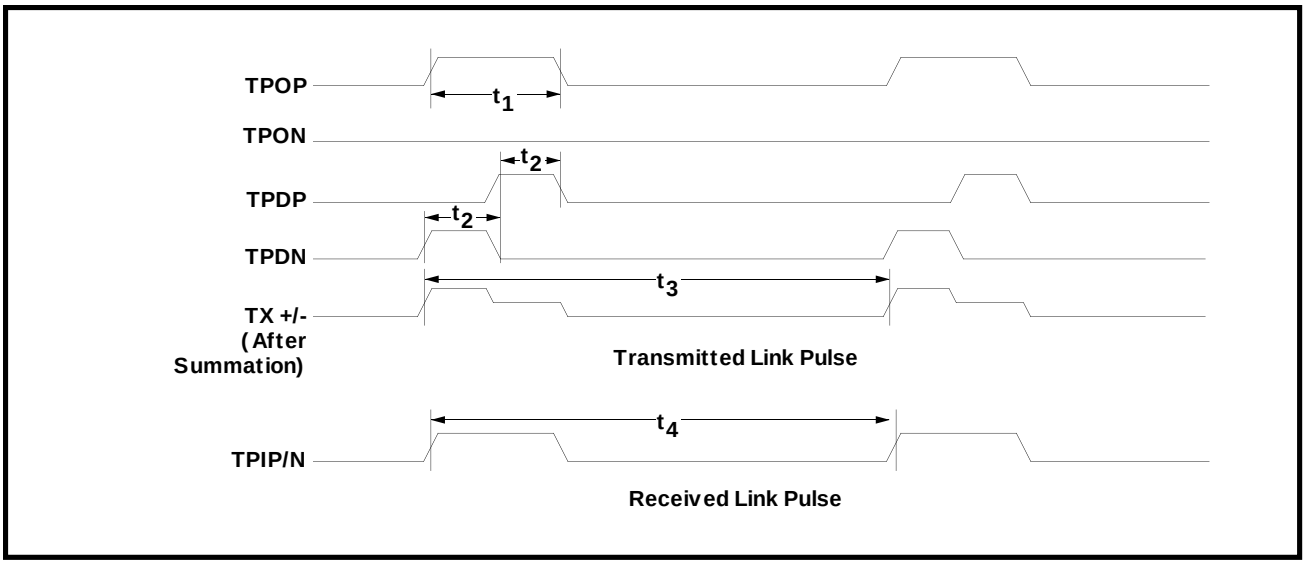


FIGURE 16: Link Test Timing

TABLE 15: Link Test Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
TPOP link pulse width	t_1			150		ns
TPDP/TPDN link pulse width	t_2			100		ns
Duration between transmitted link pulses	t_3		9		11	ms
Duration between received link pulses	t_4		4.1		65	ms

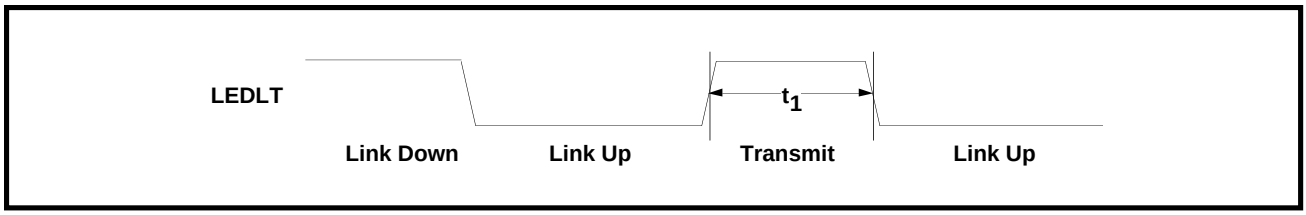


FIGURE 17: LED Timing (TP)

ELECTRICAL SPECIFICATIONS (continued)

TABLE 16: LED Timing

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Transmit blink-off timing	t_1	TP selected		100		ms

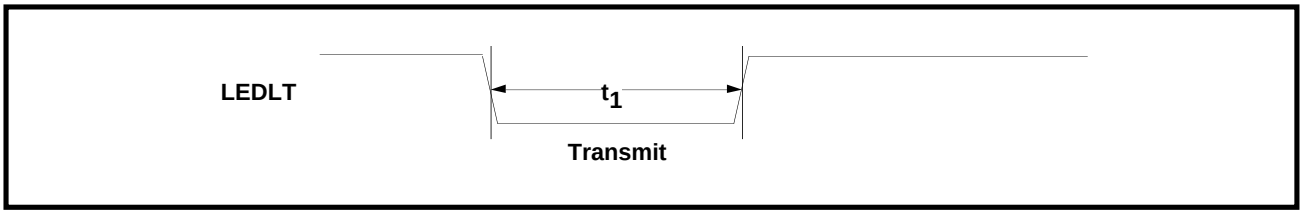


FIGURE 18: LED Timing (AUI)

TABLE 17: LED Timing

Transmit blink-on timing	t_1	AUI selected		100		ms

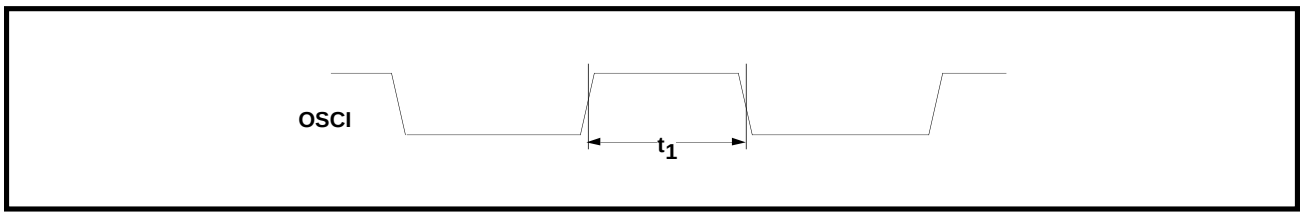


FIGURE 19: Oscillator Duty Cycle

TABLE 18: OSCI Duty Cycle

Oscillator duty cycle	t_1		40	50	60	%

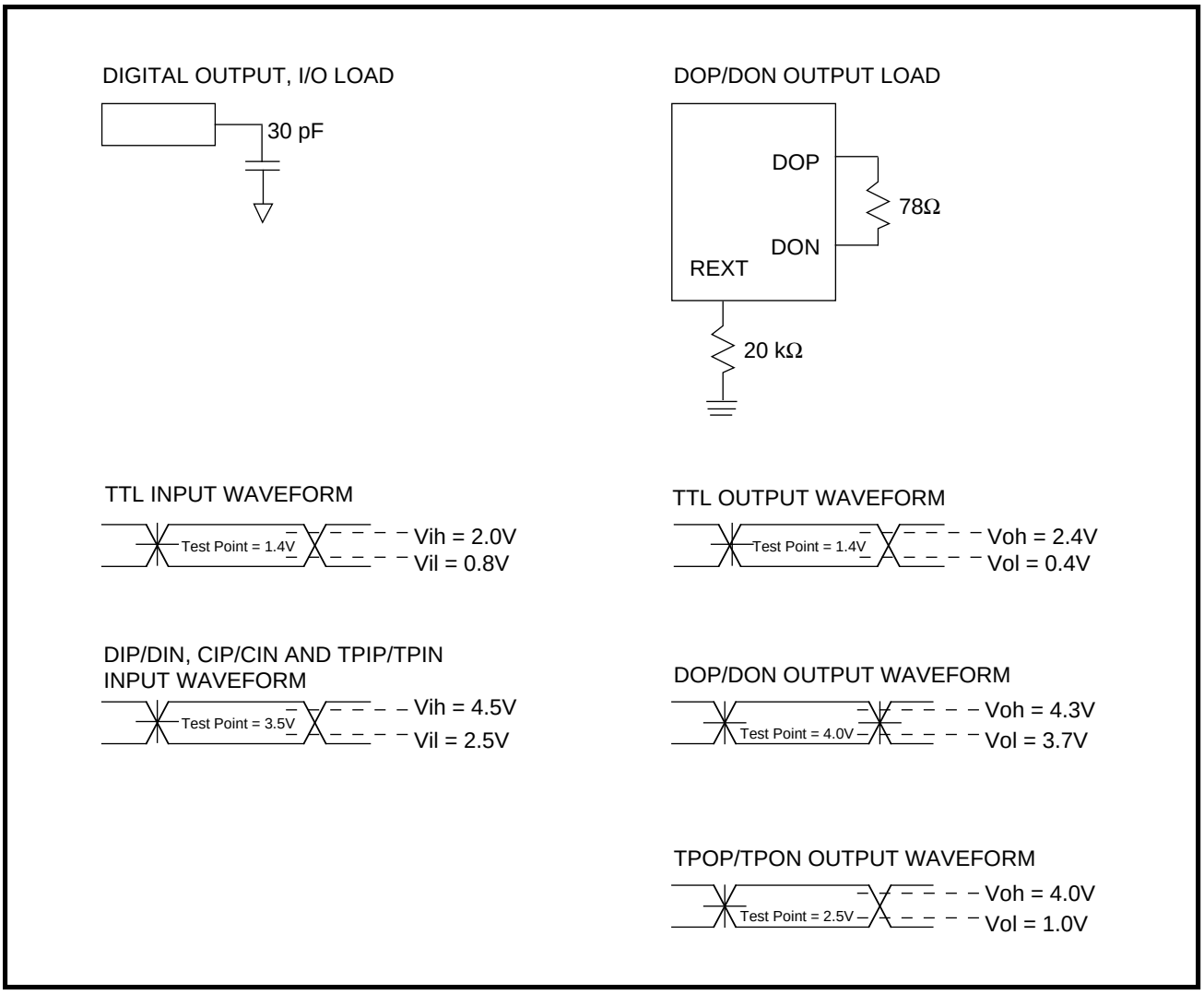
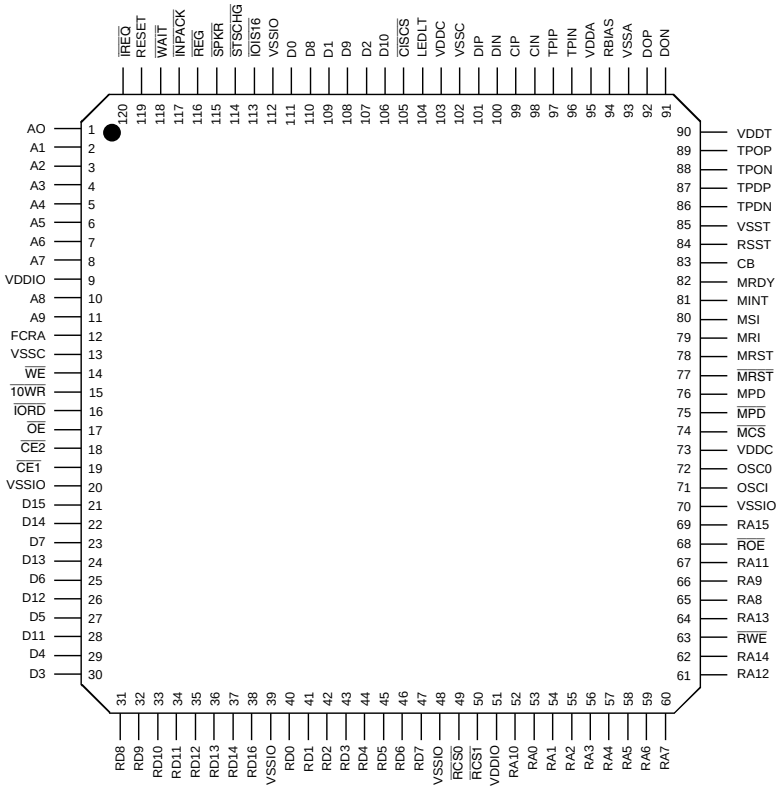


FIGURE 20: Test Conditions

TSC 78Q8378
3V, 5V PC Card
Multi-function Ethernet Combo

PACKAGE PIN DESIGNATIONS

(Top View)



TSC 78Q8378
120-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
TSC 78Q8378 120-Lead TQFP	78Q8378GT	TSC 78Q8378-CGT

TDK Semiconductor Corporation, 14351 Myford Road, Tustin, CA 92780-7068 (714) 573-6000, FAX (714) 573-6914