TDK SEMICONDUCTOR CORP.

TSC 78Q8373
3V, 5V PCMCIA Ethernet Combo

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DESCRIPTION

The TSC 78Q8373 is a highly integrated Ethernet IC for use in PCMCIA (Personal Computer Memory Card International Association) applications and can operate with a power supply of 3.3V or 5V. It contains a Media Access Controller (MAC), a 10 Mbit/s Manchester encoder/decoder (ENDEC), a 10Base-T transceiver, a memory-card bus interface (PCMCIA), and an Attachment Unit Interface (AUI). This level of integration allows the user to implement a PCMCIA card for 10Base-T using only the TSC 78Q8373, external memory, and some passive components. The internal bus interface circuit allows connection to a PCMCIA 2.1 bus without other external components. The PCMCIA bus-decoding logic can be bypassed for connection to other bus types. The TSC 78Q8373 connects to twisted-pair media via line transformers through the on-chip transceiver circuit. Connection to other media such as coaxial cable is made through the AUI port to an external transceiver, such as the TSC 78Q8392L Ethernet Coax Transceiver.

The TSC 78Q8373 has a sophisticated power management capability with three different operating modes allowing the user to maximize power savings, making it ideal for use in PCMCIA applications. During normal operation, the IC monitors its own actions and shuts down the circuits that are not being used, resulting in the lowest possible operating power. It also has a standby mode which leaves only the oscillator running, and a full shutdown mode which also turns off the oscillator.

An intelligent Buffer Manager is controlled by the host read, host write, receive and transmit pointers, and the TSC 78Q8373 manages the pointers internally without any host intervention. The device interleaves access to the buffer memory so that accesses from the host and from the network media seem to operate concurrently. Big and little endian byte orderings make for simple bus interface to all standard microprocessors.

The TSC 78Q8373 is available in a 100-lead thin QFP (TQFP) package, and can operate with a power supply of 3.3 volts or 5 volts.

FEATURES

- **Single-chip solution for 10Base-T/PCMCIA designs**
- **Operation at 3.3V or 5V**
- **Pin-compatible with TSC 78Q8370**
- **Integrated 10Base-T transceiver:**
  - **Programmable/automatic selection of twisted pair (RJ45) or AUI port**
  - **Receive polarity detection/correction on twisted-pair inputs**
- **Manchester Encoder/Decoder circuit**
- **AUI port for connection to 10Base2/5 transceiver or AUI cable**
- **Integrated bus interface compliant with PCMCIA release 2.1 specification**
- **Bus interface can be bypassed for non-PCMCIA applications**
- **Protocol Controller compliant with IEEE 802.3 and Ethernet 2.0**
- **Advanced Buffer Manager architecture:**
  - **Automatic management of all pointers**
  - **Allows "simultaneous" access to data in buffer memory by both the network and host**
  - **High-speed received packet skip**
- **Configurable Buffer Memory for design flexibility:**
  - **Two-bank transmit buffer in 2, 4, 8, or 16 Kbyte sizes**
  - **Ring-structure receive buffer from 4 to 62 Kbytes**
- **Software-configurable system bus structure:**
  - **Compatible with major microprocessors**
  - **8- or 16-bit wide data path communications with hosts**
- **Power management options:**
  - **Intelligent power mode automatically shuts off unused circuitry**
  - **Standby mode reduces power while not in operation**
  - **Full shutdown mode offers maximum power savings**
- **Available in a 100-lead TQFP package**

FUNCTIONAL DESCRIPTION

The TSC 78Q8373 consists of six major blocks as shown in Figure 1.

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- Host/PCMCIA Interface
- Manchester ENDEC
- Twisted Pair Transceiver
- Power Management

BUFFER MANAGER

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration, this makes the TSC 78Q8373 a high performance LAN controller.

The buffer memory is divided into two portions: transmit memory portion and receive memory portion. The transmit memory portion can be partitioned into 2K, 4K, 8K or 16 Kbyte buffer sizes. There is only one transmit bank if a 2 KB transmit buffer size is selected. If the transmit buffer size is greater than 2 KB, then the transmit buffer is configured into two banks of equal size. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be transmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62 KB depending on the buffer memory configuration which has a range of 8K to 64 KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from 4 sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the TSC 78Q8373 will assert a 'not ready' handshake to the host while servicing the Transmitter and/or Receiver. The TSC 78Q8373 arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operations appear to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the 8373 can potentially be receiving data from the medium and loading it into the receive buffer (if the TSC 78Q8373 is in a loop back mode or if self-reception occurs).

DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ANSI/IEEE 802-3 CSMA/CD protocol. It consists of a Transmitter, a Receiver and CRC logic (which is shared by both transmit and receive operations). Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

HOST/PCMCIA INTERFACE

The Host Interface (HIF) provides connection to the host system. It consists of the various registers, DMA circuits and ready logic. Both word and byte interfaces are supported as well as big endian and little endian data ordering. Host access to the buffer memory is through BMR8 (and BMR9). Reading from BMR8 will read a byte or word from the receive buffer and writing to BMR8 will write a byte or word to the transmit buffer. The ready logic is capable of delaying host access to the buffer memory with a time-out mechanism. Both single and burst DMA transfer modes are supported.

The PCMCIA interface circuitry builds on top of the TSC 78Q8373 generic host interface and is only active if the MODE pin is left unconnected (internally pulled-up). The TSC 78Q8373 can thus connect directly to a PCMCIA release 2.1 compliant bus. It also supports decoding for the external CIS memory (both ROM and Flash types). The 8373 pinout has been defined to minimize criss-crossing connections to the PCMCIA connector. This allows for a cost effective 2-layer PCB design.

MANCHESTER ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to either the twisted-pair transceiver block or to the Attachment Unit Interface (AUI) driver, depending on which block is active. The decoder section performs three functions: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at

the end of reception and during idle to save power. Jitter of up to ±18 ns can be tolerated by the decoder. This block also translates a 10 MHz collision signal to a logic-level signal before sending it to the DLC block if the AUI port is selected.

TWISTED PAIR TRANSCEIVER

The on-chip Twisted Pair module consists of a number of functions. It has a smart squelch circuitry to determine valid data present on the differential receive inputs TPIP/TPIN. Its transmit and pre-distortion drivers connect to the twisted pair network via the summing resistors and transformer/filter. The link detector/ generator circuitry checks the integrity of the cable connecting the two twisted pair MAUs. Collision, jabber and SQE are also incorporated.

POWER MANAGEMENT

One very useful and important feature that the TSC 78Q8373 offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

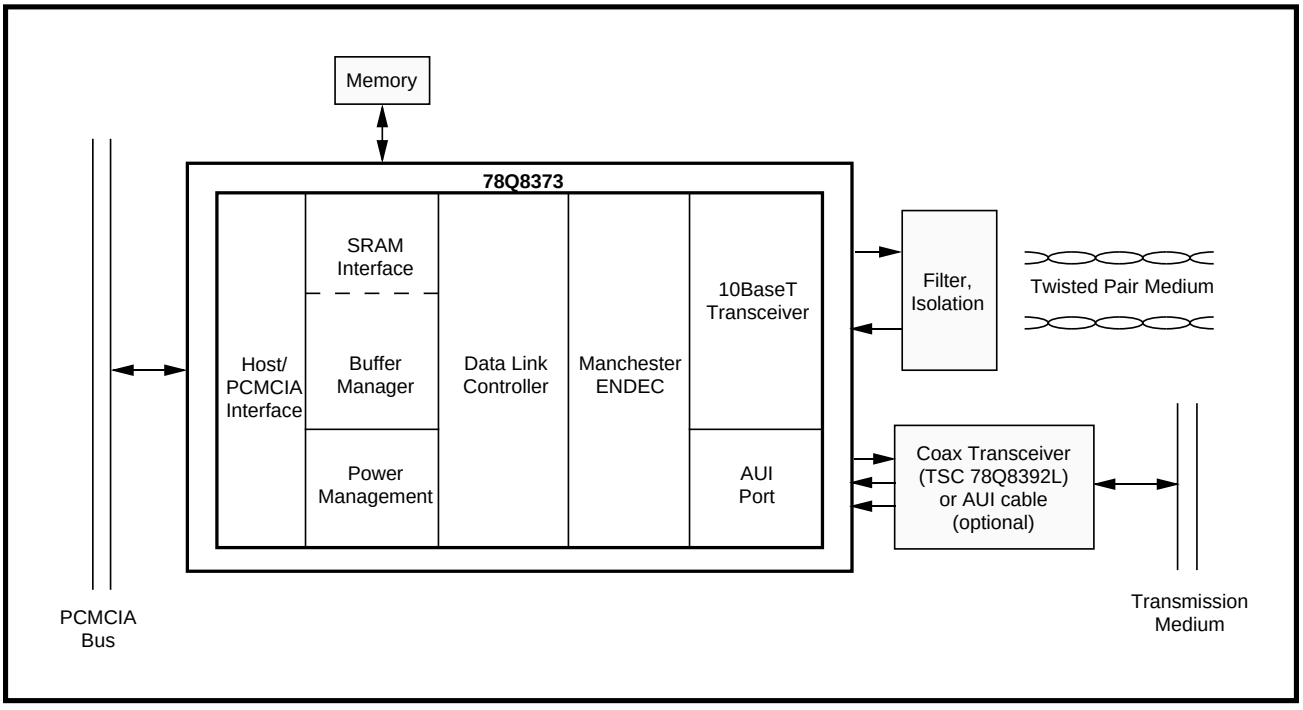

FIGURE 1: System Diagram

Pin Assignment Table - PCMCIA Bus Mode - 100-Pin TQFP

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	D1	IO4	26	$\overline{OE}$	I	51	RA4	O4	76	DON	AO
2	D8	IO4U	27	$\overline{WE}$	I	52	RA5	O4	77	DOP	AO
3	D0	IO4	28	$\overline{INPACK}$	O4	53	RA6	O4	78	AGND	P
4	A0	I	29	$\overline{REG}$	I	54	GND	P	79	REXT	R
5	A1	I	30	$\overline{ROMG}$	O4	55	VDD	P	80	AVDD	P
6	A2	I	31	$\overline{FCE}$	O4	56	RA7	O4	81	TPIN	AI
7	A3	I	32	$\overline{XPD}$	O4	57	RA12	O4	82	TPIP	AI
8	RESET	SI	33	XRST	O4	58	RA14	O4	83	MODE	TI
9	VDD	P	34	GND	P	59	$\overline{RWE}$	O4	84	DIN	AI
10	GND	P	35	RD0	IO4U	60	RA13	O4	85	DIP	AI
11	$\overline{IOWR}$	I	36	RD1	IO4U	61	RA8	O4	86	CIN	AI
12	$\overline{IORD}$	I	37	RD2	IO4U	62	RA9	O4	87	CIP	AI
13	$\overline{CE2}$	I	38	RD3	IO4U	63	RA11	O4	88	GND	P
14	D15	IO4U	39	RD4	IO4U	64	$\overline{ROE}$	O4	89	SPKRIN	SI
15	$\overline{CE1}$	I	40	RD5	IO4U	65	RA15	O4	90	$\overline{SPKR}$	O8
16	D14	IO4U	41	RD6	IO4U	66	OSCI	CI	91	CCRA	I
17	D7	IO4	42	RD7	IO4U	67	OSCO	O	92	RRST	O4
18	GND	P	43	GND	P	68	VDD	P	93	LEDLT	OD16
19	D13	IO4U	44	$\overline{RCS0}$	O4	69	GND	P	94	CB	O4
20	D6	IO4	45	$\overline{RCS1}$	O4	70	GND	P	95	$\overline{IOIS16}$	O4
21	D12	IO4U	46	RA10	O4	71	TPDN	AO	96	$\overline{IREQ}$	O8
22	D5	IO4	47	RA0	O4	72	TPDP	AO	97	$\overline{WAIT}$	O4
23	D11	IO4U	48	RA1	O4	73	TPON	AO	98	D10	IO4U
24	D4	IO4	49	RA2	O4	74	TPOP	AO	99	D2	IO4
25	D3	IO4	50	RA3	O4	75	VDD	P	100	D9	IO4U

Legend:

I:	Input (TTL level)
O4, O8:	Output with IOL = 4 or 8 mA
OD16:	Output Open Drain with IOL = 16 mA
IO4, IO4U:	Input (TTL level) and Output with IOL = 4 mA; IO4U refers to IO4 with an internal pull-up resistor
CI:	CMOS level input
SI:	Schmitt trigger input
TI:	Three-state input. May be connected to low, high, or left open.
AI:	Analog input
AO:	Analog output
P:	Power
R:	Resistor to ground
O:	Output

Pin Assignment Table - Generic Bus Mode - 100-Pin TQFP

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	HD1	IO4	26	RD8	IO4U	51	RA4	O4	76	DON	AO
2	HD8	IO4U	27	RD9	IO4U	52	RA5	O4	77	DOP	AO
3	HD0	IO4	28	RD10	IO4U	53	RA6	O4	78	AGND	P
4	HA0	I	29	RD11	IO4U	54	GND	P	79	REXT	R
5	HA1	I	30	RD12	IO4U	55	VDD	P	80	AVDD	P
6	HA2	I	31	RD13	IO4U	56	RA7	O4	81	TPIN	AI
7	HA3	I	32	RD14	IO4U	57	RA12	O4	82	TPIP	AI
8	RESET	SI	33	RD15	IO4U	58	RA14	O4	83	MODE	TI
9	VDD	P	34	GND	P	59	$\overline{\text{RWE}}$	O4	84	DIN	AI
10	GND	P	35	RD0	IO4U	60	RA13	O4	85	DIP	AI
11	$\overline{\text{WR}}$	I	36	RD1	IO4U	61	RA8	O4	86	CIN	AI
12	$\overline{\text{RD}}$	I	37	RD2	IO4U	62	RA9	O4	87	CIP	AI
13	$\overline{\text{BHE}}$	I	38	RD3	IO4U	63	RA11	O4	88	GND	P
14	HD15	IO4U	39	RD4	IO4U	64	$\overline{\text{ROE}}$	O4	89	$\overline{\text{DMACK}}$	SI
15	$\overline{\text{CS}}$	I	40	RD5	IO4U	65	RA15	O4	90	DMREQ	O8
16	HD14	IO4U	41	RD6	IO4U	66	OSCI	CI	91	EOP	I
17	HD7	IO4	42	RD7	IO4U	67	OSCO	O	92	RRST	O4
18	GND	P	43	GND	P	68	VDD	P	93	LEDLT	OD16
19	HD13	IO4U	44	$\overline{\text{RCS0}}$	O4	69	GND	P	94	CB	O4
20	HD6	IO4	45	$\overline{\text{RCS1}}$	O4	70	GND	P	95	HWORD	O4
21	HD12	IO4U	46	RA10	O4	71	TPDN	AO	96	$\overline{\text{INT}}$	O8
22	HD5	IO4	47	RA0	O4	72	TPDP	AO	97	READY	O4
23	HD11	IO4U	48	RA1	O4	73	TPON	AO	98	HD10	IO4U
24	HD4	IO4	49	RA2	O4	74	TPOP	AO	99	HD2	IO4
25	HD3	IO4	50	RA3	O4	75	VDD	P	100	HD9	IO4U

Legend:

I:	Input (TTL level)
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OD16:	Output Open Drain with IOL = 16 mA
IO4, IO4U:	Input (TTL level) and Output with IOL = 4 mA; IO4U refers to IO4 with an internal pull-up resistor
CI:	CMOS level input
SI:	Schmitt trigger input
TI:	Three-state input. May be connected to low, high, or left open.
AI:	Analog input
AO:	Analog output
P:	Power
R:	Resistor to ground
O:	Output

PIN DESCRIPTION

HOST BUS INTERFACE - PCMCIA BUS MODE

<table>
<tr><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RESET</td><td>I</td><td>HARDWARE RESET. Active high. A minimum pulse length of 800 ns is required. This pin resets the 8373's internal pointers and registers to their appropriate states. It also clears the CI (Configuration Index) in the CCR (Card Configuration Register), thus placing the 8373 in an unconfigured (Memory-only Interface) state. The 8373 remains in the unconfigured state until the CI has been written with a non-zero value.</td></tr>
<tr><td>$\overline{IOWR}$</td><td>I</td><td>I/O WRITE. The $\overline{IOWR}$ pin is an active low input that enables a write operation by the host to the 8373 internal registers as selected by the host address inputs A[0:3]. The $\overline{REG}$ and at least one of $\overline{CE1}$ or $\overline{CE2}$ must be also active for the I/O write to take place. The 8373 will not respond to the $\overline{IOWR}$ signal until it has been configured for I/O operation by the host.</td></tr>
<tr><td>$\overline{IORD}$</td><td>I</td><td>I/O READ. The $\overline{IORD}$ pin is an active low input that enables a read operation by the host from the 8373 internal registers as selected by the host address inputs A[0:3]. The $\overline{REG}$ and at least one of $\overline{CE1}$ or $\overline{CE2}$ must be also active for the I/O read to take place. The 8373 will not respond to the $\overline{IORD}$ signal until it has been configured for I/O operation by the host.</td></tr>
<tr><td>$\overline{CE1}$, $\overline{CE2}$</td><td>I</td><td>CHIP ENABLE. Active low input signals acting as chip select for the 8373. $\overline{CE1}$ enables even-numbered address bytes and $\overline{CE2}$ enables odd-numbered address bytes. When the 8373 is programmed to be in byte mode (DLCR6<5> HBYTE bit is a "1"), $\overline{CE2}$ is a don't care and only lower databus D[0:7] is used for data transfer. Combinations of $\overline{CE1}$, $\overline{CE2}$, A0 and HBYTE bit (DLCR6<5>) are used to select the different modes of I/O space word/byte transfer according to the following table (the table assumes $\overline{REG}$ is activated):
<table>
<tr><th>HBYTE</th><th>$\overline{CE2}$</th><th>$\overline{CE1}$</th><th>A0</th><th>D[15:8]</th><th>D[7:0]</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>X</td><td>even-byte</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X</td><td>odd-byte</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>odd-byte</td><td>even-byte</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>X</td><td>odd-byte</td><td>X</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>0</td><td>X</td><td>even-byte</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>1</td><td>X</td><td>odd-byte</td></tr>
</table>
For Attribute Memory access, data transfer occurs only on D[7:0] with the following valid combinations only:
<table>
<tr><th>HBYTE</th><th>$\overline{CE2}$</th><th>$\overline{CE1}$</th><th>A0</th><th>D[15:8]</th><th>D[7:0]</th></tr>
<tr><td>X</td><td>X</td><td>0</td><td>0</td><td>X</td><td>even-byte</td></tr>
</table></td></tr>
<tr><td>CCRA</td><td>I</td><td>CARD CONFIGURATION REGISTER ADDRESS. This pin connects to PCMCIA higher address bit. A high (together with $\overline{REG}$ activation) on this bit selects the internal CCR registers and a low selects the external CIS (Card Information Structure) ROM/Flash memory.</td></tr>
<tr><td>$\overline{OE}$</td><td>I</td><td>OUTPUT ENABLE. An active low input signal used to read data from the internal CCR (Card Configuration Registers) and from the external Attribute Memory (through the activation of $\overline{FCE}$ and $\overline{ROMG}$). This $\overline{OE}$ should also connect to the output enable of the external Flash Memory or the ROM.</td></tr>
</table>

HOST BUS INTERFACE - PCMCIA BUS MODE (continued)

NAME	TYPE	DESCRIPTION
$\overline{WE}$	I	WRITE ENABLE. An active low input signal used to write data to the internal CCR (Card Configuration Registers) and to the external Attribute (Flash) Memory (through the activation of $\overline{FCE}$). This $\overline{WE}$ should also connect to the write enable of the external Flash Memory.
$\overline{REG}$	I	ATTRIBUTE MEMORY SELECT. When this signal is active (low), it signifies access from or to the Attribute Memory ($\overline{OE}$ or $\overline{WE}$ active) or the I/O space ($\overline{IORD}$ or $\overline{IOWR}$ active). Attribute Memory is generally used to record card capacity and other configuration and attribute information. This includes the standardized CCRs (Card Configuration Registers) which are located internally in the 8373. When Attribute Memory is accessed, only data signals D[0:7] are valid and signals D[8:15] are ignored.
A[0:3]	I	ADDRESS BUS. Selects the set of 8373 internal registers including the CCR (Card Configuration Registers) for read or write operations.
D[0:15]	I/O	DATA BUS. A bi-directional, tri-state bus. The combinations of $\overline{CE1}$, $\overline{CE2}$ and A0 control the portion of the bus that is being utilized. A[0:3] and RBNK1,0 (DLCR7<3:2>) select the set of internal registers for access.

HOST BUS INTERFACE - PCMCIA BUS MODE

The following output signals are inactive (high) until the 8373 is configured for I/O mode.

$\overline{WAIT}$	O	$\overline{WAIT}$. An active low output that is asserted to delay completion of the current I/O read or write operation. It will also be used if the device is unable to respond to read or write requests within 2.4 µs. In these situations, the 8373 will also assert $\overline{IREQ}$ and the host read error status bit (DLCR1<6>) or host write error status bit (DLCR0<0>).
$\overline{INPACK}$	O	INPUT ACKNOWLEDGE. This active low output signal is asserted when the 8373 is selected and it can respond to an I/O read cycle requested by the host. This signal is used by the host to control the enable of any input data buffer between the card and the CPU. This signal will only be active after the 8373 is configured for I/O mode.
$\overline{IOIS16}$	O	I/O IS 16 BIT PORT. This active low output signal is asserted when the 8373 is configured for word transfer to indicate to the host that it is capable of 16-bit access. Therefore, this pin follows the register bit HBYTE (DLCR6<5>) once the 8373 is configured for I/O mode.
$\overline{IREQ}$	O	INTERRUPT REQUEST. This signal is available only after the 8373 is configured for I/O mode. It is asserted when the 8373 requires the intervention of the Host in situations as depicted in DLCR0,1 and BMR15. The IREQ signal is masked by writing a "0" to the respective interrupt enable register. To comply to with PCMCIA 2.0 spec, the 8373 supports both Pulsed- and Level- Mode interrupts as selected by the LevlREQ (CCR0<6>) register bit.
$\overline{SPKR}$	O	SPEAKER. This signal is held inactive (i.e. high) until the 8373 is configured for I/O mode. It provides a single-amplitude, on-off, binary audio waveform intended to drive the host's loudspeaker. The source for the signal is SPKRIN.

PIN DESCRIPTION (continued)

PCMCIA APPLICATION PINS

NAME	TYPE	DESCRIPTION
$\overline{\text{ROMG}}$	O	ROM ENABLE. Active low. This signal will be activated when an attribute memory read is performed on the external CIS memory.
$\overline{\text{FCE}}$	O	FLASH MEMORY CHIP ENABLE. Active low. The flash memory $\overline{\text{WE}}$ (Write Enable) and $\overline{\text{OE}}$ (Output Enable) come from PCMCIA pins $\overline{\text{WE}}$ and $\overline{\text{OE}}$.
$\overline{\text{XPD}}$	O	EXTERNAL POWER DOWN. Active low. When the 8373 enters power down mode, this pin will be low. It can be used to control power down of external devices residing on the same card.
XRST	O	EXTERNAL RESET. Active high. This pin is a reflection of CCR0<7> register bit. This allows a software controlled hardware reset of the 8373 and the rest of the devices residing on the same card.
SPKRIN	I	SPEAKER IN. This pin is qualified with the AUDIO bit, CCR1<3> to produce the inverted $\overline{\text{SPKR}}$ output.

HOST BUS INTERFACE - GENERIC BUS MODE

<table>
<tr><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RESET</td><td>I</td><td>HARDWARE RESET. Active high. A minimum pulse length of 800 ns is required. This pin resets the 8373's internal pointers and registers to their appropriate states. Note: the 8373 must be reset after power on before usage.</td></tr>
<tr><td>READY</td><td>O</td><td>READY. This output is asserted to indicate to the host that the 8373 is ready to complete the requested read or write operation. It will also be used if the device is unable to respond to read or write requests within 2.4 µs. In these situations, the 8373 will also assert $\overline{INT}$ and the host read error status bit (DLCR1 <6>) or host write error status bit (DLCR0 <0>). The polarity of the READY pin is determined by the MODE pin.</td></tr>
<tr><td>$\overline{WR}$</td><td>I</td><td>WRITE. The $\overline{WR}$ pin is an active low input that enables a write operation from the host to the 8373's internal registers as selected by the host address inputs HA[0:3].</td></tr>
<tr><td>$\overline{RD}$</td><td>I</td><td>READ. The $\overline{RD}$ pin is an active low input that enables a read operation by the host from the 8373's internal registers as selected by the host address inputs HA[0:3].</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>CHIP SELECT. An active low input signal as the chip select for the 8373.</td></tr>
<tr><td>$\overline{BHE}$</td><td>I</td><td>BYTE HIGH ENABLE. This is an active low byte/word control pin used only when the 8373 is configured for word transfer by HBYTE bit (DLCR6 <5>). Combinations of $\overline{BHE}$ and HA0 are used to select word, upper byte only or lower byte only transfers.
<table>
<tr><th>HBYTE</th><th>$\overline{BHE}$</th><th>HA0</th><th>FUNCTION</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Byte transfer on high bus HD[8:15].</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Byte transfer on low bus HD[0:7].</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Byte transfer (HD[0:7])</td></tr>
</table></td></tr>
<tr><td>$\overline{INT}$</td><td>O</td><td>INTERRUPT. This active low signal is asserted when the 8373 requires the intervention of the Host in situations as depicted in DLCR0,1 and BMR15. The $\overline{INT}$ signal is masked by writing a '0' to the respective interrupt enable register.</td></tr>
<tr><td>EOP</td><td>I</td><td>END OF PROCESS. Asserted at the end of a DMA transfer by the Host DMA controller. Further DMA requests (DMREQ) will be discontinued after EOP is asserted. Polarity can be selected via the register bit (DLCR7 <1>).</td></tr>
<tr><td>DMREQ</td><td>O</td><td>DMA REQUEST. The 8373 issues a DMREQ to the Host DMA controller to initiate a write to its transmit buffer or a read from its receive buffer.</td></tr>
</table>

PIN DESCRIPTION (continued)

HOST BUS INTERFACE - GENERIC BUS MODE

NAME	TYPE	DESCRIPTION
$\overline{\text{DMACK}}$	I	DMA ACKNOWLEDGE. An active low signal issued by the Host DMA controller when it is ready to perform data transfers between the Host and the 8373's buffer memory via BMR8.
HA[0:3]	I	HOST ADDRESS. Selects the set of internal registers to be accessible by the 8373 for read or write operations.
HD[0:15]	I/O	HOST DATA BUS. A bi-directional, tri-state bus for data, command and status transfers between the Host and the 8373 with the direction being controlled by $\overline{\text{RD}}$ and $\overline{\text{WR}}$. The combinations of HBYTE, $\overline{\text{BHE}}$ and HA0 control the portion of the bus that is being utilized. HA[0:3] and RBNK <0:1> (DLCR7 <2:3>) select the set of internal registers for access.
HWORD	O	HOST WORD CONFIGURATION. This pin is the complement of the register bit HBYTE (DLCR6 <5>). If HBYTE is a '0', the Host interface is configured for word transfers. If HBYTE is a '1', the Host interface is configured for byte transfers on the lower bus, HD[0:7].

BUFFER MEMORY INTERFACE

$\overline{\text{RCS0}}$, $\overline{\text{RCS1}}$	O	RAM CHIP SELECT. $\overline{\text{RCS0}}$ and $\overline{\text{RCS1}}$ are active low chip select lines for the SRAM with $\overline{\text{RCS0}}$ as the least significant byte.
$\overline{\text{ROE}}$	O	RAM OUTPUT ENABLE. Active low. This is the output enable asserted by the 8373 during buffer memory read cycles for the SRAM.
$\overline{\text{RWE}}$	O	RAM WRITE ENABLE. Active low. This is the write enable asserted by the 8373 during buffer memory write cycles for the SRAM.
RD[0:15]	I/O	RAM DATA BUS. This is the data bus between the 8373 and the buffer memory. It can be configured for byte or word transfer depending on register bit RBYTE (DLCR6 <4>) RAM BYTE. For word transfers, the ordering of the most and least significant byte is defined by the register bit, INTLMOT (DLCR7 <0>). In PCMCIA bus mode, this data bus is only 8 bits wide (RD[0:7]).
RA[0:15]	O	RAM ADDRESS BUS. Addresses up to 64 KByte of SRAM buffer memory.

NETWORK ATTACHMENT UNIT INTERFACE

DON, DOP	O	TRANSMIT DATA NEGATIVE and POSITIVE. Differential outputs to external transceiver for transmission.
DIN, DIP	I	RECEIVE DATA NEGATIVE and POSITIVE. Manchester differential inputs from external transceiver for reception.
CIN, CIP	I	COLLISION DETECT NEGATIVE and POSITIVE. When an externally connected transceiver detects a collision on the medium, these differential inputs are driven by a 10 MHz signal.
REXT	-	EXTERNAL RESISTOR. External biasing resistor. Connect to 20 kΩ ±1% to AGND.

NETWORK TWISTED-PAIR MEDIUM INTERFACE

NAME	TYPE	DESCRIPTION
TPON, TPOP	O	TWISTED-PAIR OUTPUT NEGATIVE and POSITIVE. Driver outputs to twisted-pair medium. Must be summed together with TPDN and TPDP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPDN, TPDP	O	TWISTED-PAIR DELAYED NEGATIVE and POSITIVE. Delayed (50 ns) driver outputs to twisted-pair medium. Must be summed together with TPON and TPOP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPIN, TPIP	I	TWISTED-PAIR INPUT NEGATIVE and POSITIVE. Inputs from twisted-pair medium.

DEVICE POWER

VDD	P	POWER SUPPLY. A +5V DC (±5%) or +3.3 VDC (±0.3V) supply is required.
GND	P	SYSTEM GROUND.
AVDD	P	ANALOG VDD. The analog VDD pin required by the internal AUI and twisted-pair circuits is to be connected to a different VDD path from the digital VDD. A +5V DC (±5%) or +3.3 VDC (±0.3V) supply is required.
AGND	P	ANALOG GROUND. The analog ground required by the internal encoder/decoder is to be connected to a separate GND path from the digital GND.

CRYSTAL OSCILLATOR

OSCI	I	OSCILLATOR IN. Connection for one side of the 20 MHz crystal or an input for an external 20 MHz clock source.
OSCO	O	OSCILLATOR OUT. Connection for other side of the 20 MHz crystal. Left unconnected if an external clock is used.

MISCELLANEOUS

CB	O	CONTROL BIT. A complement of the internal register bit, DLCR4 <2>, which is used to activate any external hardware.
RRST	O	REMOTE RESET. This pin follows the RMTRST register bit (DLCR1 <4>). The RMTRST bit is '1' only if a packet with the pattern 0900H in the Type Field is detected and ENA_RMTRST (DLCR5 <2>) is activated. This feature can be used by the nodes on the network to remotely-control external hardware.
MODE	I	MODE SELECT. Tied high to select Generic bus mode with active high READY timing. Tied low to select Generic bus mode with active low READY timing. Left open to select PCMCIA bus mode (it will be internally pulled up).
LEDLT	O	LED LINK, TRANSMIT. Connect to LED with current limiting resistor to VDD. LED is on during link up and off during link down. During link up (when LED is on), a transmission will blink off the LED temporarily to indicate activity. This feature is available for both twisted pair and AUI interfaces.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Supply voltage, Vdd	-0.5 to 6.0V
Input voltage, Vin	-0.5 to Vdd + 0.5V
Output voltage, Vout	-0.5 to Vdd + 0.5V
Storage temperature, Tstg	-55 to 150°C
Lead temperature (max 10 sec soldering), Tl	235°C (IR)

DC CHARACTERISTICS (Ta = 0 to 70°C, Vdd = 5V ±5%, 5V Values)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Low level input voltage	Vil	TTL inputs			0.8	V
		OSCI pin			1.6	V
		Schmitt inputs			1.1	V
High level input voltage	Vih	TTL inputs	2.2			V
		OSCI pin	3.8			V
		Schmitt inputs	3.5			V
Pull down current (RESET pin)	Ipd		13		50	µA
Low level output voltage	Vol	Rated Iol	0		0.4	V
High level output voltage	Voh	Rated Ioh	2.4		Vdd	V
Low level output current	Iol	Pin types O4, IO4, IO4U Vdd = 5V	4			mA
(with Vol = 0.4V)		Pin type O8 Vdd = 5V	8			mA
		Pin type OD16 Vdd = 5V	16			mA
High level output current	Ioh	Pin types O4, IO4, IO4U Vdd = 5V	-4			mA
(with Voh = 2.4V)		Pin type O8 Vdd = 5V	-8			mA
Leakage current (input/output)	Il		-10		10	µA
Supply current	Idd	Fully active(1)			40	mA
		Idle			30	mA
Power down supply current	Ipwrdn	Osc. on			10	mA
		Osc. off			100	µA

Note: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

DC CHARACTERISTICS (Ta = 0 to 70°C, Vdd = 3.3V ±0.3V, 3V Values)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Low level input voltage	Vil	TTL inputs			0.8	V
		OSCI pin			0.7	V
		Schmitt inputs			0.4	V
High level input voltage	Vih	TTL inputs	2			V
		OSCI pin	2.1			V
		Schmitt inputs	2.4			V
Pull down current (RESET pin)	Ipd		5		28	µA
Low level output voltage	Vol	Rated Iol	0		0.4	V
High level output voltage	Voh	Rated Ioh	2.4		Vdd	V
Low level output current	Iol	Pin types O4, IO4, IO4U Vdd = 3.3V	2.4			mA
(with Vol = 0.4V)		Pin type O8 Vdd = 3.3V	4.9			mA
		Pin type OD16 Vdd = 3.3V	9.8			mA
High level output current	Ioh	Pin types O4, IO4, IO4U Vdd = 3.3V	-1.5			mA
(with Voh = 2.4V)		Pin type O8 Vdd = 3.3V	-3			mA
Leakage current (input/output)	Il		-10		10	µA
Supply current	Idd	Fully active(1)			28	mA
		Idle			20	mA
Power down supply current	Ipwrdn	Osc. on			6	mA
		Osc. off			100	µA

Note: (1) Fully active means 3 “simultaneous” operations: transmitting, receiving (through twisted-pair port) and either host write or read.

ELECTRICAL SPECIFICATIONS (continued)

AUI CHARACTERISTICS

(VDD = 5V ± 5%, 3.3 ± 0.3V, Vss = 0V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Low Output Voltage for DOP, DON Vaol	Rext = 20 kΩ Rl = 78Ω	Vdd-1.5		Vdd-0.75	V
High Output Voltage for DOP, DON Vaoh	Rext = 20 kΩ Rl = 78Ω	Vdd-0.55		Vdd	V
DOP, DON Output Current Iao	Rext = 20 kΩ	8		14	mA
DIP, DIN, CIP, CIN Open Circuit Input Voltage (bias) Valb	Vdd = 5V ± 5% Vdd = 3.3 ± 0.3V	2.45 2.13		3.33 2.88	V
DIP, DIN, CIP, CIN Diff Squelch Threshold Vasq		-300		-120	mV
DOP, DON Diff Idle Output Vadi	Rl = 78Ω	-40		40	mV
DOP, DON Diff Peak Output Vadv	Rext = 20 kΩ Rl = 78Ω	620		1100	mV
DOP, DON Output Resistance Rao				75	Ω

TWISTED PAIR
(VDD = 5V ± 5%, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.45		3.33	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 5V	-3.1		3.1	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	300		585	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-585		-300	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		180		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-180		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	120		300	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-300		-120	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		100		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-100		mV
TPOP, TPON High Output Voltage Vtoh	I = 32 mA	Vddtp -0.44		Vddtp	V
TPOP, TPON Low Output Voltage Vtol	I = 32 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN High Voltage Vtdh	I = 16 mA	Vddtp -0.44		Vddtp	V
TPDP, TPDN Low Voltage Vtdl	I = 16 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN Output Resistance Rtd				27	Ω
TPOP, TPON Output ResistanceRto				13.5	Ω

Note 1: Sine wave at 2 MHz, 5 MHz and 7 MHz
Note 2: Sine wave : 5 MHz ≤ f ≤ 10 MHz

ELECTRICAL SPECIFICATIONS (continued)

TWISTED PAIR
(VDD = 3.3 ± 0.3V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.13		2.88	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 3.3V	-2.2		2.2	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	210		410	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-410		-210	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		130		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-130		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	90		210	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-210		-90	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		70		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-70		mV
TPOP, TPON High Output Voltage Vtoh	I = 50 mA	Vdd_{TP} -0.3		Vdd_{TP}	V
TPOP, TPON Low Output Voltage Vtol	I = 50 mA	Vss_{TP}		Vss_{TP} +0.3	V
TPDP, TPDN High Voltage Vtdh	I = 25 mA	Vdd_{TP} -0.3		Vdd_{TP}	V
TPDP, TPDN Low Voltage Vtdl	I = 25 mA	Vss_{TP}		Vss_{TP} +0.3	V
TPDP, TPDN Output Resistance Rtd				12	Ω
TPOP, TPON Output Resistance Rto				6	Ω

Note 1: Sine wave at 2 MHz, 5 MHz and 7 MHz
Note 2: Sine wave: 5 MHz ≤ *f* ≤ 10 MHz

TRANSFORMER RATIO:

5V OPERATION		3.3V OPERATION	
RX	TX	RX	TX
1:1	1:1	1:1.4 (step down)	1:1.4 (step down)

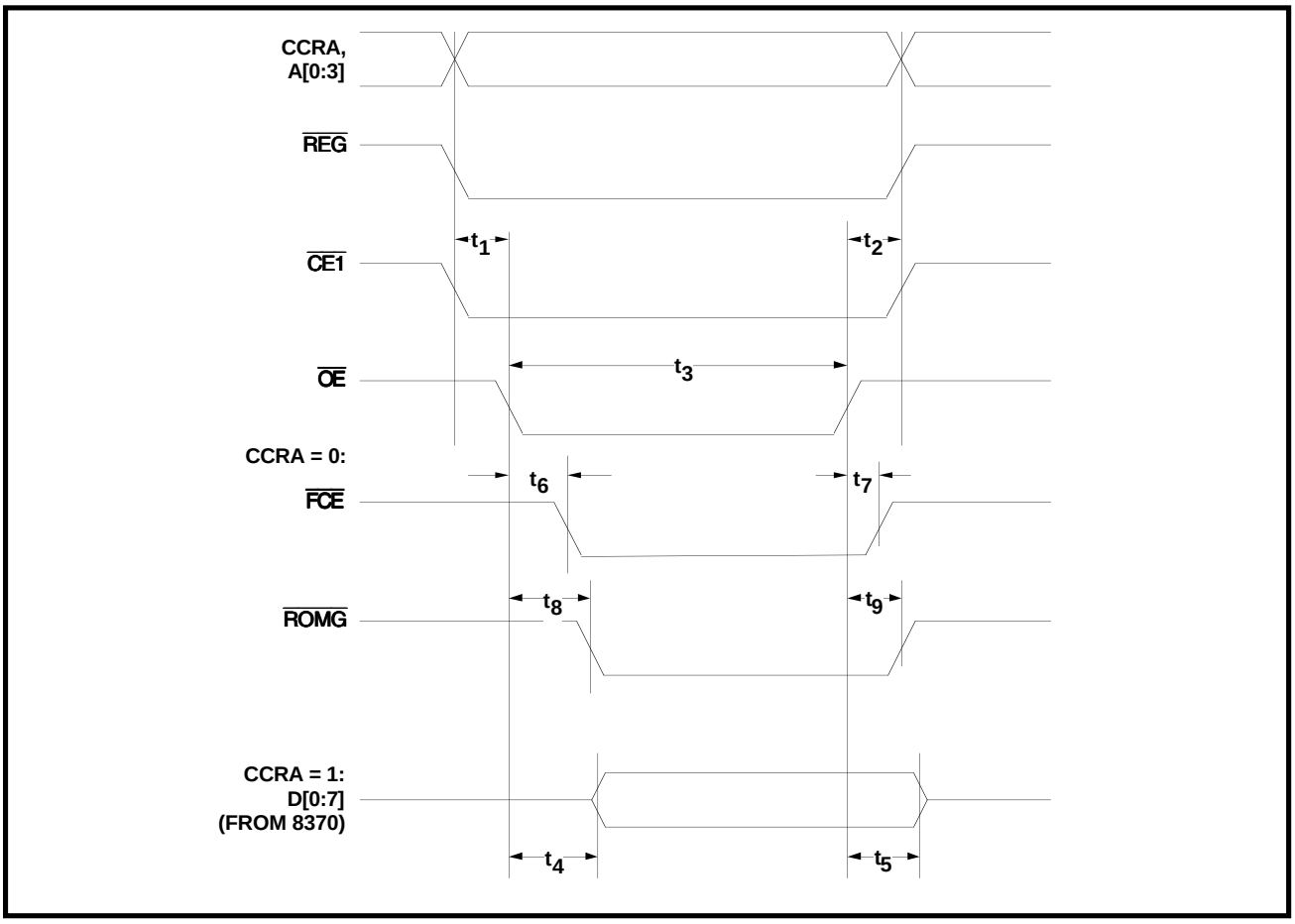


FIGURE 2: Attribute Memory Read Cycle (PCMCIA mode)

Unless otherwise stated, the following conditions apply to the remaining timing tables:
Ta = 0°C to +70°C, Vdd = 5 ± 5%, Vdd = 3.3V ± 0.3V

TABLE 1: Attribute Memory Read Cycle (PCMCIA mode) (Refer to Figure 2)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
CCRA, A[0:3] Valid to $\overline{OE}$ low; $\overline{REG}$, $\overline{CE1}$ low to $\overline{OE}$ low	t_1		0			ns
$\overline{OE}$ high to CCRA, A[0:3] invalid; $\overline{OE}$ high to $\overline{REG}$, $\overline{CE1}$ high	t_2		0			ns
$\overline{OE}$ low pulse width	t_3	Vdd = 5V	30			ns
		Vdd = 3.3V	35			ns
$\overline{OE}$ low to D[0:7] valid	t_4				45	ns
$\overline{OE}$ high to D[0:7] invalid (data hold)	t_5		10			ns
$\overline{OE}$ low to $\overline{FCE}$ low	t_6	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns
$\overline{OE}$ high to $\overline{FCE}$ high	t_7	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns
$\overline{OE}$ low to $\overline{ROMG}$ low	t_8	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns
OE high to ROMG high	t_9	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns

TABLE 2: Attribute Memory Write Cycle (PCMCIA MODE) (Refer to Figure 3)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
CCRA, A[0:3] Valid to $\overline{WE}$ low; $\overline{REG}$, $\overline{CE1}$ low to $\overline{WE}$ low	t_1		0			ns
$\overline{WE}$ high to CCRA, A[0:3] invalid; $\overline{WE}$ high to $\overline{REG}$, $\overline{CE1}$ high	t_2		0			ns
$\overline{WE}$ low pulse width	t_3	Vdd = 5V	30			ns
		Vdd = 3.3V	35			ns
D[0:7] valid to $\overline{WE}$ high (data setup)	t_4		15			ns
$\overline{WE}$ high to D[0:7] invalid (data hold)	t_5		10			ns
$\overline{WE}$ low to $\overline{FCE}$ low	t_6	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns
WE high to FCE high	t_7	Vdd = 5V			25	ns
		Vdd = 3.3V			35	ns

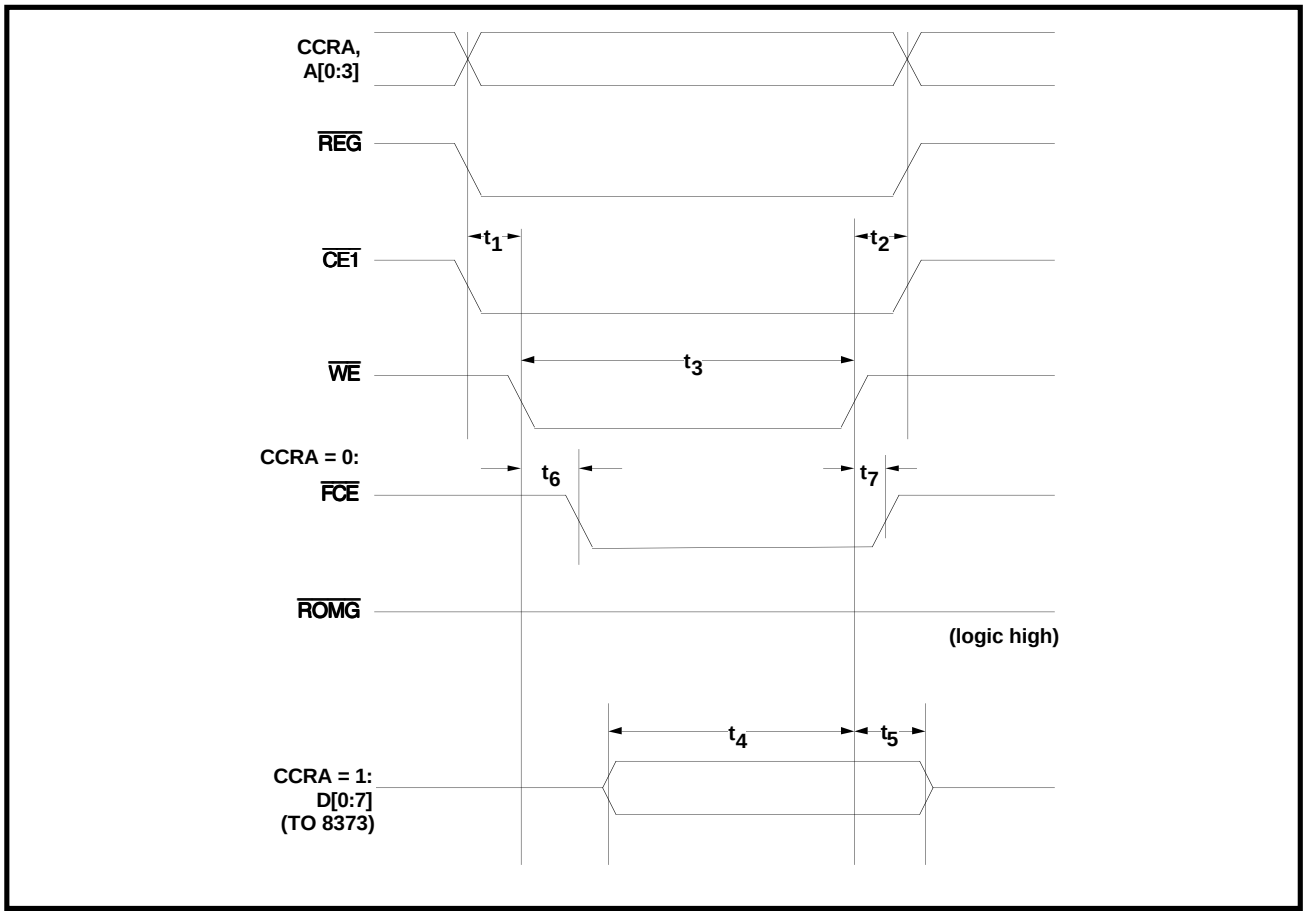


FIGURE 3: Attribute Memory Write Cycle (PCMCIA mode)

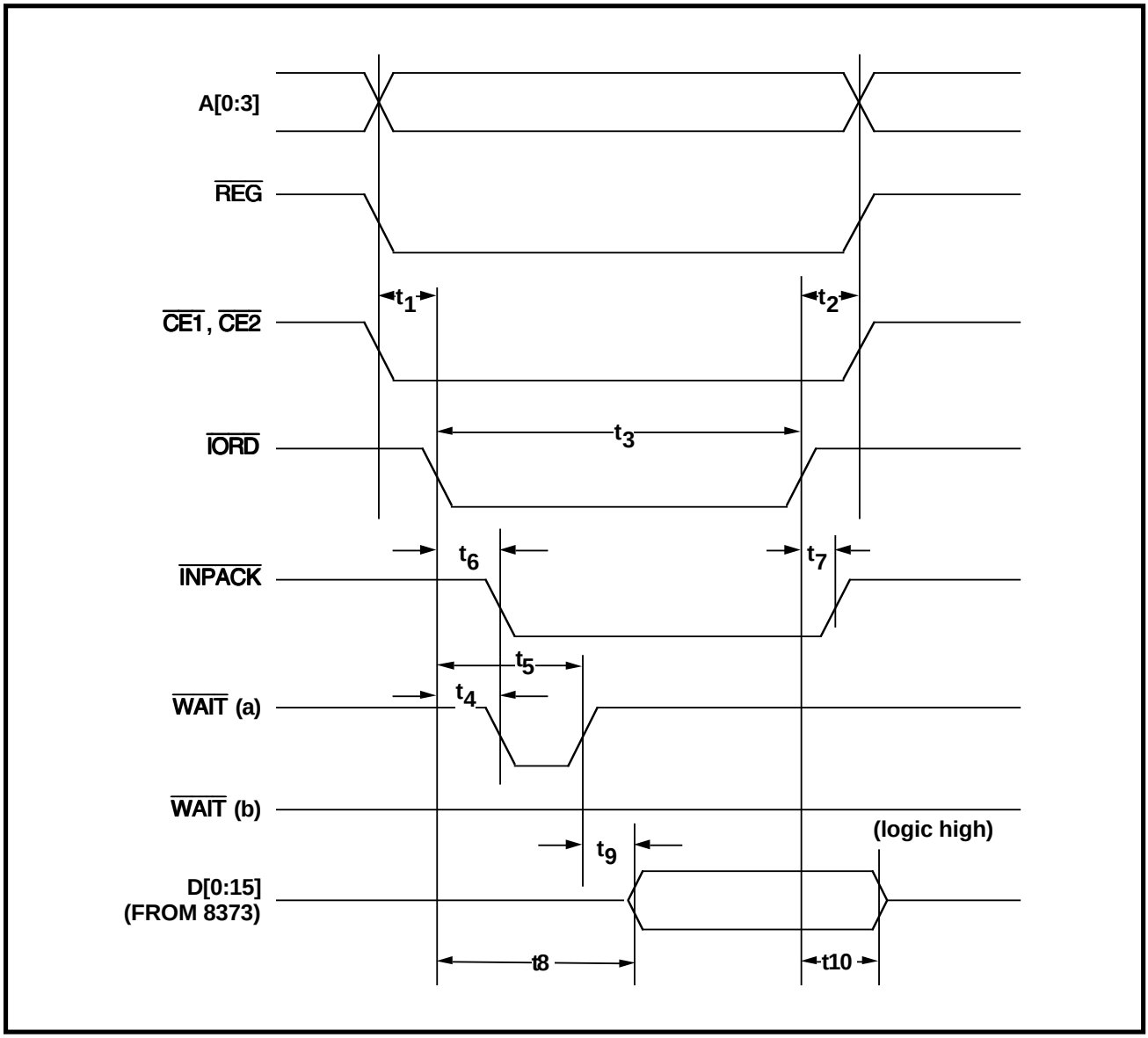


FIGURE 4: I/O Read Cycle (PCMCIA mode)

TABLE 3: I/O Read Cycle (PCMCIA mode) (Refer to Figure 4)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
A[0:3] valid to $\overline{IORD}$ LOW; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ low to $\overline{IORD}$ low	t_1			0			ns
$\overline{IORD}$ high to A[0:3] invalid; $\overline{IORD}$ high to $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ high	t_2			0			ns
$\overline{IORD}$ low pulse width	t_3		Vdd = 5V	30			ns
			Vdd = 3.3V	35			ns
$\overline{IORD}$ low to $\overline{WAIT}$ low	t_4	Port busy (a)	Vdd = 5V	0		35	ns
			Vdd = 3.3V			50	ns
$\overline{IORD}$ low to $\overline{WAIT}$ high(1)	t_5	Port busy (a)				350	ns
$\overline{IORD}$ low to $\overline{INPACK}$ low	t_6		Vdd = 5V			25	ns
			Vdd = 3.3V			35	ns
$\overline{IORD}$ high to $\overline{INPACK}$ high	t_7		Vdd = 5V			25	ns
			Vdd = 3.3V			35	ns
$\overline{IORD}$ low to D[0:15] valid	t_8	Register access (b)	Vdd = 5V			50	ns
			Vdd = 3.3V			70	ns
$\overline{WAIT}$ high to D[0:15] valid	t_9	Port busy (a)				5	ns
$\overline{IORD}$ high to D[0:15] invalid (data hold)	t_{10}			10			ns

TABLE 4: I/O Write Cycle (PCMCIA mode) (Refer to Figure 5)

A[0:3] valid to $\overline{IOWR}$ LOW; $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ low to $\overline{IOWR}$ low	t_1			0			ns
$\overline{IOWR}$ high to A[0:3] invalid; $\overline{IOWR}$ high to $\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$ high	t_2			0			ns
$\overline{IOWR}$ low pulse width	t_3		Vdd = 5V	30			ns
			Vdd = 3.3V	35			ns
$\overline{IOWR}$ low to $\overline{WAIT}$ low	t_4	Port busy (a)	Vdd = 5V			35	ns
			Vdd = 3.3V			50	ns
$\overline{IOWR}$ low to $\overline{WAIT}$ high(1)	t_5	Port busy (a)				350	ns
D[0:15] valid to $\overline{IOWR}$ high (data setup)	t_6			15			ns
$\overline{IOWR}$ high to D[0:15] invalid (data hold)	t_7			10			ns

Note: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host read error.

(a) For Buffer Memory Port when port is busy.

(b) For register or port is not busy.

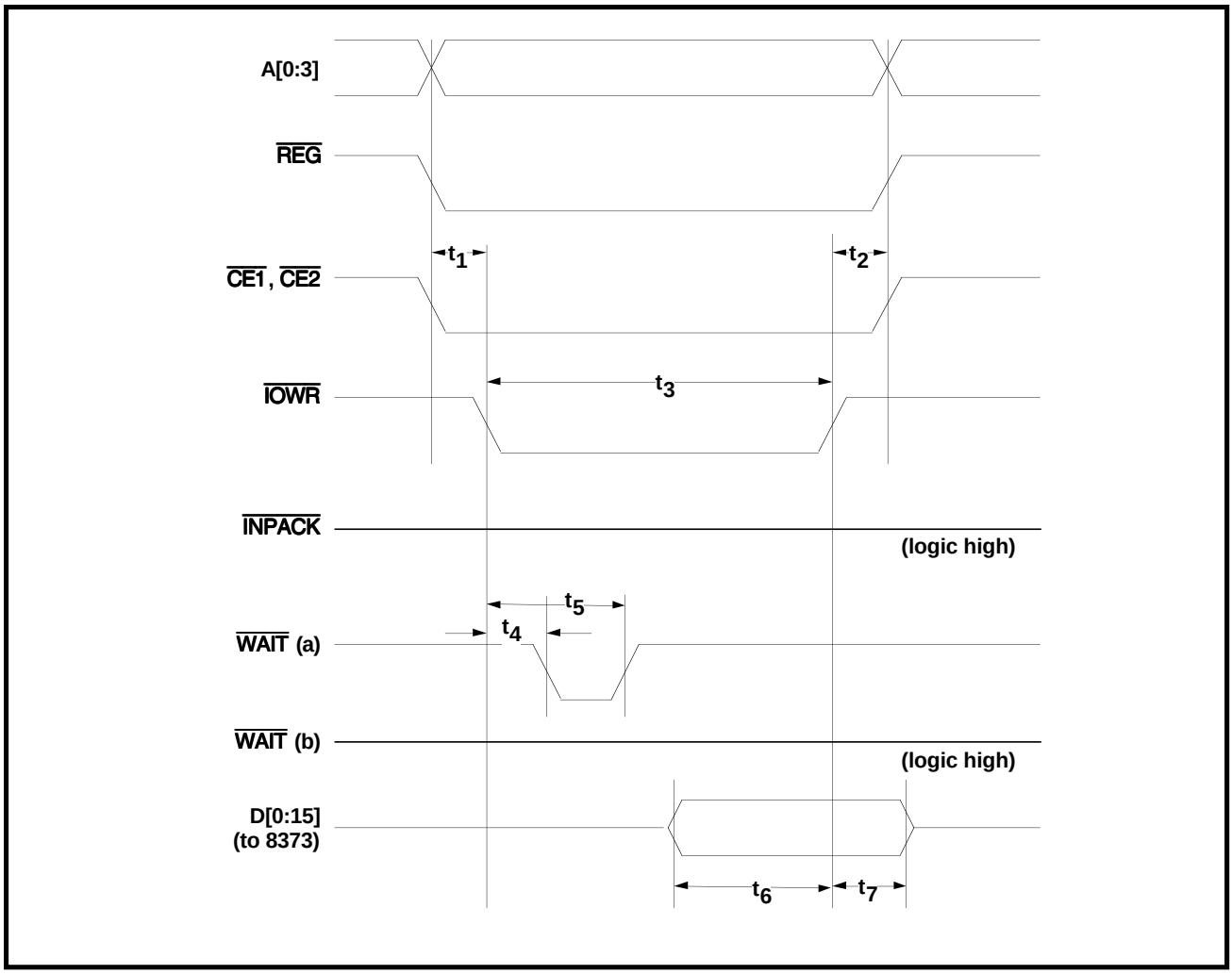


FIGURE 5: I/O Write Cycle (PCMCIA mode)

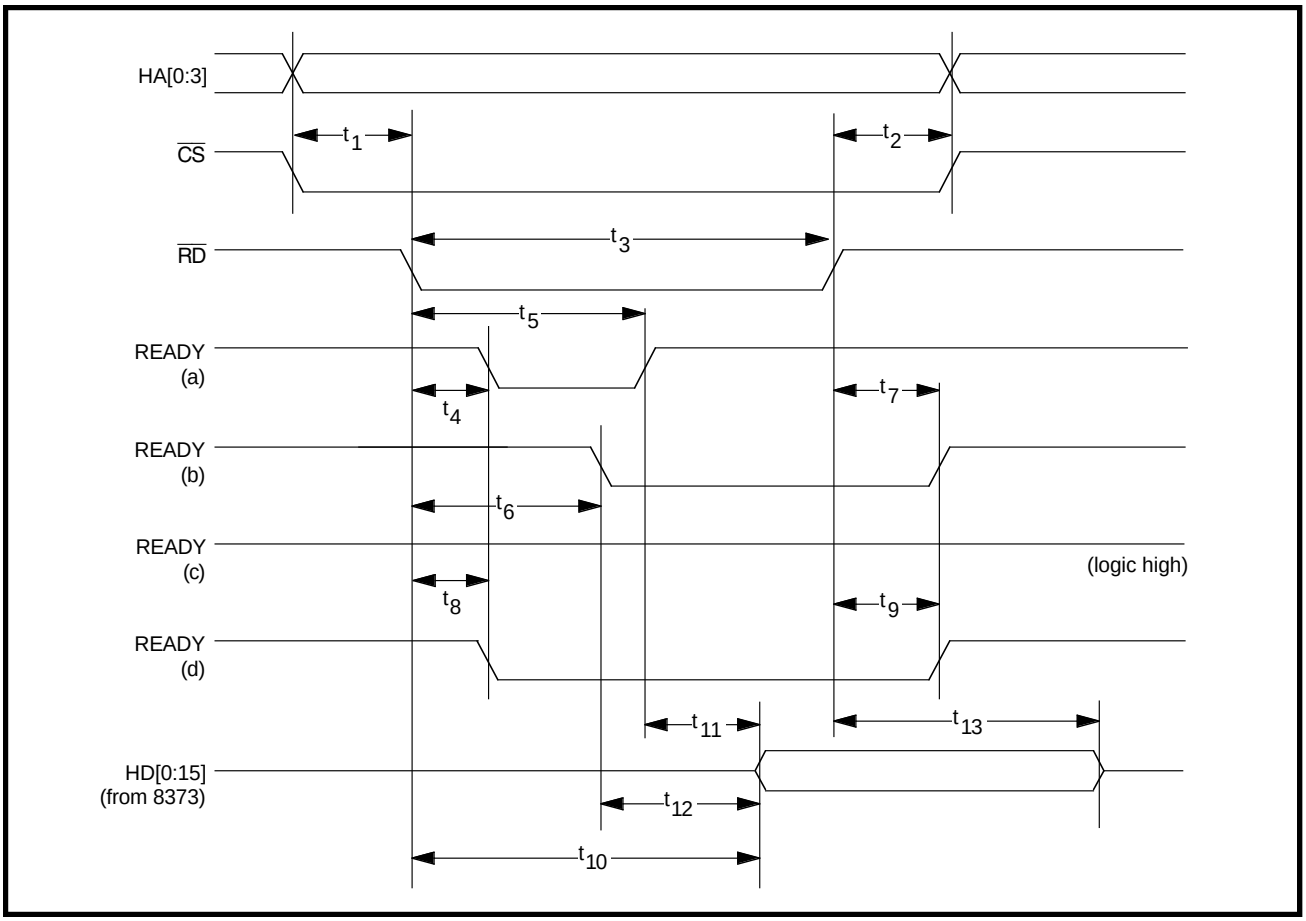


FIGURE 6: Read Cycle, Generic Bus Mode (Refer to Table 5)

TABLE 5: Read Cycle, Generic Bus Mode (Refer to Figure 6)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
$\overline{CS}$ low to $\overline{RD}$ low; HA[0:3] valid to $\overline{RD}$ low	t_1			0			ns
$\overline{RD}$ high to $\overline{CS}$ high; $\overline{RD}$ high to HA[0:3] invalid	t_2			0			ns
$\overline{RD}$ low pulse width	t_3		Vdd = 5V	30			ns
			Vdd = 3.3V	35			ns
$\overline{RD}$ low to READY low	t_4	(a)	Vdd = 5V	0		35	ns
			Vdd = 3.3V			45	ns
$\overline{RD}$ low to READY high (1)	t_5	(a)				350	ns
$\overline{RD}$ low to READY low (1)	t_6	(b)		0		350	ns
$\overline{RD}$ high to READY high	t_7	(b)		0		25	ns
$\overline{RD}$ low to READY low	t_8	(d)	Vdd = 5V	0		30	ns
			Vdd = 3.3V			40	ns
$\overline{RD}$ high to READY high	t_9	(d)		0		28	ns
$\overline{RD}$ low to HD[0:15] valid	t_{10}	Register access	Vdd = 5V			45	ns
			Vdd = 3.3V			60	ns
READY high to HD[0:15] valid	t_{11}	Port access				5	ns
READY low to HD[0:15] valid	t_{12}	Port access				5	ns
$\overline{RD}$ high to HD[0:15] invalid (data hold)	t_{13}			10			ns

Note: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in “loopback” reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host read error.
(a) For Buffer Memory Port when port is busy and RDYSEL = 1.
(b) For Buffer Memory Port when port is busy and RDYSEL = 0.
(c) For register or port is not busy and RDYSEL = 1.
(d) For register or port is not busy and RDYSEL = 0.

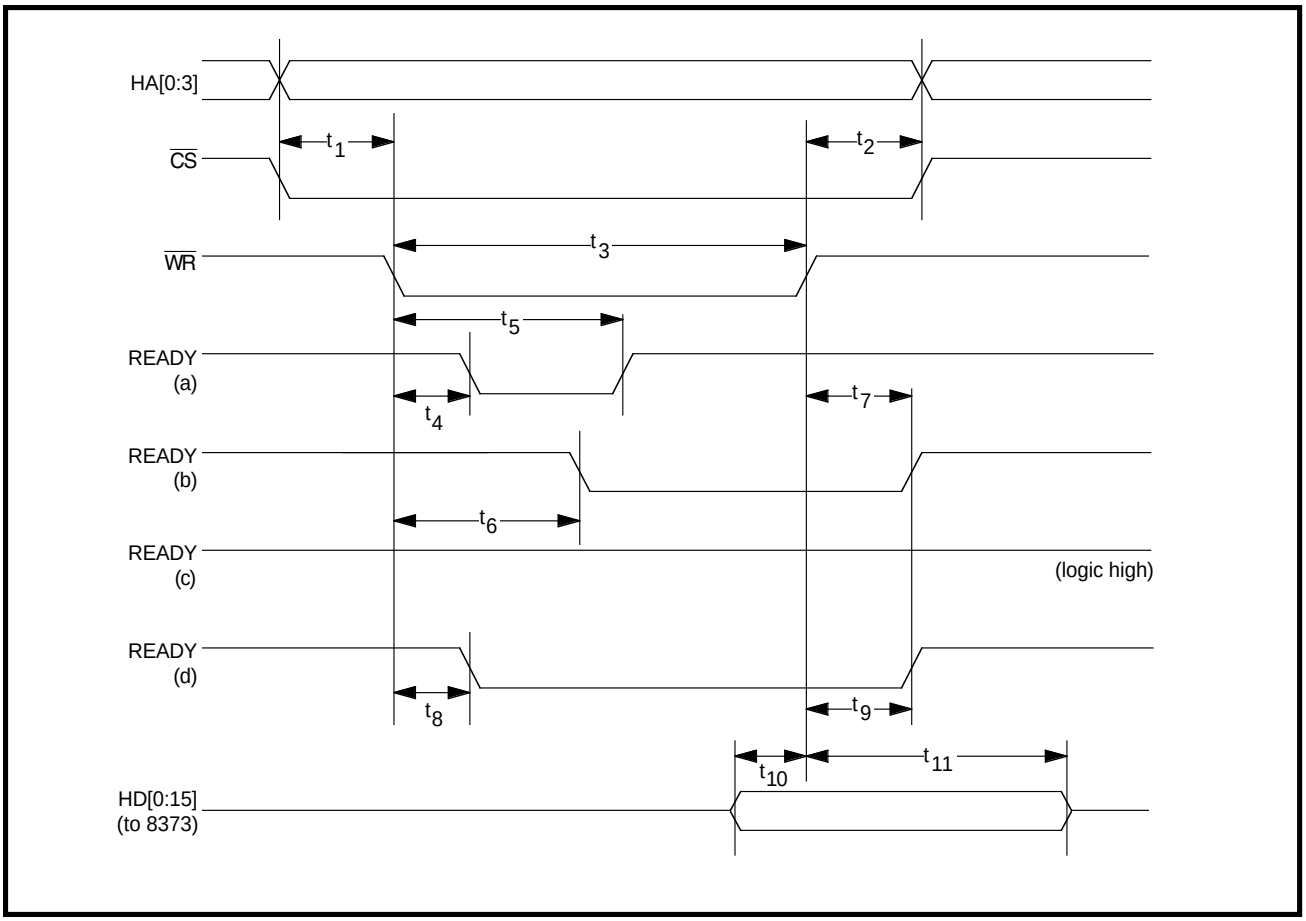


FIGURE 7: Write Cycle, Generic Bus Mode (Refer to Table 6)

TABLE 6: Write Cycle, Generic Bus Mode (Refer to Figure 7)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{CS}$ low to $\overline{WR}$ low; HA[0:3] valid to WR low	t_1		0			ns
$\overline{WR}$ high to $\overline{CS}$ high; $\overline{WR}$ high to HA[0:3] invalid	t_2		0			ns
$\overline{WR}$ low pulse width	t_3	Vdd = 5V	30			ns
		Vdd = 3.3V	35			ns
$\overline{WR}$ low to READY low	t_4	(a) Vdd = 5V	0		35	ns
		Vdd = 3.3V			45	ns
$\overline{WR}$ low to READY high (1)	t_5	(a)			350	ns
$\overline{WR}$ low to READY low (1)	t_6	(b)	0		350	ns
$\overline{WR}$ high to READY high	t_7	(b)			28	ns
$\overline{WR}$ low to READY low	t_8	(d) Vdd = 5V	0		30	ns
		Vdd = 3.3V			40	ns
$\overline{WR}$ high to READY high	t_9	(d)	0		25	ns
HD[0:15] valid to WR high (data setup)	t_{10}		15			ns
$\overline{WR}$ high to HD[0:15] invalid (data hold)	t_{11}		10			ns

Note: (1) Maximum of 350 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active on “loopback” reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host write error.
(a) For Buffer Memory Port when port is busy and RDYSEL = 1.
(b) For Buffer Memory Port when port is busy and RDYSEL = 0.
(c) For register or port is not busy and RDYSEL = 1.
(d) For register or port is not busy and RDYSEL = 0.

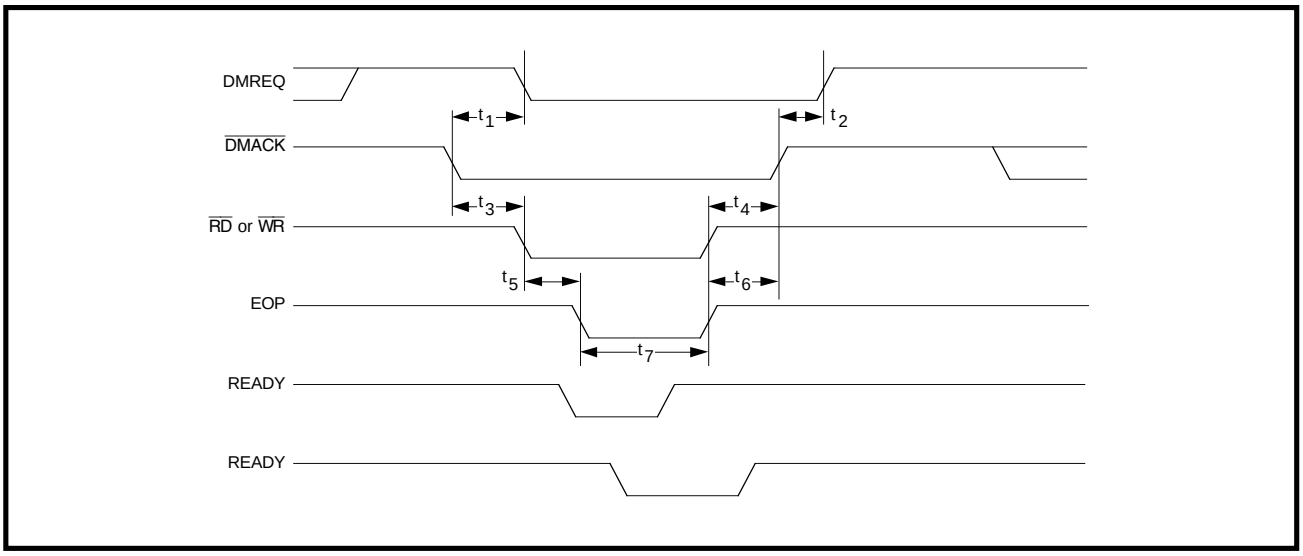


FIGURE 8: Single-Cycle DMA Timing

TABLE 7: Single-Cycle DMA Timing (Refer to Figure 8)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{DMACK}$ low to DMREQ low	t_1	Vdd = 5V	0		25	ns
		Vdd = 3.3V			30	ns
$\overline{DMACK}$ high to DMREQ high	t_2	Vdd = 5V	0		25	ns
		Vdd = 3.3V			30	ns
$\overline{DMACK}$ low to $\overline{RD}$ or $\overline{WR}$ low	t_3		0			ns
$\overline{RD}$ or $\overline{WR}$ high to $\overline{DMACK}$ high	t_4		0			ns
$\overline{RD}$ or $\overline{WR}$ low to EOP low	t_5		0			ns
EOP high to $\overline{DMACK}$ high	t_6		0			ns
EOP low pulse width	t_7		10			ns

Note: (1) An asserted EOP terminates any further DMREQ after $\overline{DMACK}$ returns high.
(2) The DMA cycle uses $\overline{DMACK}$ as the chip select. $\overline{DMACK}$ overrides $\overline{CS}$ and HA[0:3] if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
(3) For READY timing and HD[0:15] timing, see Figure 6, t_4-t_{13}, and Figure 7, t_4-t_{11}.

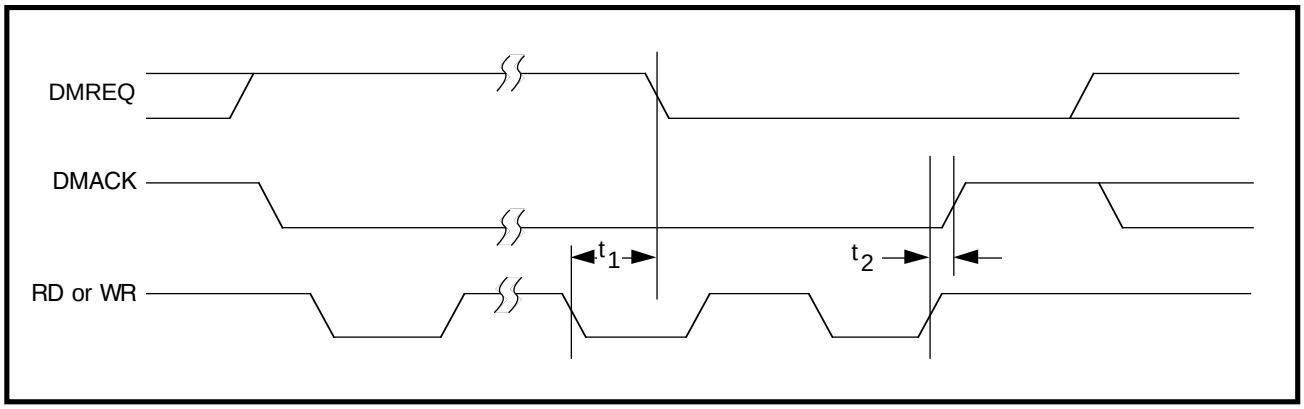


FIGURE 9: Burst DMA Timing

TABLE 8: Burst DMA Timing

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
$\overline{RD}$ or $\overline{WR}$ low to DMREQ low	5V	t_1			30	ns
	3.3V	t_1			40	ns
$\overline{RD}$ or $\overline{WR}$ high to DMACK high		t_2	0			ns

Note: (1) DMREQ goes low during the next-to-last transfer of the burst. $\overline{DMACK}$ should not go high until after the $\overline{RD}$ or $\overline{WR}$ pulse of the last transfer cycle goes high
(2) The DMA cycle uses $\overline{DMACK}$ as the chip select. $\overline{DMACK}$ overrides $\overline{CS}$ and HA[0:3] if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
(3) For READY timing and HD[0:15] timing, see Figure 6, t_4-t_{13}, and Figure 7, t_4-t_{11}.

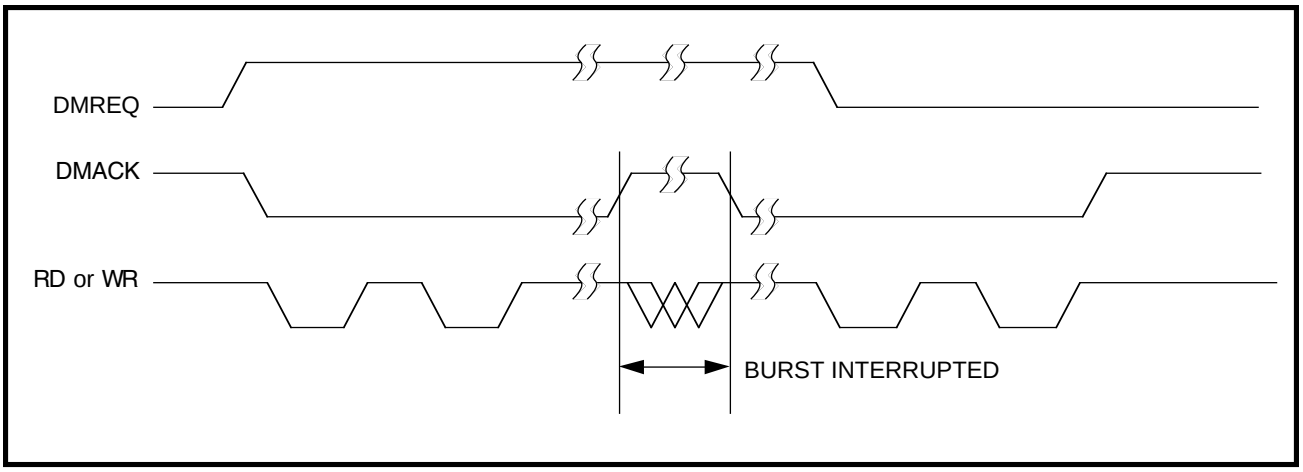


FIGURE 10: Burst DMA Interrupted by $\overline{\text{DMACK}}$

Note: Burst can be interrupted by $\overline{\text{DMACK}}$ high-going pulse during the burst. Burst will resume when $\overline{\text{DMACK}}$ returns low.

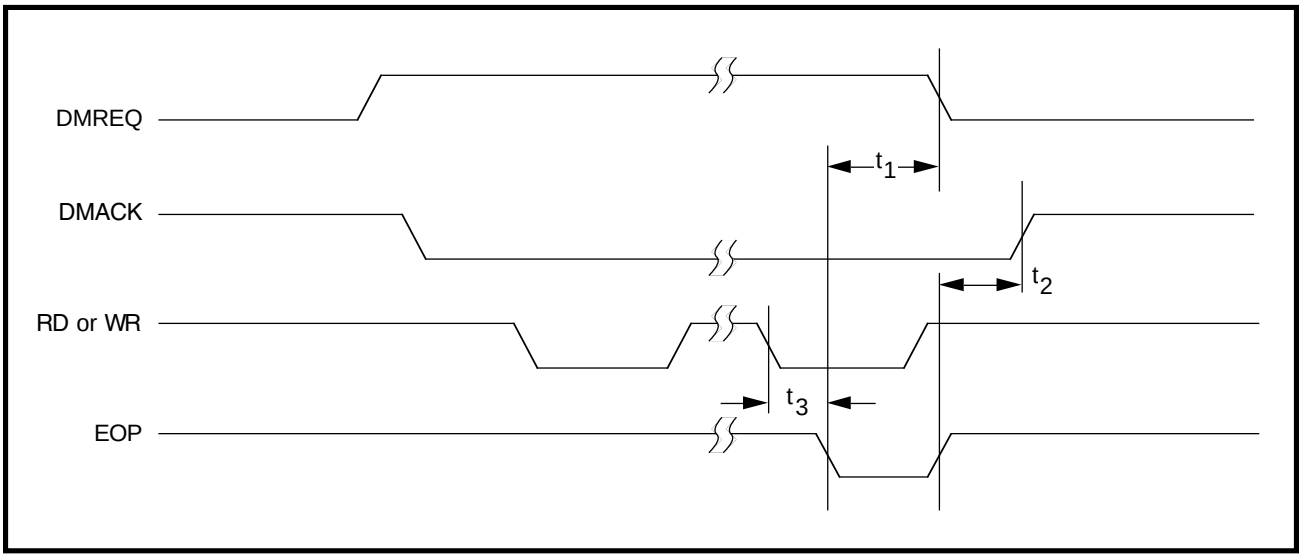


FIGURE 11: Burst DMA Terminated by EOP

TABLE 9: Burst DMA Terminated by EOP

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
EOP low to DMREQ low	t_1	Vdd = 5V	4		28	ns
		Vdd = 3.3V			35	ns
EOP high to DMACK high	t_2		3			ns
RD or WR low to EOP low	t_3		0			ns

Note: EOP can be asserted during any transfer of the burst to terminate the process following that transfer.

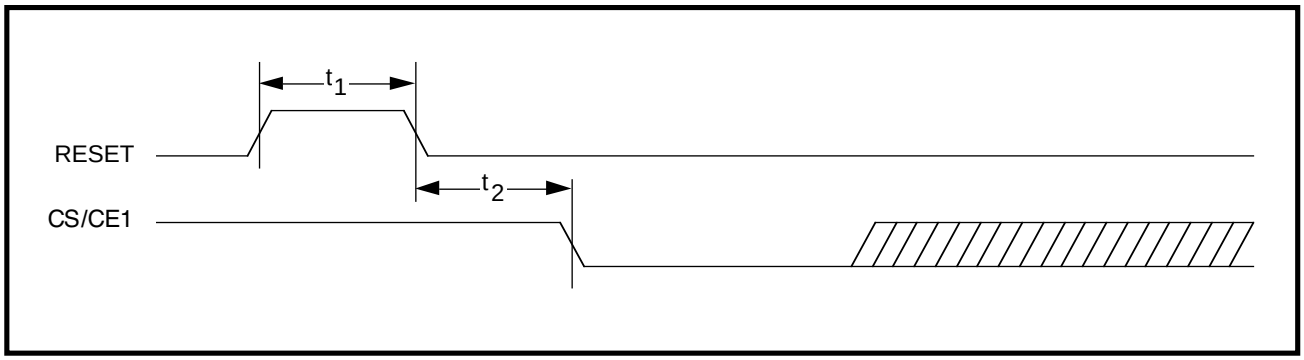


FIGURE 12: RESET Timing

TABLE 10: RESET Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RESET pulse width t_1		500			ns
RESET low to first $\overline{CS}/\overline{CE1}$ low t_2		800			ns

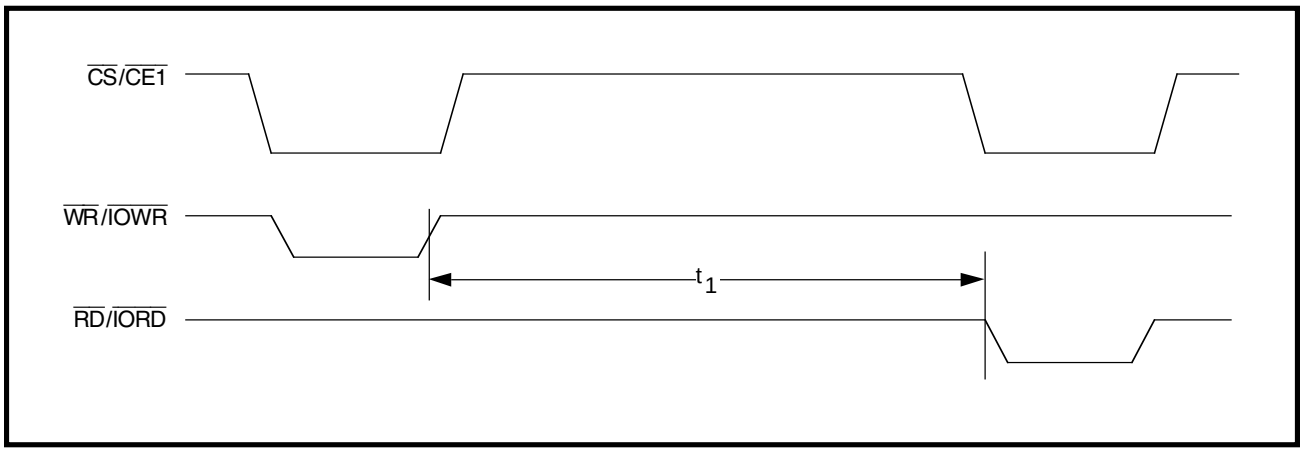


FIGURE 13: Skip Packet Timing

TABLE 11: Skip Packet Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Writing Skip Packet high to next Buffer Memory Port read t_1		200			ns

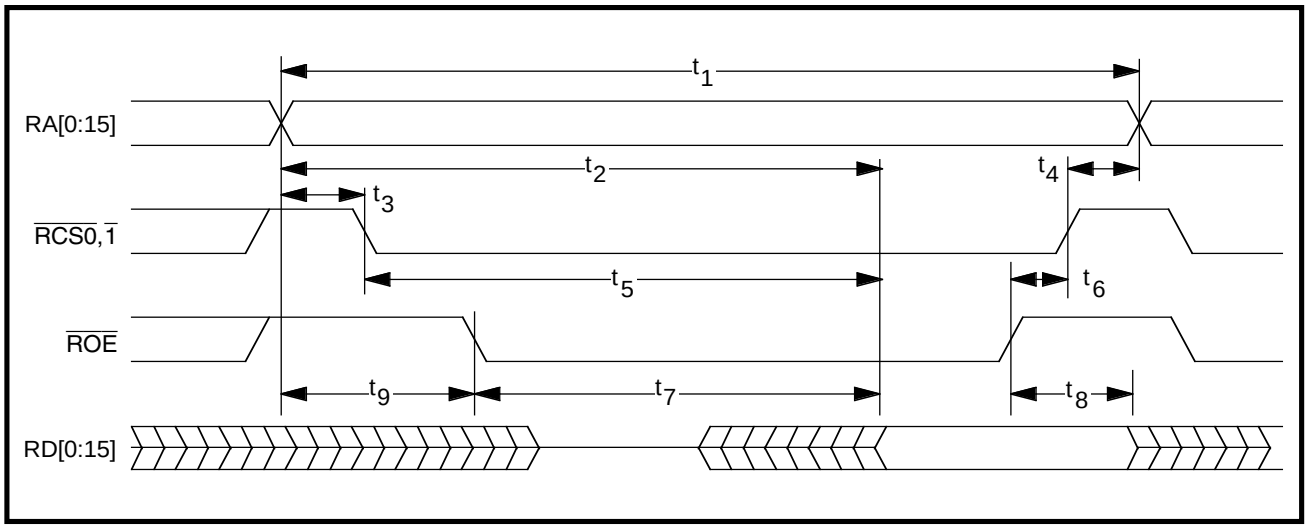


FIGURE 14: SRAM Read Timing

TABLE 12: SRAM Read Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Read cycle	t_1	RAMSP = 1	95			ns
		RAMSP = 0	145			ns
Address access time	t_2	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
Address valid to $\overline{RCS0,1}$ low	t_3				8	ns
$\overline{RCS0,1}$ high to address invalid	t_4		0			ns
Chip select access time	t_5	RAMSP = 1			75	ns
		RAMSP = 0			125	ns
$\overline{ROE}$ high to $\overline{RCS0,1}$ high	t_6		0		8	ns
Output enable access time	t_7	RAMSP = 1			50	ns
		RAMSP = 0			100	ns
Data hold time	t_8		0			ns
Address valid to $\overline{ROE}$ low	t_9				30	ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

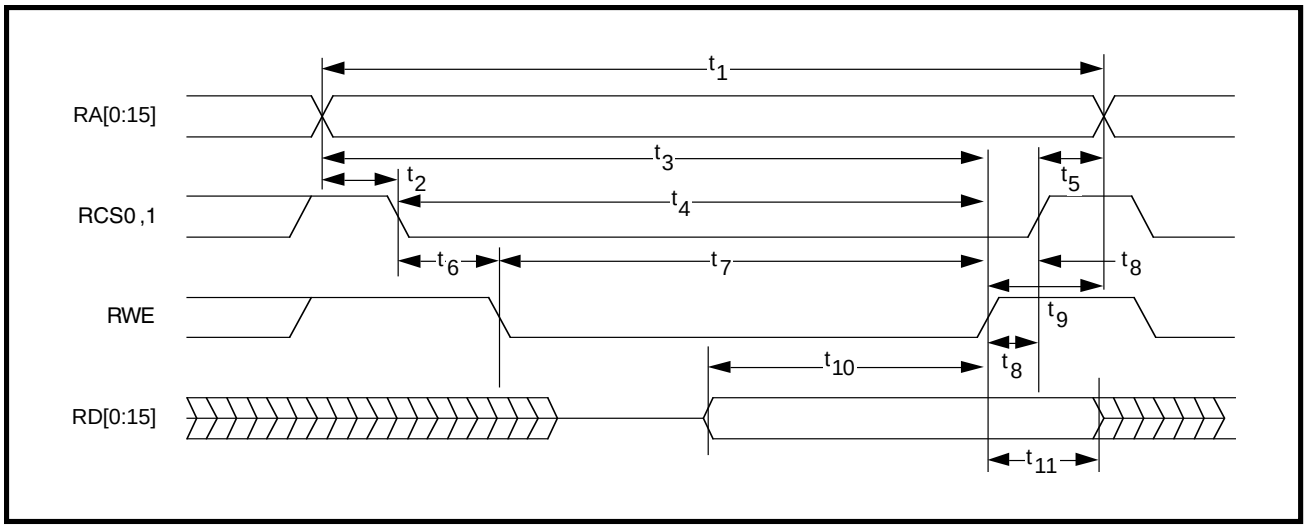


FIGURE 15: SRAM Write Timing

TABLE 13: SRAM Write Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Write Cycle	t_1	RAMSP = 1	95			ns
		RAMSP= 0	145			ns
Address Valid to $\overline{RCS0,1}$ low	t_2				8	ns
Address Valid to $\overline{RWE}$ high	t_3	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ high	t_4	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RCS0,1}$ high to Address Invalid	t_5		0			ns
$\overline{RCS0,1}$ low to $\overline{RWE}$ low	t_6		0			ns
$\overline{RWE}$ Pulse Width	t_7	RAMSP = 1	70			ns
		RAMSP = 0	120			ns
$\overline{RWE}$ high to $\overline{RCS0,1}$ high	t_8		0			ns
$\overline{RWE}$ high to Address Invalid	t_9		10			ns
Data Setup Time	t_{10}	RAMSP = 1	40			ns
		RAMSP = 0	90			ns
Data Hold Time	t_{11}		20			ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

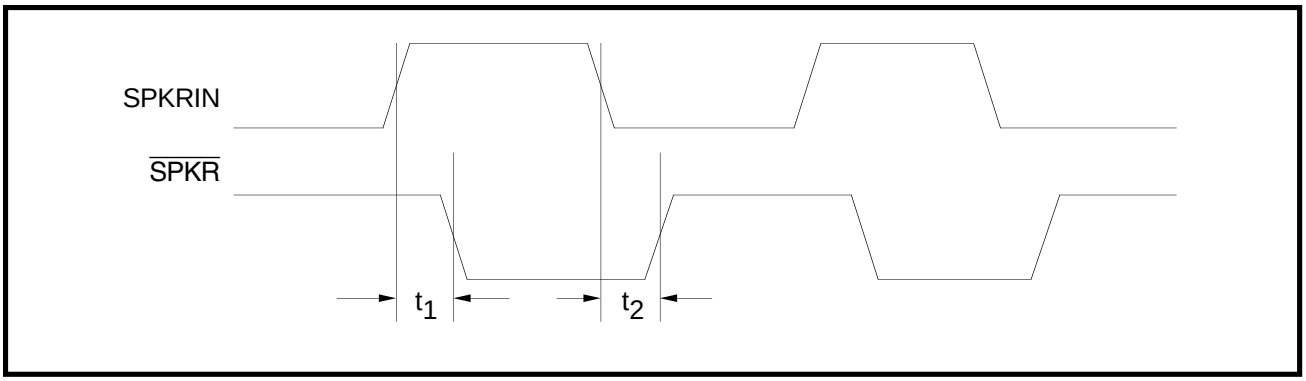


FIGURE 16: Speaker Timing

TABLE 14: Speaker Timing (Refer to Figure 16)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{SPKR}$	Vdd = 5V			25	ns
high to low propagation delay t_1	Vdd = 3.3V			30	ns
$\overline{SPKR}$	Vdd = 5V			25	ns
low to high propagation delay t_2	Vdd = 3.3V			30	ns

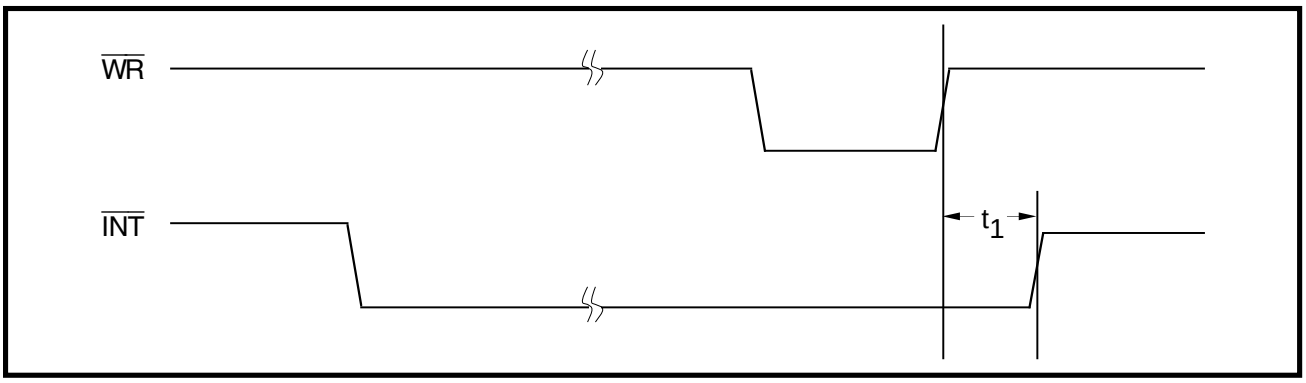


FIGURE 17: Interrupt Timing (Generic Bus Mode)

TABLE 15: Interrupt Timing (Generic Bus Mode)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{INT}$ t_1	Vdd = 5V	7		40	ns
signal cleaning delay	Vdd = 3.3V			50	ns

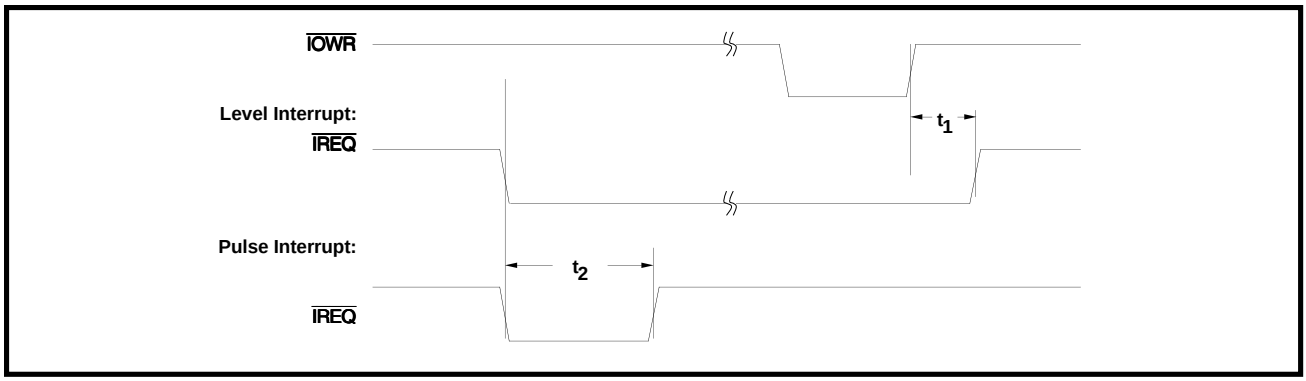


FIGURE 18: Interrupt Timing (PCMCIA Mode)

TABLE 16: Interrupt Timing (PCMCIA Mode)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
$\overline{IREQ}$		level interrupt	Vdd = 5V	7		40	ns
signal clearing delay	t_1		Vdd = 3.3V			50	ns
$\overline{IREQ}$ low pulse width	t_2	pulse interrupt		750		800	ns

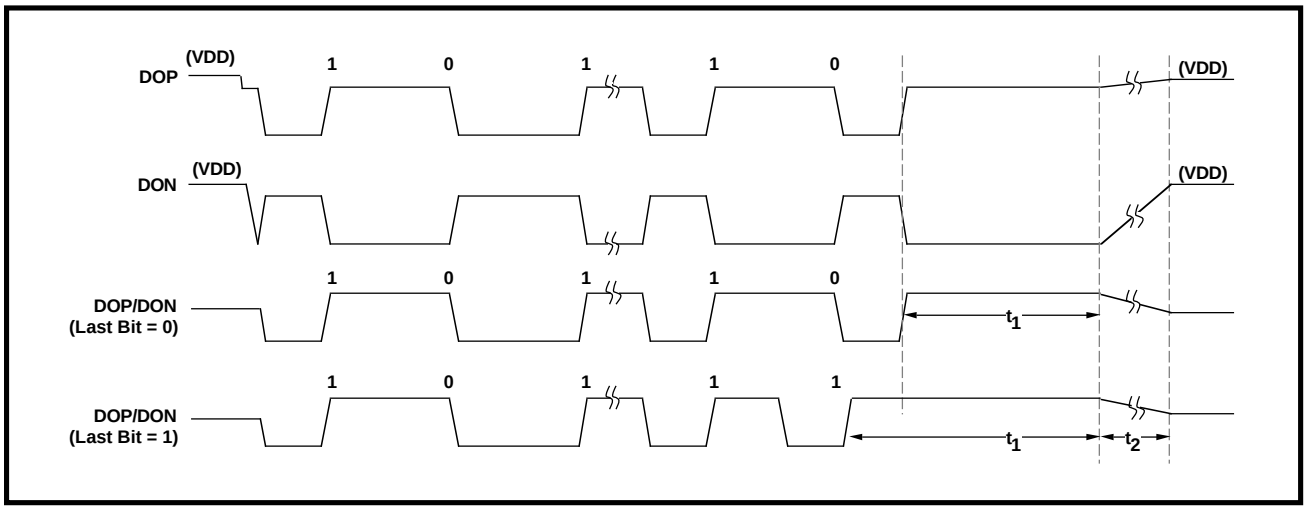


FIGURE 19: Transmit Timing (AUI)

TABLE 17: Transmit Timing (AUI)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
DOP/DON end-of-packet delimiter	t_1		200			ns
DOP/DON line voltage transition	t_2				8	µs

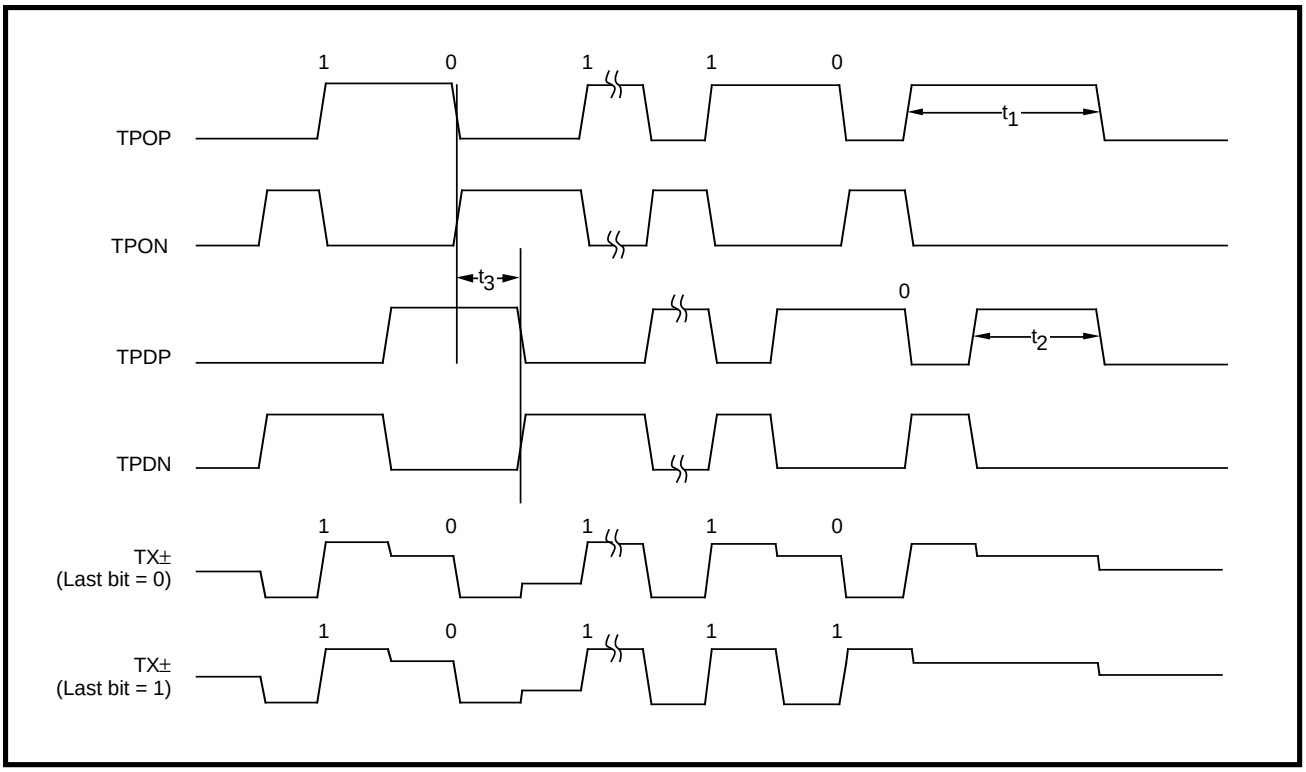


FIGURE 20: Transmit Timing (TP)

TABLE 18: Transmit Timing (TP)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPOP/TPON end-of-packet delimiter t_1		250			ns
TPDP/TPDN end-of-packet delimiter t_2		200			ns
TPOP to TPDP and TPON to TPDN delay t_3			50		ns

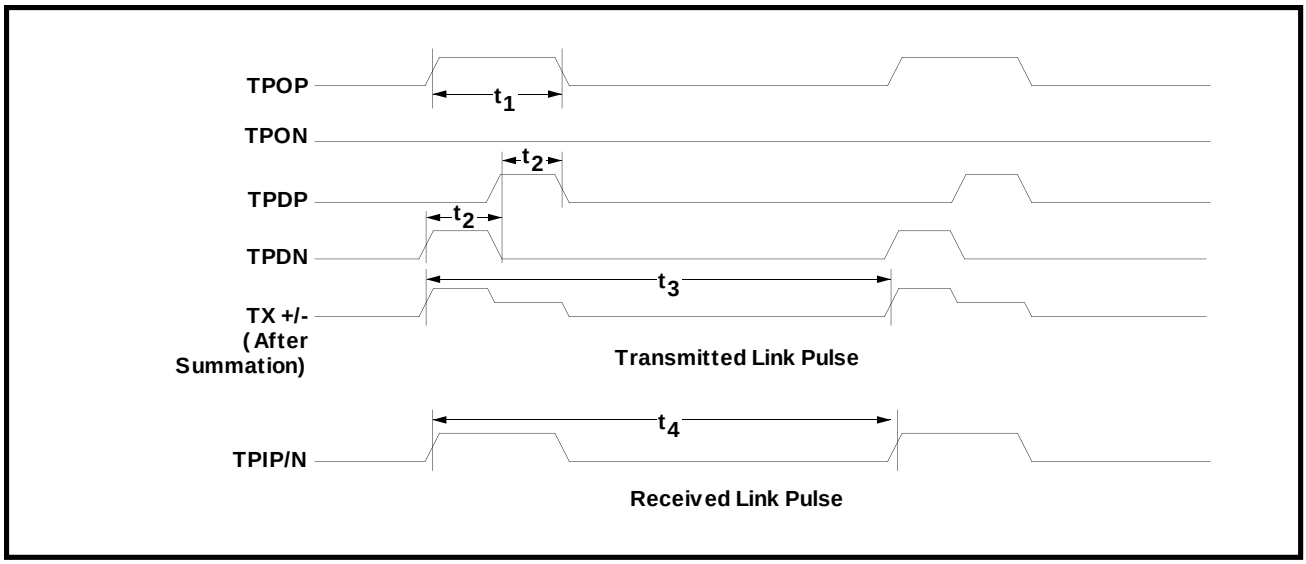


FIGURE 21: Link Test Timing

TABLE 19: Link Test Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TPOP link pulse width	t_1			150		ns
TPDP/TPDN link pulse width	t_2			100		ns
Duration between transmitted link pulses	t_3		9		11	ms
Duration between received link pulses	t_4		4.1		65	ms

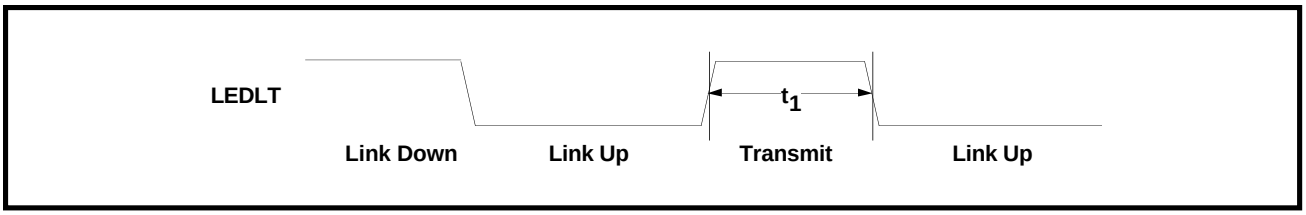


FIGURE 22: LED Timing (TP)

TABLE 20: LED Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Transmit blink-off timing	t_1	TP selected		100		ms

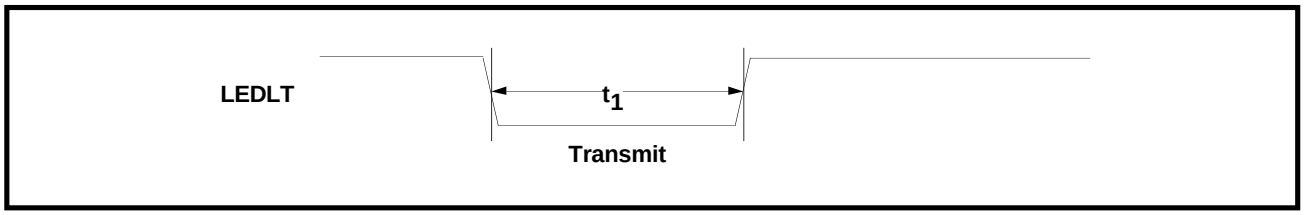


FIGURE 23: LED Timing (AUI)

TABLE 21: LED Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Transmit blink-on timing	t_1	AUI selected		100		ms

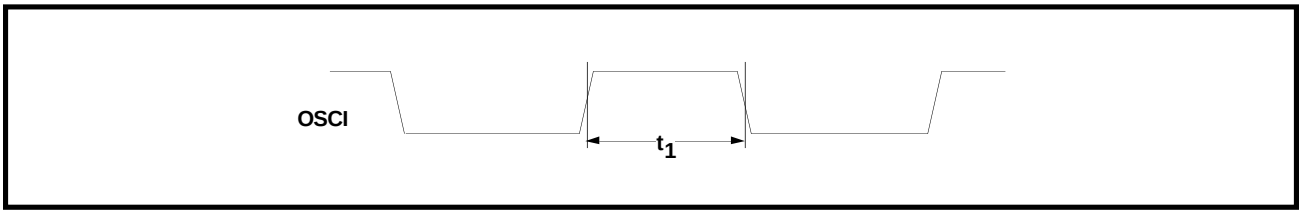


FIGURE 24: Oscillator Duty Cycle

TABLE 22: OSCI Duty Cycle

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Oscillator duty cycle	t_1		40	50	60	%

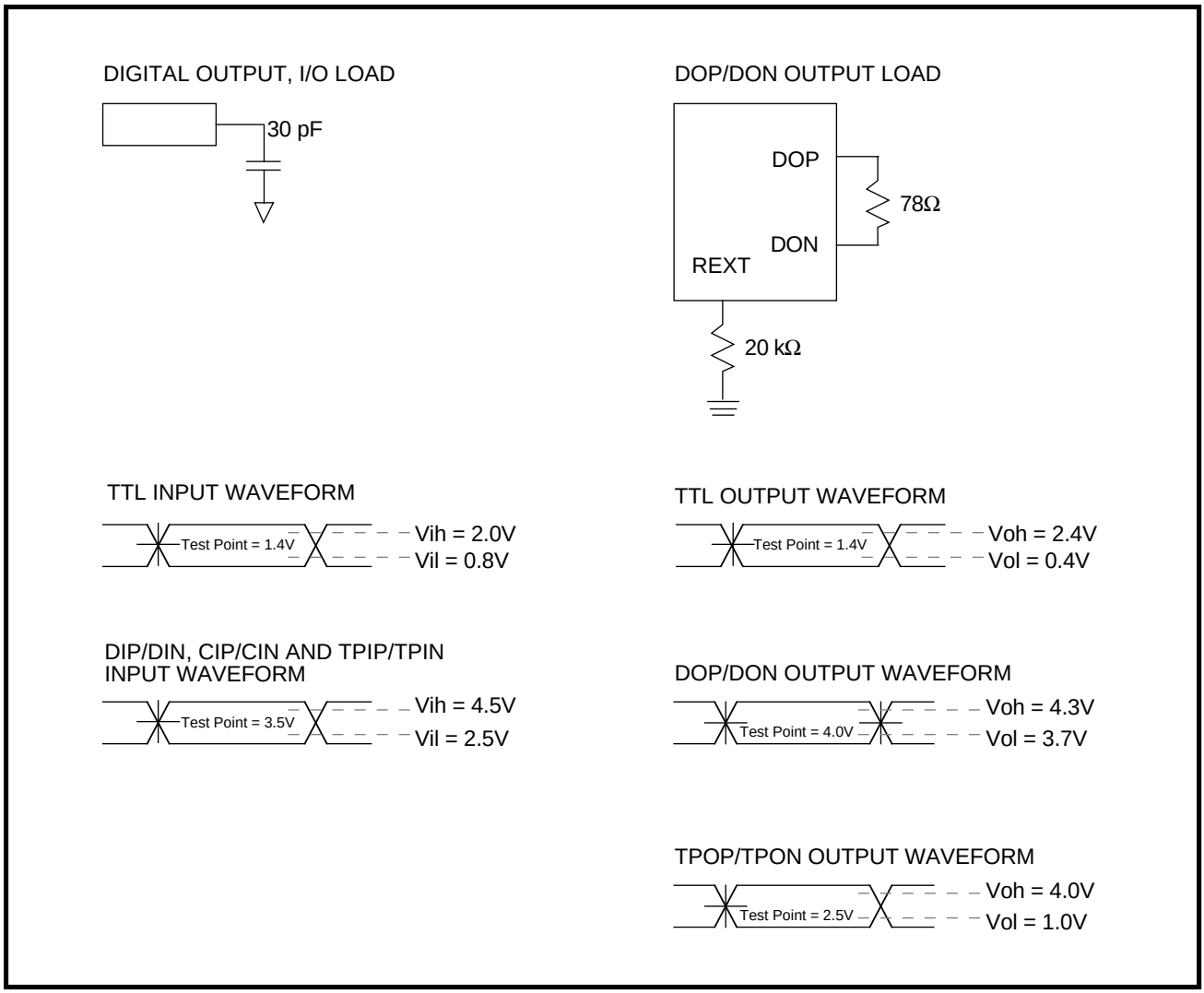
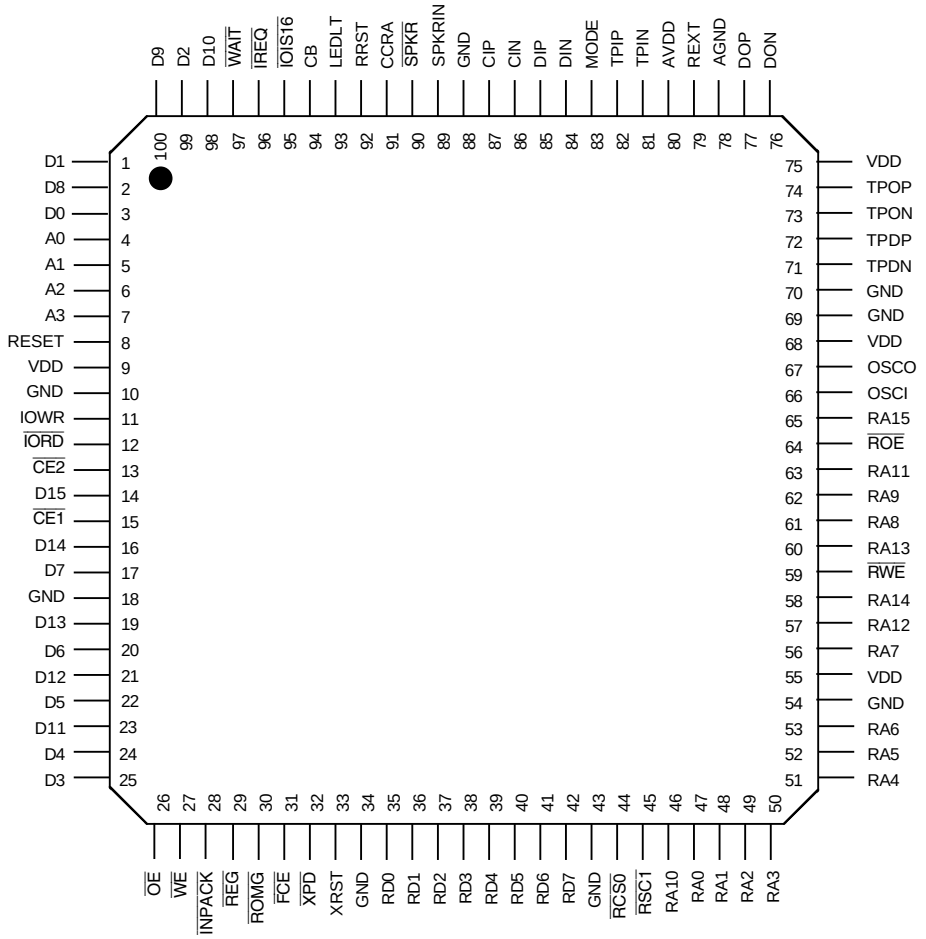


FIGURE 25: Test Conditions

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

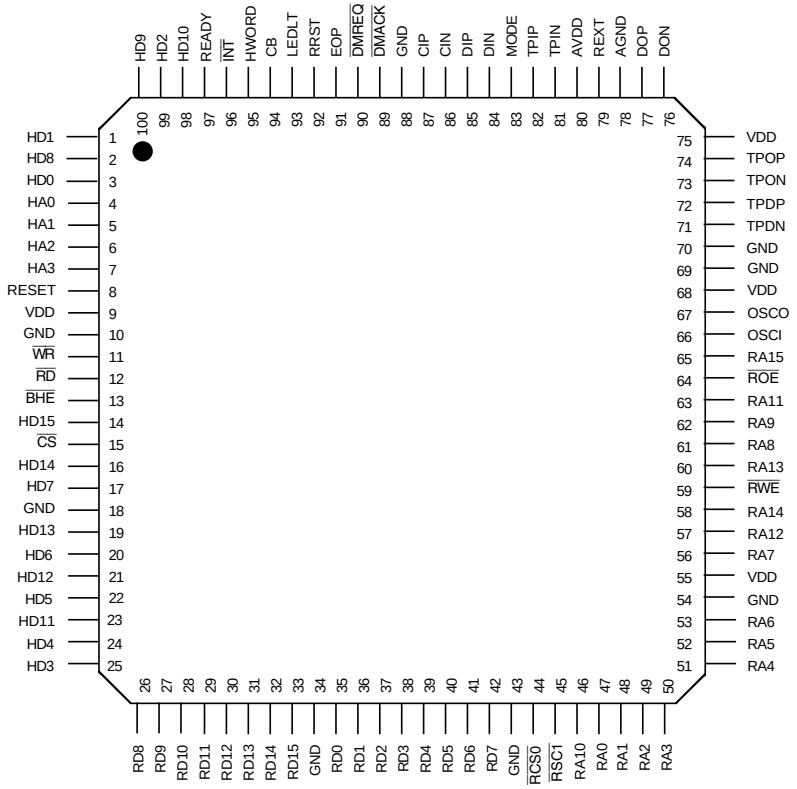


TSC 78Q8373
100-Lead TQFP
PCMCIA Bus Mode

TSC 78Q8373
3V, 5V PCMCIA
Ethernet Combo

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



TSC 78Q8373

100-Lead TQFP
Generic Bus Mode

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
TSC 78Q8373 - PCMCIA Ethernet Combo 100-lead TQFP	78Q8373-CGT	78Q8373-CGT

TDK Semiconductor Corporation, 14351 Myford Road, Tustin, CA 92780-7068 (714) 508-8800, FAX (714) 508-8877

