# W9980 Digital Voice Recorder

## General Applications:

W9980 was specially designed for long duration digital recoding appliance using NVM as the storage device. The typical applications are included voice recorder, language learning tool, voice notebook, and high quality voice toy.

## 1 GENERAL DESCRIPTION

The W9980D is DSP base Digital Voice Recorder chip. This chip compress and decompress sampled voice data by the algorithm G.723.1 and get high quality voice data for play or for voice to text translate. The W9990D integrate interfaces for DVR application and minimize PC board area. This chip build in good power management and suitable for portable machine design.

The voice sampling rate for ITU-G.723.1 can be 8K or 11K and support 5.3K/6.3K bit rate for 8K sampling rate or 7.3/8.7K data rate for 11K sampling rate. The compression rate is 24 or 20 for the two bit rate. The ITU-G.723 get high quality voice compress data and suitable for voice recognition after decompress. The W9980D build in UART and Parallel port interface to PC host, the compressed data can upload to PC for voice mail or for voice to text translation by IBM Via-Voice software.

The W9980D integrate Synchronous Serial Port to interface external CODEC for voice sample and play, LCD interface, PIO interface for user interface and memory interface for voice data recorded. The memory controller can interface to SmartMedia, CompactFlash, IDE, or Intel/AMD type flash memory. In addition to receive bit stream from external CODEC, this chip can receive bit stream from the 8032/8051 mode 0 serial port by the synchronous serial port interface to these external micro controller.

The W9980D is a 3.3V device with TTL compatibility 3.3V only I/O, and is packaged in a 128L LQFP.

## 2 FEATURES

### ❑ DSP CORE

- 30 MIPS 24-bits instruction, 16-bits integer data DSP core
- Internal one Instruction and two data access at one cycle
- Build-in two bank instruction ROM. 13Kx24 and 4Kx24
- Build-in 8Kx16 ROM and 4Kx16 SRAM for 1st data access
- Build-in 2Kx16 ROM and 1Kx16 SRAM for 2nd data access
- External data memory extension with 2K base up to 16M words
- Three interrupts support (IRQ0_, IRQ1_ and IRQ2_)
- Low power consumption - 50mA during operation
- Power down mode support - 30uA during power down

### ❑ CODEC Interface

- Synchronous serial port connecting external CODEC device for voice input and sound play

### ❑ Memory Interface

- Support SmartMedia and CompactFlash interface for voice recorded with no size limitation
- Support AMD/Intel type flash memory interface for voice recorded up to 16Mwords on 2K words base.

### ❑ LCD Interface

- Support 1/3 bias (1, 2, 3 Volt) 1/4 duty TN-LCD interface up to 100 LCD dots (4COM * 25 SEGMENT)
- Support serial interface to external LCD driver up to 160 dots

### ❑ GPIO interface

- 12 GPIOs for key-pad and system control

- GPIO input change from low-to-high and high-to-low generate different interrupts to DSP core (IRQ0_ and IRQ1_)

❑ **Host Interface**

- NS16550 compatible UART support for PC data upload/download
- IEEE 1284 parallel port byte mode support for PC data upload/download

❑ **uP 8051/8032 serial mode Interface**

- Support 8051/8032 synchronous serial bitstream for data decode

❑ **Operation Frequency is 30MHz**

❑ **3.3V Device with TTL-compatible 3.3V I/O**

❑ **128L LQFP Package**

❑ **Compression algorithm**

- Provide ITU-G.723.1 (5.3K/6.3K bit rate) voice coding/decoding
- Programmable voice sampling rate. 8K for normal mode recording and 11K for precise mode recording
- Provide Silence-Detection and Comfort-Noise-Generation to lengthen the recording time

❑ **User Interface**

- Categorize Messages : Provide 4 folders to store different kinds of message and up to 99 records for each folder
- Tape-Recorder/CD Type Operation : Provide keys ″record″ , ″play″, ″stop″, ″pause″, ″forward″, ″backward″, ″erase″, and ″erase all″ operation
- Voice Editing Append : Each record can be appended by new message
- Voice Editing Delete : Each record message can be deleted
- Fast Scan : Play first 5 second of each record for message search
- Date and Time Stamp : Every record is indexed by ″data″, ″time″ and ″time-spend″ stamp
- Reserved Recording Time : The UI display the ″reserved recording time″ to indicate available time for recording

- Alarm Clock : Provide 4 time zones up to 80 sets of alarm clock (20 sets/zone)
- Voice Alarm : Alarm by voice message or beeps
- Up/Download : Voice message upload/download to PC
- Low Power Detection : Warning message if battery low.
- Automatic Power-Down : System power-down if 5 minutes no operation

## 3 PIN CONFIGURATION

The W9980D is packaged in a 128L LQFP. The pin configuration is shown in Figure 3.1

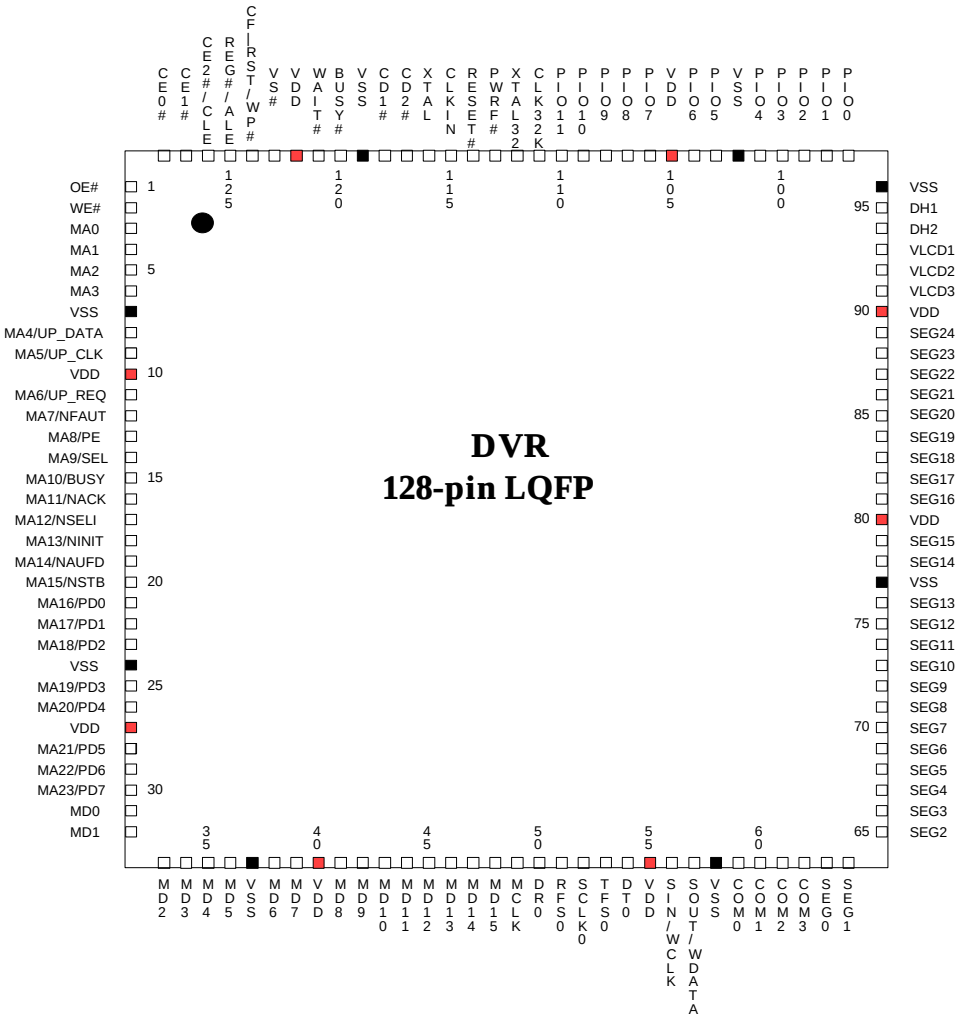


**Figure 3.1 W9980D Pin configuration**

## 4 PIN DESCRIPTION

The following signal types are used in these description.

I Input pin

IU Input pin with internal pull-up resistor

B BI-direction input/output pin

O Output pin

AIO Analog input/output pin

P Power supply pin

G Ground pin

### 4.1 Pin Definition

**LCD Interface**

| Pin Name | Pin Number | Type | Description |
|---|---|---|---|
| COM0-COM3 | 59-62 | O | LCD panel common pins. (1/3 bias, 1/4 duty) |
| SEG0-SEG24 | 63-76, 78-79, 81-89 | O | LCD panel segment pins. (1/3 bias, 1/4 duty) |
| VLCD3 | 91 | P | LCD voltage pin must connect to 3~3.3 V |
| VLCD2 | 92 | I | For LCD voltage level shift during display (2V) |
| VLCD1 | 93 | I | For LCD voltage level shift during display (1V) |
| DH2,DH1 | 94,95 | I | Connect a capacitor to both pins, used for the LCD double voltage capacitor. |
| SIN / WCLK | 56 | I<br><br>O | This pin play the UART SIN signal if external LCD driver function OFF<br><br>Is the external LCD driver clock pin if external LCD driver function ON |
| SOUT / WDATA | 57 | O | This pin play the UART SOUT signal if external LCD driver function OFF |

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|---|---|---|---|
| | | | It is the external LCD driver serial data pin if external LCD driver function ON |

**GPIO Interface**

| Pin Name | Pin Number | Type | Description |
|---|---|---|---|
| PIO0 | 97 | B | GPIO pin used as MODE key by UI |
| PIO1 | 98 | B | GPIO pin used as ERASE key by UI |
| PIO2 | 99 | B | GPIO pin used as SET key by UI |
| PIO3 | 100 | B | GPIO pin used as STOP key by UI |
| PIO4 | 101 | B | GPIO pin used as REC key by UI |
| PIO5 | 103 | B | GPIO pin used as PLAY key by UI |
| PIO6 | 104 | B | GPIO pin used as REW key by UI |
| PIO7 | 106 | B | GPIO pin used as FF key by UI |
| PIO[8:11] | 107-110 | B | GPIO pins |

**CODEC Interface**

| Pin Name | Pin Number | Type | Description |
|---|---|---|---|
| MCLK | 49 | O | Master clock output to external CODEC |
| DR | 50 | I | Serial data received from CODEC |
| RFS | 51 | B | Receiver frame sync of CODEC serial port |
| SCLK | 52 | B | Serial clock of CODEC serial port |
| TFS | 53 | B | Transmitter frame sync of CODEC serial port |
| DT | 54 | O | Serial data transmitted to CODEC |

**Memory Interface**

| Pin Name | Pin Number | Type | Description |
|---|---|---|---|
| CD2# | 118 | IU | Card Detected 2 from CompactCard |
| CD1# | 118 | B | Card Detected 1 from Compact Card.<br><br>In test mode 0 this pin is external Instruction ROM CS_ and in test mode 1 used as internal Instruction ROM0 CS_ |
| BUSY# | 120 | IU | External Flash RDY/BUSY_ signal. In test mode 1 this pin used as internal SRAM2 CS_ |
| WAIT# | 121 | IU | Wait state insert signal used to lengthen the external data memory bus cycle |
| VS# | 123 | I | ″Voltage sense 1″ from CompactFlash Card. This signal should be grounded by CFC to indicate initially 3.3V operation |
| CF_RST /<br><br>WP# | 124 | B | CompactFlash Card reset or SmartMedia Write-Protect signal. This signal is direct drive by the register CF_RST or WP# on 0x3e03.<br><br>In test mode 0 is used as external 2nd data memory CS_. In test mode 1 is used as internal 2nd data ROM CS_ |
| REG# /<br><br>ALE | 125 | O | CompactFlash REG# signal, this signal direct inverse drive by register REG_EN on 0x3e03<br><br>SmartMedia Flash ALE , indicate address cycle |
| CE2# /<br><br>CLE | 126 | O | CE2# is one of external memory CS_ signal. It active if external memory access and register CE2_EN on 0x3e03 is enable<br><br>SmartMedia Flash CLE, indicate command cycle. |
| CE1# | 127 | O | CE1# is one of external memory CS_ signal. It active if external memory access and register CE1_EN on 0x3e03 is enable |
| CE0# | 128 | B | CE0# is one of external memory CS# signal. It active if external memory access and register CE0_EN on 0x3e03 is enable<br><br>In test mode 0 is used as external 1st data memory CS_. In test mode 1 is used as internal 1st data RAM CS# |
| OE# | 1 | B | External memory OE# signal |

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|---|---|---|---|
| | | | In test mode 1 is used to read internal memory |
| WE# | 2 | B | External memory WE# signal<br><br>In test mode 1 is used to write internal memory |
| MA0-MA3 | 3,4,5,6 | B | External memory address 0-3<br><br>In test mode 1 is internal memory address 0-3 |
| MA4 /<br>UP_DATA | 8 | B | External memory address 4 if register UPIC_EN on register 0x3e21 disable<br><br>In test mode 1 is internal memory address 4<br><br>This pin get external synchronous serial data if UPIC_EN enable (8051/8032 serial mode 0) |
| MA5 /<br><br>UP_CLK | 9 | B | External memory address 5 if register UPIC_EN on register 0x3e21 disable<br><br>In test mode 1 is internal memory address 5<br><br>This pin is external synchronous serial clock in if UPIC_EN enable (8051/8032 serial mode 0) |
| MA6 /<br><br>UP_REQ | 11 | | External memory address 6 if register UPIC_EN on register 0x3e21 disable<br><br>In test mode 1 is internal memory address 6<br><br>This pin is external synchronous serial clock in if UPIC_EN enable (8051/8032 serial mode 0)port data in if UPIC_EN enable (8051/8032 serial mode 0) |
| MA7 /<br>NFAUT | 12 | B | External memory address 7 if register PPIC_EN on register 0x3e03 disable<br><br>In test mode 1 is internal memory address 7<br><br>This pin drive the signal nFault on parallel port if PPIC_EN enable (Parallel Port Interface enable) |
| MA8 /<br><br>PE | 13 | B | External memory address 8 if register PPIC_EN on register 0x3e03 disable<br><br>In test mode 1 is internal memory address 8 |

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|---|---|---|---|
| | | | This pin drive the signal PError on parallel port |
| MA9 / SEL | 14 | B | External memory address 9 if register PPIC_EN on register 0x3e03 disable<br>In test mode 1 is internal memory address 9<br>This pin drive the signal Select on parallel port |
| MA10 / BUSY | 15 | B | External memory address 10 if register PPIC_EN on register 0x3e03 disable<br>In test mode 1 is internal memory address 10<br>This pin drive the signal Busy on parallel port |
| MA11 / NACK | 16 | B | External memory address 11 if register PPIC_EN on register 0x3e03 disable<br>In test mode 1 is internal memory address 11<br>This pin drive the signal nAck on parallel port |
| MA12 / NSELI | 17 | B | External memory address 12<br>In test mode 1 is internal memory address 12<br>This pin connect the signal nSelectIn if parallel port is used |
| MA13 / NINIT | 18 | B | External memory address 13<br>In test mode 1 is internal memory address 13<br>This pin connect the signal nInit if parallel port is used |
| MA14 / NAUFD | 19 | B | External memory address 14<br>This pin connect the signal nAutoFd if parallel port is used |
| MA15 / NSTB | 20 | B | External memory address 15<br>This pin connect the signal nStrobe if parallel port is used |
| MA16-23 / PD0-7 | 21,22,23,25,26,28 ,29,30 | B | External memory address 16-23<br>In test mode 0 is external Instruction bits 16-23 |

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|---|---|---|---|
| | | | In test mode 1 output internal instruction ROM code 16-23<br><br>These pin is parallel port data pins 0-7 if register PPIC_EN is enable |
| MD0-MD7 | 31,32,33,34,35,36 ,38,39 | B | External memory DATA 0-7, SmartMedia IO0-7<br><br>In test mode 1 these pins output internal memories data bits 0-7 |
| MD8-15 | 41-49 | B | External memory DATA 8-15<br><br>In test mode 1 these pins output internal memories data bits 8-15 |

**Miscellaneous**

| Pin Name | Pin Number | Type | Description |
|---|---|---|---|
| CLK32K,<br><br>XTAL32 | 111,112 | I<br><br>O | Crystal pair for 32,768Hz |
| PWRF# | 113 | IU | Power-fail/battery-low detected pin to generate interrupt IRQ2_<br><br>In test mode 1 is internal instruction ROM1 CS_ |
| RESET# | 114 | I | Chip reset signal, it also setting the test mode by MD[2:0] and LCD mode by MD[4:3] |
| CLKIN,<br><br>XTAL | 115,116 | I<br><br>O | Crystal pair for DSP operation |

**Power and Ground**

| Pin Name | Pin Number | Type | Description |
|---|---|---|---|
| VDD | 10,27,40,55,<br><br>80,90,105,<br><br>122 | P | Power supply +3.3V $\pm$ 0.3V |

| | | | |
|---|---|---|---|
| VSS | 7,24,37,58,77,96, 102,119 | G | Ground |

**4.1 Power-on Reset Initialization**

During power-on reset, state of the memory data line MD[4:0] are latch into the W9980D`s internal configuration registers as device configuration information. For pull-up or pull-down a 4.7K ohm resistor is connect to VDD or VSS.

The configuration is used for LCD mode and for chip test/diagnostic. In normally function all these five pin should pull-up.

**Power-on Reset configuration**

| MD Bit | Value | Description |
|---|---|---|
| MD4 | 0 | The LCD driver inverse the LCD segment display on/off |
| | 1 | The LCD driver display segment on/off normally |
| MD3 | 0 | External serial LCD driver enable. In this mode pin56,57 are LCD function and disable UART function |
| | 1 | External LCD disable and pin 56,57 are UART function |
| MD2-0 | 000 | Test mode 0. All internal ROM/RAM are disable, DSP access Instruction/data from external memory |
| | 001 | Test mode 1. This mode is used to test internal memory all internal memory can be access by external pin |
| | 010 | Test mode 2. Internal long counter test. split these counter into several part and GPIO0-7 show the result |
| | 011 | Test mode 3. In this mode the instruction always from external |
| | 100 | Test mode 4. Stack test. To test the stacks on PSQ. These stacks can be directly access by memory pin |
| | 111 | Normal mode |

## 5 SYSTEM DIAGRAM

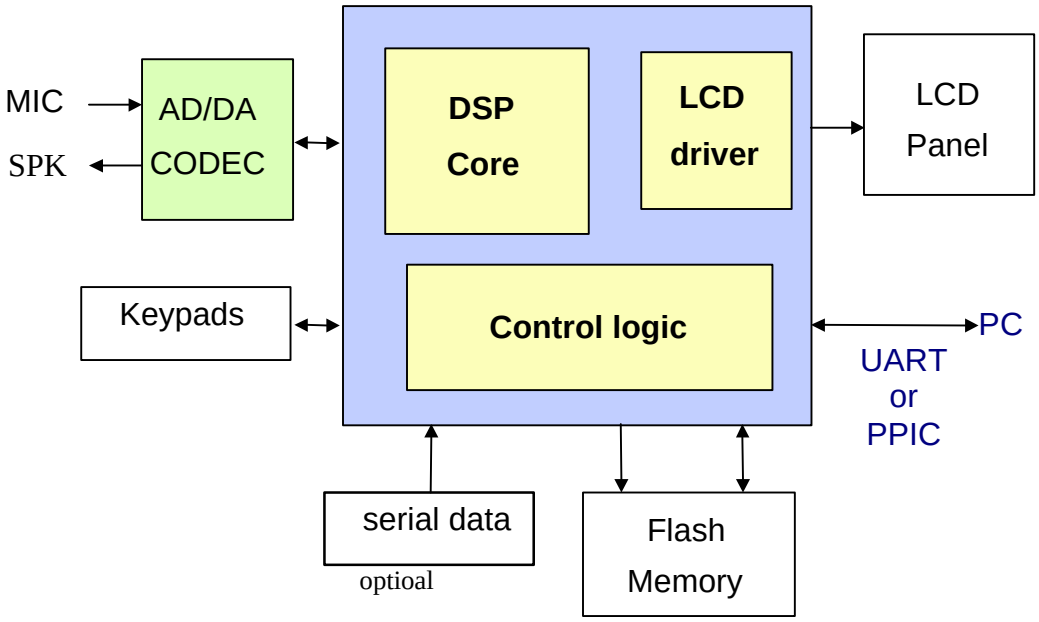


**Figure 5.1 W9980D-Based Digital Voice Recorder System Diagram**