



W921E400A/W921C400

4-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

The W921E400A/W921C400 is a single-chip CMOS 4-bit microcontroller that is a subset of W921E880A/W921C880. It features a 4-bit ALU, three multi-function timers, one channel DTMF generator, a beep tone generator, a serial I/O port and built in four by one channel comparator circuit, thus it can be easily implemented as telephone processor. Using the serial transmit/receive function, the W921E400A/W921C400 series can interface with Winbond LCD driver IC by the serial control circuit. There are also seven interrupt sources and 48-level subroutine nesting for interrupt applications.

The W921E400A/W921C400 have two power reduction modes, hold mode and stop mode, which help to minimize power dissipation. This product is a powerful microcontroller for telephone processor, remote controllers, multiple I/O products, keyboard controllers, speech synthesis LSI controllers, and other products with few components.

2. FEATURES

Operating Voltage

- 2.8 to 5.5V operating voltage for W921E400A EPROM TYPE
- 2.4 to 5.5V operating voltage for W921C400 MASK ROM TYPE

Operating Frequency

- Crystal or RC for main system clock:
 - Crystal for 400K, 800K, 2M, 3.58M, 4 MHz
 - RC up to 4 MHz

Memory

- 4K × 10-bit ROM (super EPROM):
- 512 × 4-bit RAM:
 - 64 × 4-bit special register
 - 16 × 4-bit working register
 - 128 × 4-bit general register
 - 304 × 4-bit multi-purpose register

Stack

- 8-bit stack pointer

I/O Pins

- 13 bidirectional and individually controllable I/O lines:
 - P2 Port: P2.0 to P2.1 large sink current pins and open drain option
 - P3 Port: P3.0 to P3.3 multi-function I/O
 - P4 Port: P4.2 to P4.3 open drain and pull high resistor option, multi-function I/O
 - P5 Port: P5.1 multi-function I/O
 - P6 Port: P6.0 to P6.3 open drain and pull high resistor option, multi-function I/O
- 8 bidirectional I/O lines:
 - PA Port: PA.0 to PA.3 open drain and pull high resistor option
 - PB Port: PB.0 to PB.3 open drain and pull high resistor option

Serial I/O Interface

- Clock synchronous multi-nibbles serial transmitter/receiver interface

DTMF Generator

- One channel DTMF generator

Beep Tone Generator

- 4 frequencies (2K, 1K, 630, 520 Hz) software selectable beep tone generator

Voltage Comparator

- Multiplexed four channel voltage comparator

Timer/Counter

- Timer 0: 2 to 19 order divider, auto-reload timer, watch-dog timer
- Timer 2: 2 to 19 order divider, auto-reload timer, arbitrary waveform generator, period/pulse width measurement function
- Timer 3: 2 to 19 order divider, auto-reload timer

Interrupt

- Two external sources: INT0 (P4.3), P4 Port (P4.2)
- Five internal sources: Timer 0, Timer 2, Timer 3, Comparator, Serial Port

Operating Mode (System Clock)

- Normal mode: System clock operating
- HOLD mode: No operation except for oscillator (system clock stops only)
- STOP mode: No operation including oscillator

Addressing Mode

- ROM: Indirect call addressing mode
Long jump/call addressing mode
- RAM: Direct addressing mode
Indirect addressing mode
Working register addressing mode
- Look-up table addressing mode

Instruction Sets

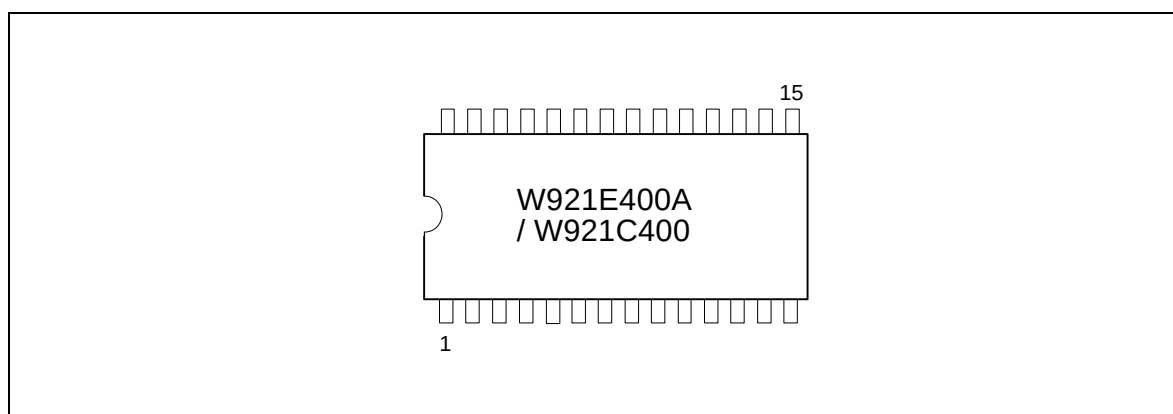
- 117 instruction sets

Package Type

- 28-pin DIP, 28-pin SOP

3. PIN CONFIGURATION

PIN NAME	DIP28 (OR SOP28)	PIN NAME	DIP28 (OR SOP28)
P2.0	1	PA.0	15
P2.1	2	PA.1	16
P3.0/ANI0	3	PA.2	17
P3.1/ANI1	4	PA.3	18
P3.2/ANI2	5	PB.0	19
P3.3/ANI3	6	PB.1	20
P4.2	7	PB.2	21
P4.3/INT0	8	PB.3	22
P5.1/TM2	9	BTG	23
P6.0/WDATA	10	DTMF	24
P6.1/WCLK	11	$\overline{\text{RESET}}$	25
P6.2/RDATA	12	$\overline{\text{OSCO}}$	26
VSS	13	OSCI	27
P6.3/RCLK	14	VDD	28



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4. PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
OSCI	I	Main oscillator input pin with internal capacitor
$\overline{\text{OSCO}}$	O	Main oscillator output pin
P2.0 to P2.1	I/O*	I/O port 2 with large sink current
P3.0/ANI0 to P3.3/ANI3	I/O	I/O port 3 or analog input (ANI0 to ANI3) pins
P4.2	I/O*	I/O pin P4.2 or the input pin of interrupt port
P4.3/INT0	I/O*	I/O pin P4.3 or INT0 input pin
P5.1/TM2	I/O	I/O pin P5.1 or the controlled pin of timer2
P6.0/WDATA	I/O*	I/O pin P6.0 or the data output pin of serial interface
P6.1/WCLK	I/O*	I/O pin P6.1 or the clock I/O pin of WDATA
P6.2/RDATA	I/O*	I/O pin P6.2 or the data input pin of serial interface
P6.3/RCLK	I/O*	I/O pin P6.3 or the clock I/O pin of RDATA
PA.0 to PA.3	I/O*	I/O port A with wake up stop mode function
PB.0 to PB.3	I/O*	I/O port B with wake up stop mode function
DTMF	O	Dual tone multi-frequency output pin
BTG	O	Beep tone generator output pin
$\overline{\text{RESET}}$	I	Reset input pin with low active
VDD	I	Positive power supply input pin
VSS	I	Negative power supply input pin

Notes:

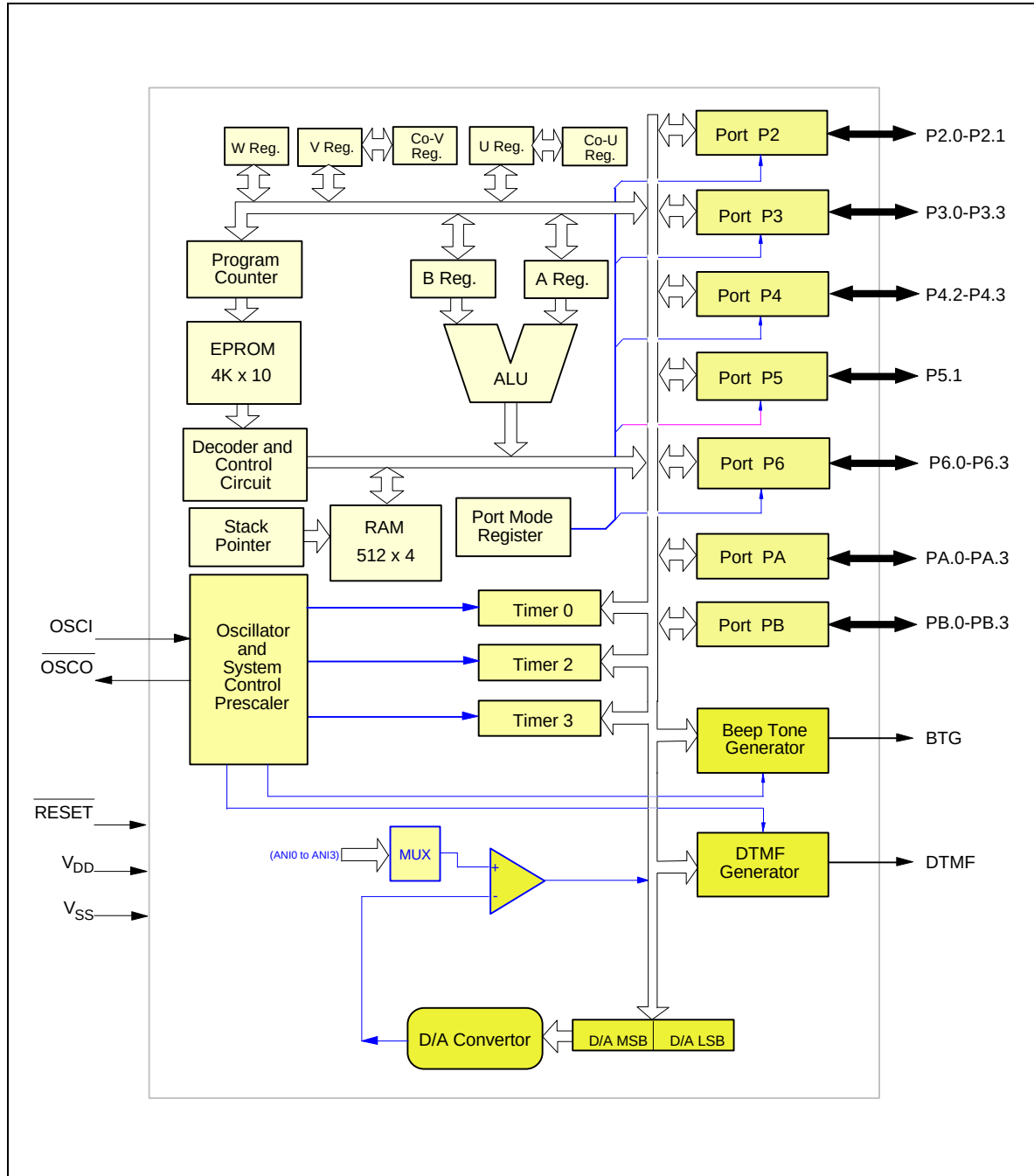
* open drain option by software

☆ open drain and pull high resistor option by software

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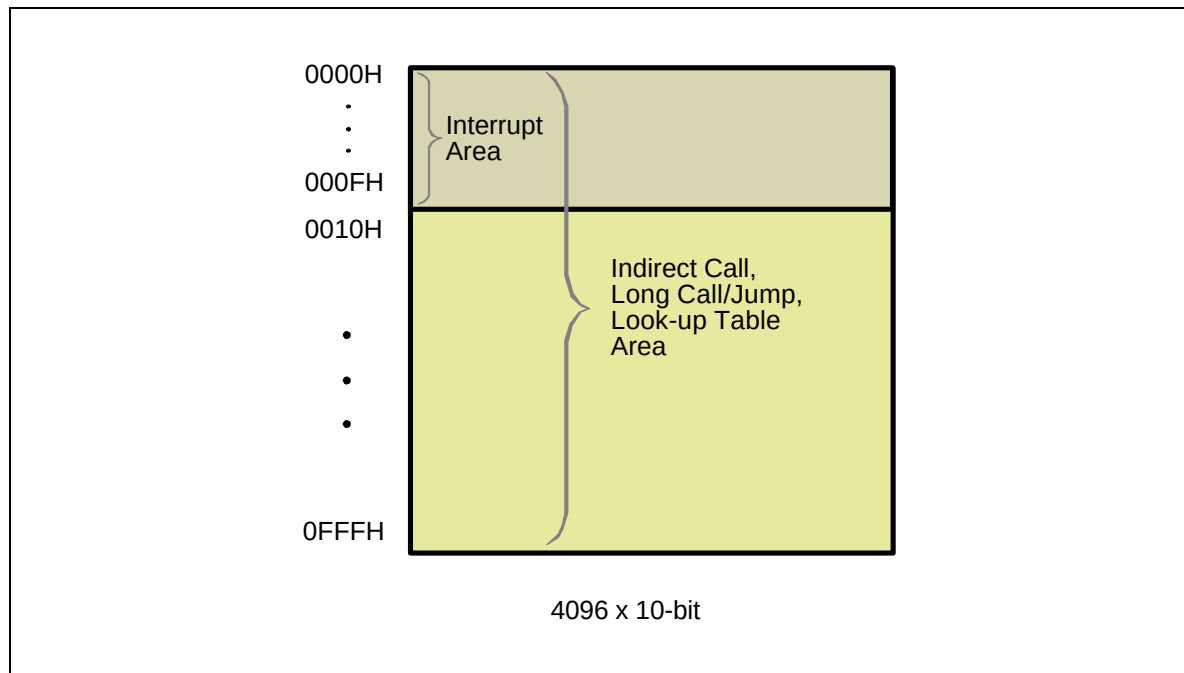


5. BLOCK DIAGRAM



6. FUNCTION DESCRIPTION

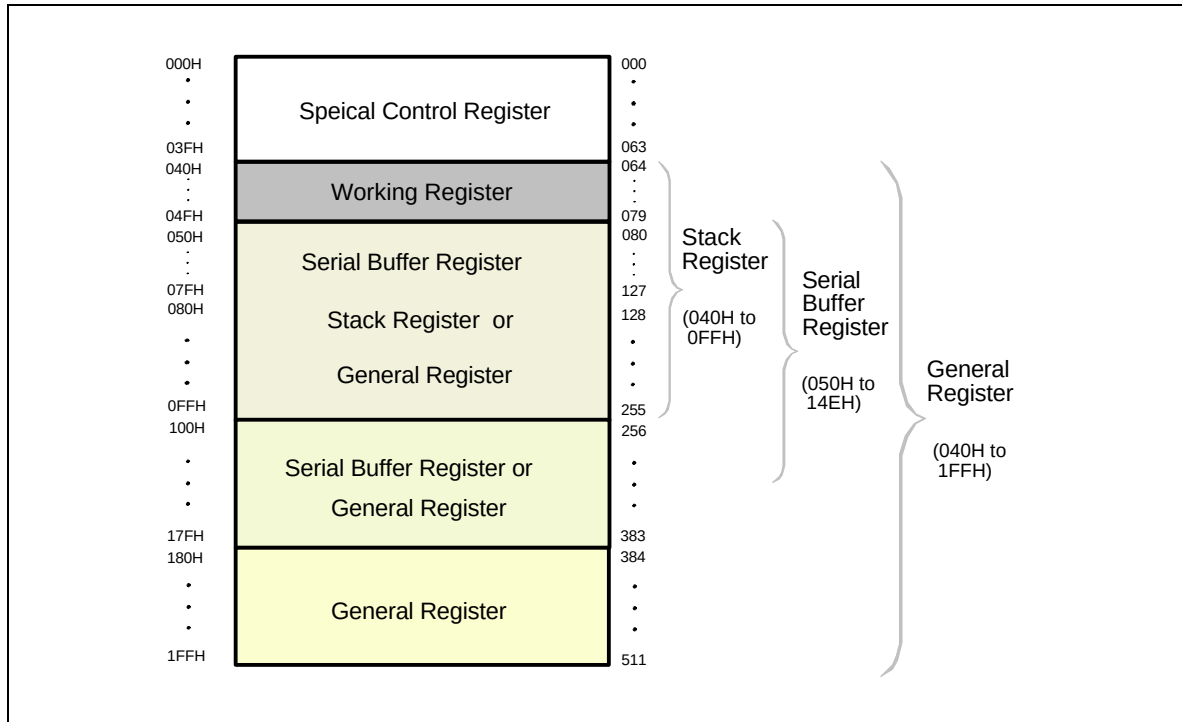
6.1 ROM Memory Map



0000H	JMPL Instruction (Reset)
0001H	XXXXX XXXXX
0002H	JMPL Instruction (INT0)
0003H	XXXXX XXXXX
0004H	JMPL Instruction (TM0)
0005H	XXXXX XXXXX
0006H	RESERVED
0007H	
0008H	JMPL Instruction (TM2)
0009H	XXXXX XXXXX
000AH	JMPL Instruction (Comparator/TM3)
000BH	XXXXX XXXXX
000CH	JMPL Instruction (P4.2)
000DH	XXXXX XXXXX
000EH	JMPL Instruction (Serial Port)
000FH	XXXXX XXXXX

Priority: Reset > INT0 > TM0 > TM2 > (Comparator/TM3) > P4.2 > Serial Port

6.2 RAM Memory Map



6.2.1 Special Control Register Area

There are 64×4 -bit registers in the special control register area. All control registers such as DTMF control register, serial speed control register, ..., etc. are in this area. Refer to the following table for detailed register map.

ADDR.	DESCRIPTION	ABBREVIATION	INITIAL VALUE
000H	Reserved		-
001H	Reserved		-
002H	Reserved		-
003H	Port P4 Pull High Resistor Register	(P4PH)	00H
004H	Port P4 Output Type Register	(P4TP)	00H
005H	Port P6 Pull High Resistor Register	(P6PH)	00H
006H	Port P6 Output Type Register	(P6TP)	00H
007H	Port PAB Pull High Resistor Register	(PABPH)	00H
008H	Port PAB Output Type Register	(PABTP)	00H

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Special Control Register Map, continued

ADDR.	DESCRIPTION	ABBREVIATION	INITIAL VALUE
009H	Serial LSB Nibble Register	(SRLNR)	02H
00AH	Serial MSB Nibble Register	(SRMNR)	00H
00BH	Serial Speed Control Register	(SRSPC)	00H
00CH	Serial Clock Inverter Control Register	(SRINV)	00H
00DH	Port P2 Output Type Register	(P2TP)	00H
00EH	Reserved		-
00FH	Port P3 I/O Status Control Register	(P3IO)	00H
010H	Port P4 I/O Status Control Register	(P4IO)	00H
011H	Port P5 I/O Status Control Register	(P5IO)	00H
012H	Port P6 I/O Status Control Register	(P6IO)	00H
013H	DTMF Oscillation Control Register	(OSCCTR)	00H
014H	DTMF Register	(DTMF)	00H
015H	Row/Column Frequency Control Register	(RCCTL)	00H
016H	D/A Control Register	(DACTL)	00H
017H	D/A Converter LSB Data Register	(DALSB)	00H
018H	D/A Converter MSB Data Register	(DAMSB)	00H
019H	Comparator Analog Input Multiplexer	(ANIMUX)	00H
01AH	Comparator Control Register	(COMPTR)	04H
01BH	Reserved		-
01CH	Reserved		-
01DH	Reserved		-
01EH	TM2 Read Only MSB Data Register	(TM2RM)	0FH
01FH	TM2 Read Only LSB Data Register	(TM2LM)	0FH
020H	TM0 Control Register	(TM0CR)	00H
021H	TM0 MSB Data Register	(TM0MSB)	0FH
022H	TM0 LSB Data Register	(TM0LSB)	0FH
023H	TM0 Status Register	(STTM0)	00H
024H	Reserved		-
025H	Reserved		-
026H	Reserved		-
027H	Reserved		-
028H	Reserved		-

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Special Control Register Map, continued

ADDR.	DESCRIPTION	ABBREVIATION	INITIAL VALUE
029H	Reserved		-
02AH	TM2 Control Register	(TM2CR)	00H
02BH	TM2 MSB Data Register	(TM2MSB)	0FH
02CH	TM2 LSB Data Register	(TM2LSB)	0FH
02DH	TM2 Status Register	(STTM2)	00H
02EH	TM2 Trigger Condition Register	(TGTM2)	00H
02FH	TM3 Control Register	(TM3CR)	00H
030H	TM3 MSB Data Register	(TM3MSB)	0FH
031H	TM3 LSB Data Register	(TM3LSB)	0FH
032H	TM3 Status Register	(STTM3)	00H
033H	Reserved		-
034H	Interrupt Enable Flag	(ENINT)	00H
035H	Stop Mode Released Flag	(STPRF)	08H
036H	Hold Mode Released Flag 1	(HMRF1)	00H
037H	Hold Mode Released Flag 2	(HMRF2)	00H
038H	Hold Mode Released Flag 3	(HMRF3)	00H
039H	Interrupt Control Register 1	(INTCT1)	00H
03AH	Interrupt Control Register 2	(INTCT2)	00H
03BH	Interrupt Control Register 3	(INTCT3)	00H
03CH	Hold Released Status Flag 1	(HRSTS1)	00H
03DH	Hold Released Status Flag 2	(HRSTS2)	00H
03EH	Hold Released Status Flag 3	(HRSTS3)	00H
03FH	Beep Tone Generator Register	(BTGR)	00H

6.2.2 Stack Register Area

There is one 8-bit stack pointer in this chip, and the stacks located address are 040H to 0FFH. After power on reset the stack pointer will be set to 0FFH. The stack pointer will be decreased by 4 when the CALL/CALLP or interrupt is accepted, and will be increased by 4 when the RTN or RTNI instruction is executed. The format of the stack content is shown in the following table.

	:	:	:	
0F8H	Z	C	—	PC12
0F9H	PC11	PC10	PC9	PC8
0FAH	PC7	PC6	PC5	PC4
0FBH	PC3	PC2	PC1	PC0
0FCH	Z	C	—	PC12
0FDH	PC11	PC10	PC9	PC8
0FEH	PC7	PC6	PC5	PC4
0FFH	PC3	PC2	PC1	PC0

Stack 1

Stack 0

6.2.3 Working Register Area

The located area from 040H to 04FH is known as working register. The instruction MOV WRn, A or MOV A, WRn can move the A accumulator data to the working register or move working register data to the A accumulator directly within the 1 word/1 machine cycle. The other direct instructions such as MOV Mx, A or MOV A, Mx instruction are 2 words/2 machine cycles. Therefore the working register can save the program memory size in ROM and improve the control speed in μ C application circuit.

Only the WR0 to WR7 are available in the arithmetic and logic operation (i.e. only 040H to 047H can be active). The instructions are as follows:

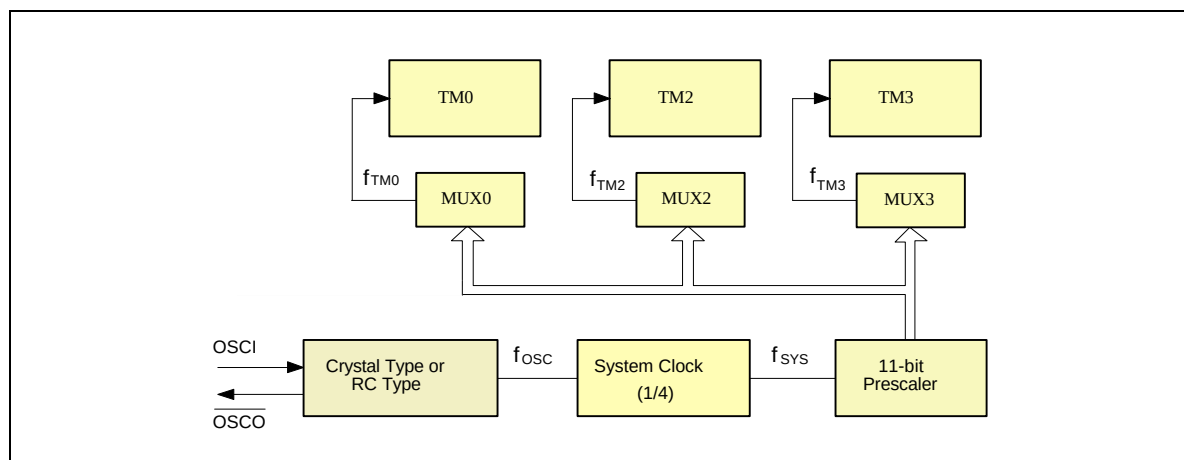
```

ADD  A,  WRx
ADC  A,  WRx
SUB  A,  WRx
SBC  A,  WRx
ANL  A,  WRx
ORL  A,  WRx
XRL  A,  WRx
CMP  A,  WRx

```

where x = 0 to 7.

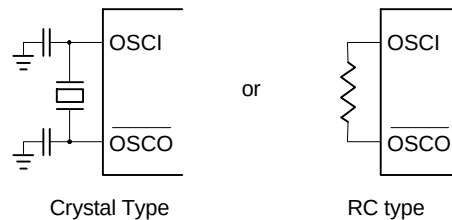
6.3 Internal Oscillator Circuit



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The W921E400A/W921C400 provides a crystal or RC oscillation circuit selected by bit0 of INI register (refer to section 6.14) to generate the system clock through external connections. If a crystal oscillator is used, a crystal or ceramic resonator must be connected to OSCI and $\overline{\text{OSCO}}$, and the capacitor must be connected if an accurate frequency is needed. The oscillator configuration is shown as follows.



6.4 Initial State

The W921E400A/W921C400 is reset either by a power-on reset or by using the external $\overline{\text{RESET}}$ pin. The initial state of the W921E400A/W921C400 after the reset function is executed is described below. The EVF interrupt request signal register value is random, so user must do CLR EVF,#11111111b instruction to clear all interrupt request signals after power-on reset.

Program counter (PC)	0000H
Stack pointer	0FFH
Special function registers	Refer to section 6.2.1
TM0, TM2, TM3 input clock	Fosc / 8
TM0, TM2, TM3 contents	0FFH
I/O port	Input mode
PM registers	1111B
DTMF output	Disable (H-Z)
EVF interrupt request signal register	Random

6.5 Input/Output

There are 21 I/O pins. All the I/O pins will remain in the input mode after power on reset.

The I/O instructions are described as follows:

```

MOV    A, Px    Input port x to A accumulator
MOV    B, Px    Input port x to B accumulator
MOV    Px, A    Output A accumulator data to port x.
MOV    Px, B    Output B accumulator data to port x.
    
```

The input or output status of port 2 to port 6 can be pin controlled by port mode register (PMx, where x = 2 to 6). Data 0 in PMx indicates the corresponding pin as output mode, and data 1 indicates the relative pin as input mode. For example, MOV PM3, #0101B, it sets P3.0 and P3.2 in input mode and P3.1 and P3.3 in output mode. The I/O instructions don't affect the input or output mode in port2 to port6.

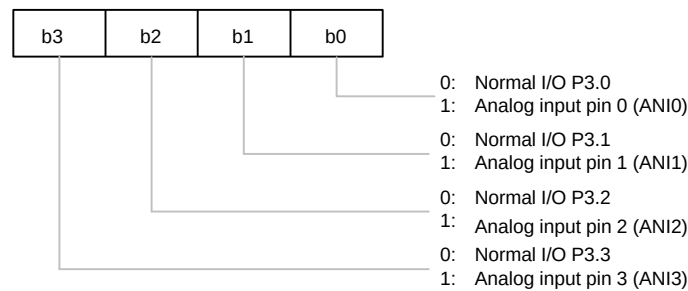
The input or output mode of port A to port B only can be decided by I/O instructions. For example, MOV A, Px will change Px to input mode and MOV Px, A will change it to output mode.

6.5.1 Normal/Special function selection of I/O

Some of the I/O ports can be programed to special function via special control register. The detail functions are as follows.

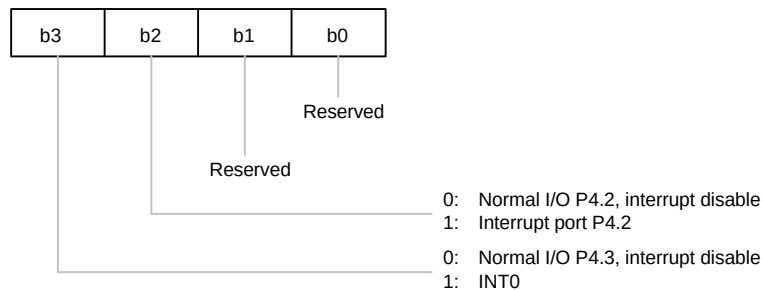
- P2.0 to P2.1: Two 15 mA sink current normal I/O pins only
- P3.0 to P3.3: Multi-function I/O pins (selected by P3IO register)
 - Normal function I/O pins
 - Special function input pins

P3IO register: (address = 00FH, default data = 0H)



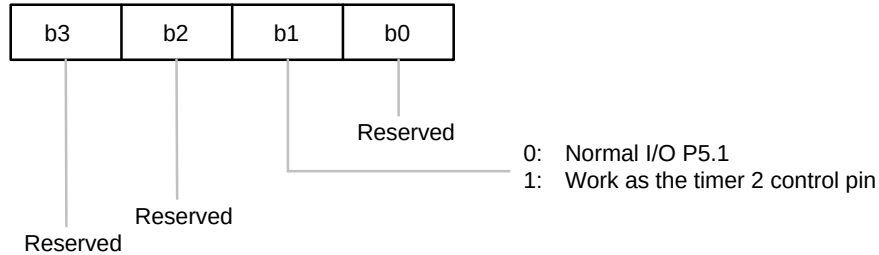
- P4.2 to P4.3: Multi-function I/O pins (selected by P4IO register)
 - Normal function I/O pins
 - Special function input pins: (All the pins are falling edge active)

P4IO register: (address = 010H, default data = 0H)



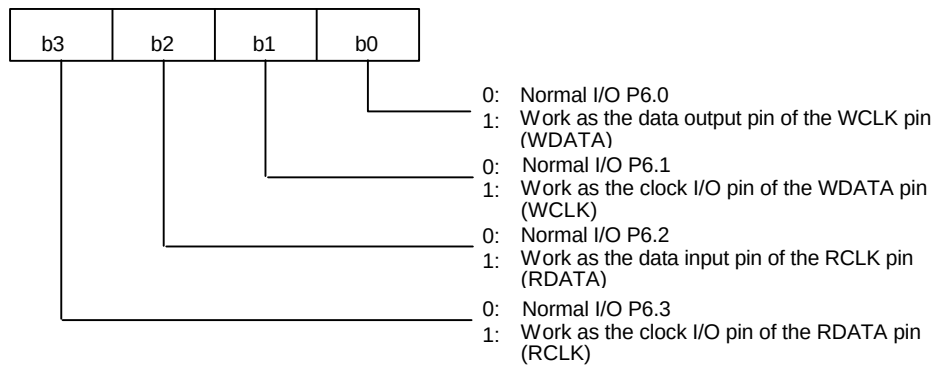
- P5.1: Multi-function I/O pins (selected by P5IO register)
 - Normal function I/O pins
 - Special function I/O pins

P5IO register: (address = 011H, default data = 0H)



- P6.0 to P6.3: Multi-function I/O pins (selected by P6IO register)
 - Normal function I/O pins
 - Special function I/O pins

P6IO register: (address = 012H, default data = 0H)



- PA.0 to PA.3: Normal function I/O pins only
- PB.0 to PB.3: Normal function I/O pins only

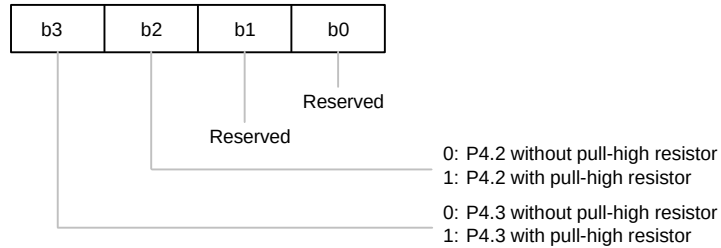
6.5.2 Pull High and Open Drain Control of I/O

Some of the above I/O ports can be controlled with pull-high resistor or open drain by programming the special register.

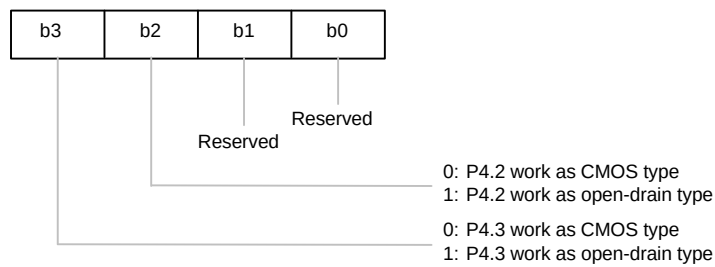
All pull-high resistors of the following table are 400 K Ω in 3.0 voltage test condition. After power on reset the following special register will all reset to '0H'.

- P4.2 to P4.3:

P4PH register: (address = 003H, default data = 0H)

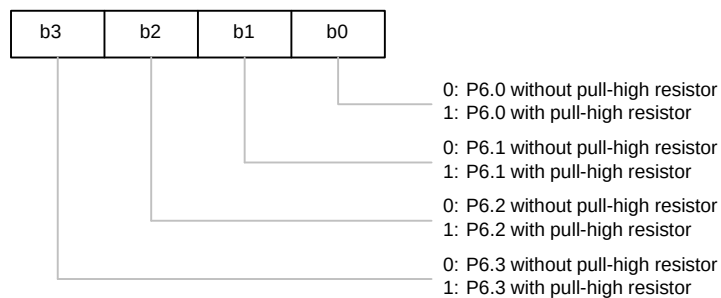


P4TP register: (address = 004H, default data = 0H)

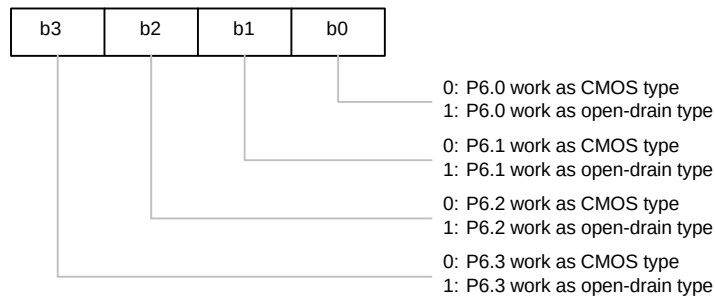


- P6.0 to P6.3:

P6PH register: (address = 005H, default data = 0H)

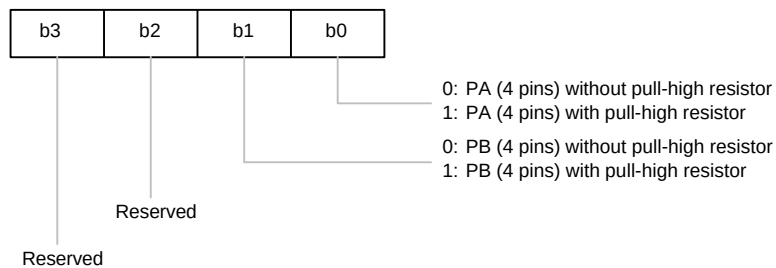


P6TP register: (address = 006H, default data = 0H)

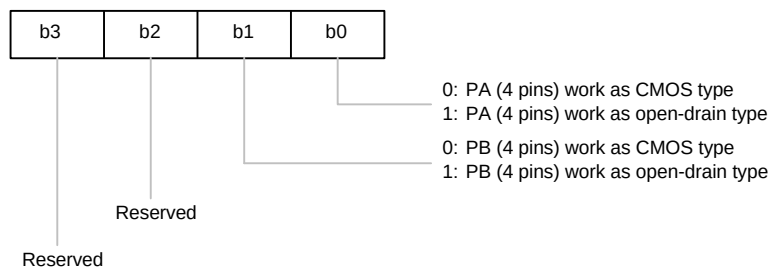


• PA, PB:

PABPH register: (address = 007H, default data = 0H)

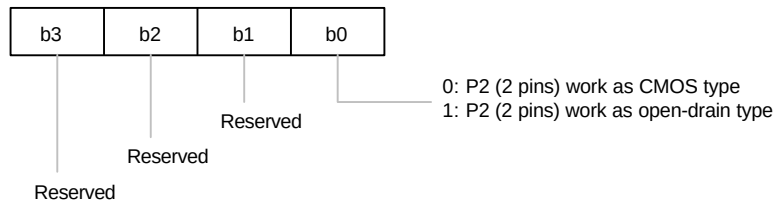


PABTP register: (address = 008H, default data = 0H)



- P2:

P2TP register: (address = 00DH, default data = 0H)



6.6 Serial Port

The W921E400A/W921C400 has a clock-synchronous serial interface which transmits and receives 8-bit data as default. User can program the P6IO register to select port P6 as the serial port.

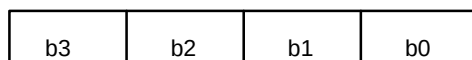
The serial transmitter/receiver function can be operated with multi-nibble function and the LSB of every nibble is transmitted/received first.

The serial transmitted/received data are come from or are stored into the serial buffer registers (address 050H to 14EH); how many nibbles will be transmitted/received is decided by the serial MSB nibble register (SRMNR, address = 0AH) and serial LSB nibble register (SRLNR, address = 09H).

SRMNR REG: (ADDRESS = 00AH, default data = 0H)

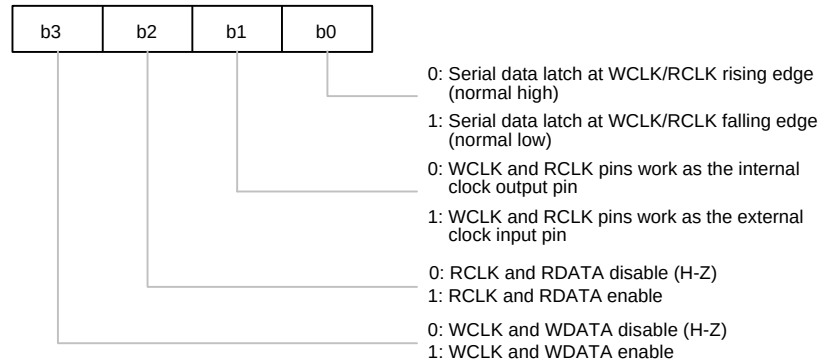


SRLNR REG: (ADDRESS = 009H, default data = 2H)

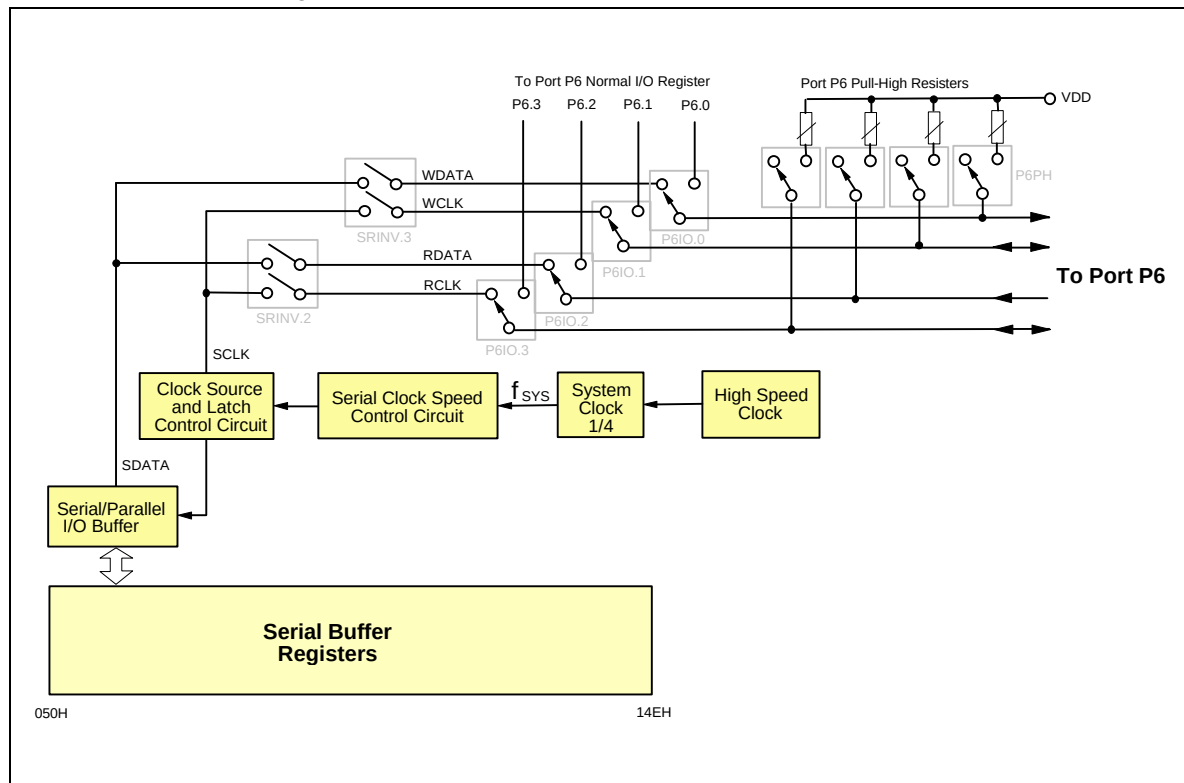


The transceiver data will be latched on the rising or falling edge of the clock; this is determined by the serial clock inverter control register (SRINV, address = 00CH). Before SOP or SIP instruction is executed the SRINV register must be set to the exact value. Once the bit3 and bit2 of SRINV register are both cleared to zero, the serial transceiver function will be reset to initial status immediately.

SRINV register: (address = 00CH, default data = 0H)



The serial interface configuration is shown below:



The internal serial clock can be controlled by the serial clock speed control register (SRSPC) and the format is as follows:

SRSPC register: (address = 00BH, default data = 0H)

b3	b2	b1	b0	Input frequency
0	0	0	0	Reserved
0	0	0	1	fsys/4 Hz
0	0	1	0	fsys/8 Hz
0	0	1	1	fsys/16 Hz
0	1	0	0	fsys/32 Hz
0	1	0	1	fsys/64 Hz
0	1	1	0	fsys/128 Hz
0	1	1	1	fsys/256 Hz
1	0	0	0	fsys/512 Hz
1	0	0	1	fsys/1024 Hz
1	0	1	0	fsys/2048 Hz

Normally the WCLK or RCLK pin will remain in high state and the serial data will be latched at the rising edge of the WCLK or RCLK signal, but the serial clock inverter control register (SRINV) will invert the above function. In this case WCLK or RCLK pin will remain in low state and the serial data will be latched at the falling edge of the WCLK or RCLK signal.

The transmitting serial clock can come from WCLK or RCLK, depending on which one is enabled. If the serial function is disabled, it will cause the relative pins to be in high impedance and it will not affect the contents of serial buffer registers (start at address 050H).

6.7 DTMF Generator

There is one dual tone multi-frequency (DTMF) generator channel in this chip. The correct DTMF output frequency is decided by the OSCCTR register as shown below.

OSCCTR register: (address = 013H, default data = 0H)

b3	b2	b1	b0	Osc. Selection
Reserved	0	0	0	400 KHz
	0	0	1	800 KHz
	0	1	0	2 MHz
	0	1	1	4 MHz
	1	0	0	Reserved
	1	0	1	3.58MHz

There are four bits in the DTMF register; the functions are described in the following table:

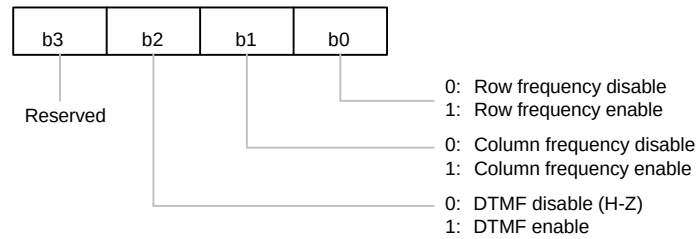
DTMF register: (address = 014H, default data = 0H)

b3	b2	b1	b0	Function Description
X	X	0	0	Column 1 (1209 Hz) output
X	X	0	1	Column 2 (1336 Hz) output
X	X	1	0	Column 3 (1477 Hz) output
X	X	1	1	Column 4 (1633 Hz) output
0	0	X	X	Row 1 (697 Hz) output
0	1	X	X	Row 2 (770 Hz) output
1	0	X	X	Row 3 (852 Hz) output
1	1	X	X	Row 4 (941 Hz) output

Note : X Å don't care

The output frequency of the row and column will be controlled by the row/column frequency control register (RCCTL).

RCCTL register: (address = 015H, default data = 0H)



The following table shows the DTMF keypad and its frequency.

C1	C2	C3	C4		
1	2	3	A	R1	
4	5	6	B	R2	
7	8	9	C	R3	
*	0	#	D	R4	

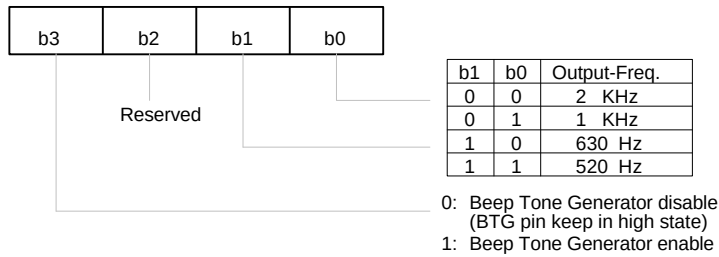
Key	Frequency
R1	697 Hz
R2	770 Hz
R3	852 Hz
R4	941 Hz
C1	1209 Hz
C2	1336 Hz
C3	1477 Hz
C4	1633 Hz



6.8 Beep Tone Generator

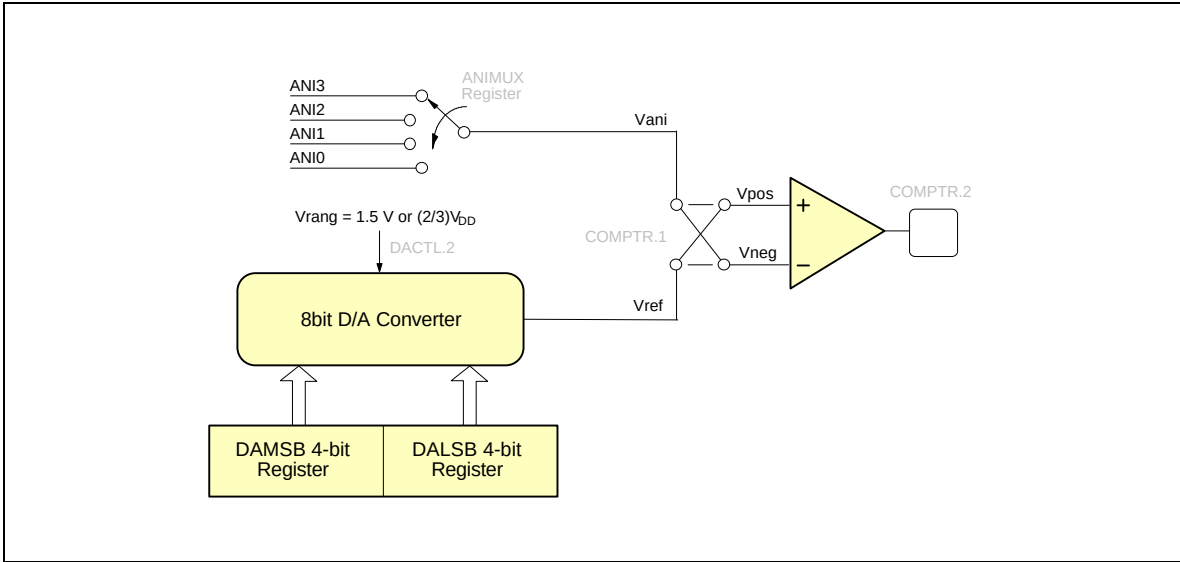
There are four kinds of frequency that can output from the BTG pin that works as beep tone generator. The BTG pin can output the special frequency -- 2 KHz, 1 KHz, 630 Hz or 520 Hz, and the correct output frequency is decided by the OSCCTR register (address = 013H) and BTGR register (address = 03FH) as shown below:

BTGR REG: (ADDRESS = 03FH, default data = 0H)



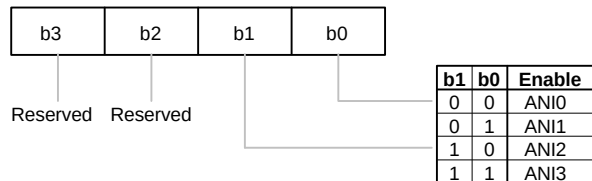
If the Beep Tone Generator is disabled by setting bit3 of the BTGR register to zero or after power on reset, the BTG output pin will remain in high state.

6.9 Comparator



There are 4-channel inputs to the comparator negative (can be programmed to positive) terminal, but only one channel will be active at a time. The control register is shown below.

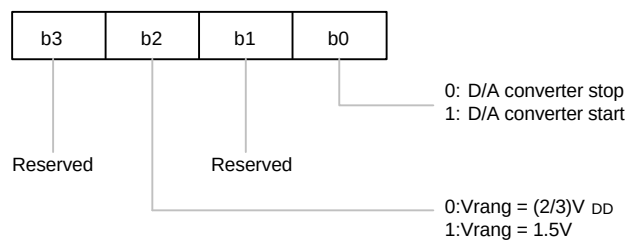
ANIMUX register: (address = 019H, default data = 0H)



The content of 8-bit D/A converter is divided into D/A MSB data register (DAMSB) and D/A LSB data register (DALSB). The block diagram is shown below.

- D/A Converter Control Register:

DACTL register: (address = 016H, default data = 0H)

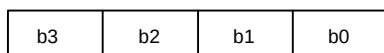


When the DACTL register bit0 is set by software, the 8-bit D/A converter starts converting. The only way to disable the D/A converter is to reset the bit0 of the DACTL register using the software control.

The power source of the D/A converter can be selected from the $(2/3)V_{DD}$ or 1.5V by programming the DACTL register bit2.

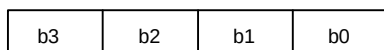
- D/A Converter LSB Data Register

DALSB register: (address = 017H, default data = 0H)

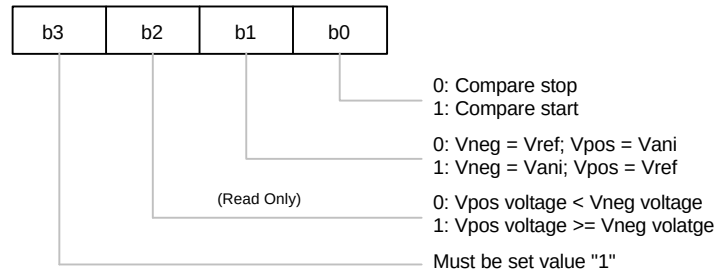


- D/A Converter MSB Data Register

DAMSB register: (address = 018H, default data = 0H)



COMPTR register: (address = 01AH, default data = DH)



When the COMPTR register bit0 is set by software, the comparator starts and the bit2 of the COMPTR register will be set to "1" initially. The comparing result will be stored in the bit2 of the COMPTR register and will keep this value until the bit0 of the COMPTR register is set again. The only way to disable the comparator is to reset the bit0 of the COMPTR register using the software control.

The initial value of the COMPTR bit2 is "1", the falling edge of COMPTR bit2 will cause the comparator interrupt to become active if the enable flag of the comparator interrupt is set.

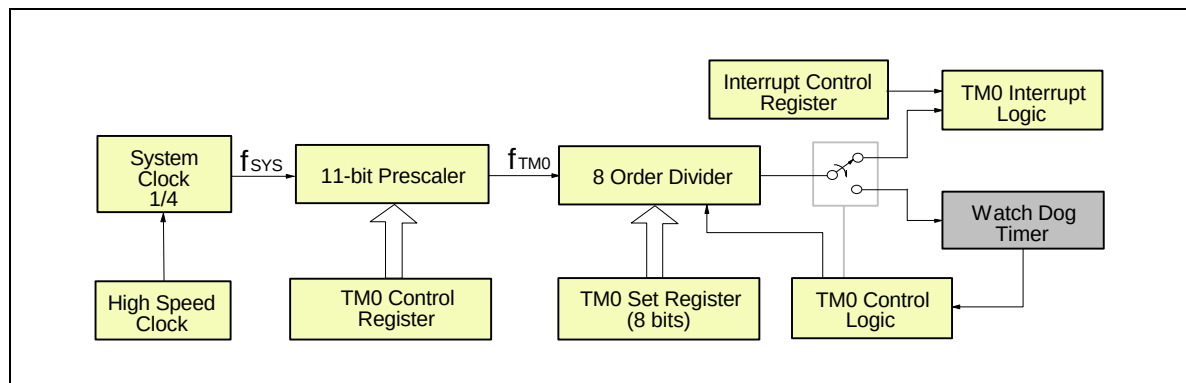
6.10 Timer/Counter

There are three timers (TM0, TM2 and TM3) in this chip, and all can be initialized at any time by writing data into the TM0, TM2 and TM3 set register.

6.10.1 TM0

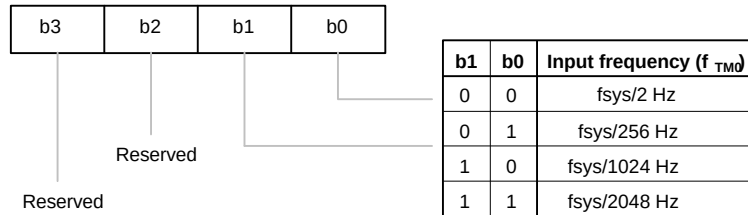
TM0 can perform the following functions:

1. 2 to 19 order divider
2. Auto-reload timer
3. Watch-dog timer



The format of the TM0 control register (TM0CR) is described below:

TM0CR register: (address = 020H, default data = 0H)



The TM0 set register is divided into TM0 MSB data register (TM0MSB register, address = 021H, default = 0FH) and TM0 LSB data register (TM0LSB register, address = 022H, default = 0FH).

TM0 will underflow when TM0 set register is from 00H to 0FFH and the value in the TM0MSB and TM0LSB will be auto reloaded to the TM0 set register when the STTM0 bit2 is set. TM0 will decrease by 1 at the frequency of timer 0 clock after the timer 0 has started.

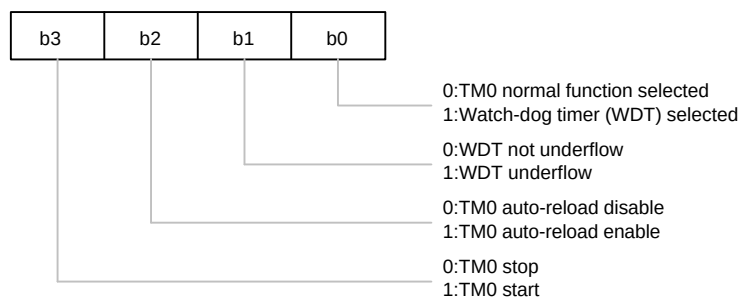
If at any time the STTM0 bit3 is from 0 to 1 (disable to enable) in the timer mode, the TM0MSB and TM0LSB will be auto reloaded to the TM0 set register again and restart the timer 0. TM0 will stop operating while the STTM0 bit3 is reset to 0.

The TM0 starts to count when the STTM0 register bit3 is set. When TM0 underflows, the STTM0 bit3 will be reset by hardware to stop TM0 if the auto-reload is disabled, but the STTM0 bit3 will not be reset if the auto-reload is enabled.

When the TM0 normal function is performed, the watch-dog timer function will be disabled automatically.

The format of the TM0 status register (STTM0) is described below:

STTM0 register: (address = 023H, default data = 0H)



If TM0 works as the watch-dog timer (WDT), the bit1 of the STTM0 register will be set when the WDT is underflow, in the meanwhile, the system is reset just as with the power on reset except the STTM0 bit1. The WDT (STTM0 bit1) will be reset to zero only with power on reset or RAM write mode.

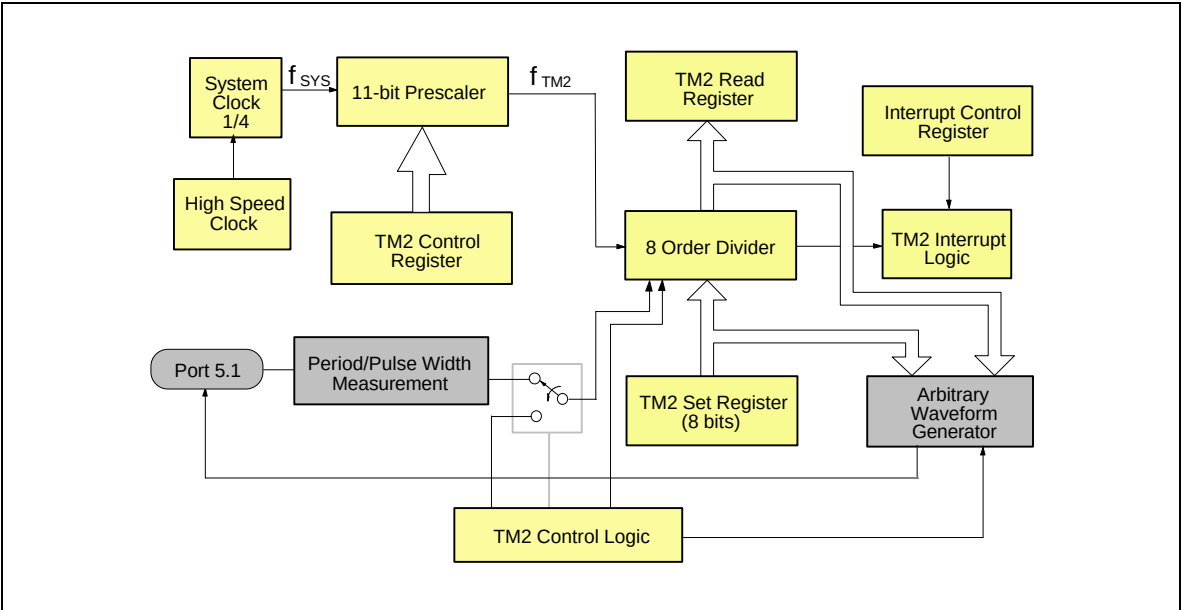
In the timer mode the time out will be the programming data subtract 1 ([TM0MSB, TM0LSB]-1). TM2 and TM3 are the same as TM0.



6.10.2 TM2

TM2 can perform the following functions:

- 1. 2 to19 order divider
- 2. Auto-reload timer
- 3. Arbitrary waveform generator
- 4. Period/pulse width measurement function



TM2CR register: (address = 02AH, default data = 0H)

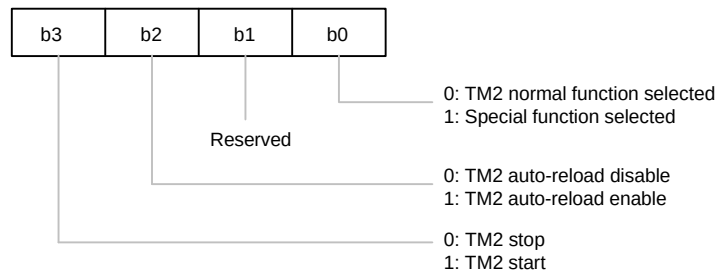
b3	b2	b1	b0	Input frequency (f_{TM2})
0	0	0	0	$f_{sys}/2$ Hz
0	0	0	1	$f_{sys}/4$ Hz
0	0	1	0	$f_{sys}/8$ Hz
0	0	1	1	$f_{sys}/16$ Hz
0	1	0	0	$f_{sys}/32$ Hz
0	1	0	1	$f_{sys}/64$ Hz
0	1	1	0	$f_{sys}/128$ Hz
0	1	1	1	$f_{sys}/256$ Hz
1	0	0	0	$f_{sys}/512$ Hz
1	0	0	1	$f_{sys}/1024$ Hz
1	0	1	0	$f_{sys}/2048$ Hz

The TM2 set register is divided into TM2 MSB data register (TM2MSB register, address = 02BH, default = 0FH) and TM2 LSB data register (TM2LSB register, address = 02CH, default = 0FH).

The TM2 read register is divided into TM2 read only MSB data register (TM2RM register, address = 01EH, default = 0FH) and TM2 read only LSB data register (TM2RL register, address = 01FH, default = 0FH).

The format of the status of TM2 register (STTM2) is described below:

STTM2 register: (address = 02DH, default data = 0H)



If the TM2 is in the timer mode, divider will underflow when it is from 00H to 0FFH and the value in the TM2MSB and TM2LSB will be auto reloaded to the TM2 set register. The TM2 will decrease by 1 at the frequency of timer 2 clock after the timer 2 has started.

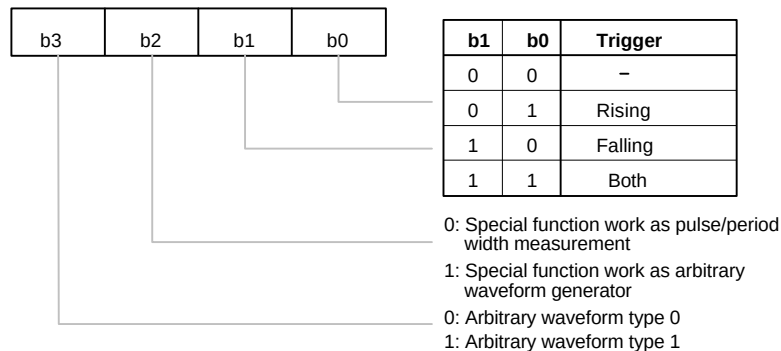
If at any time the STTM2 bit3 is from 0 to 1 (disable to enable) the TM2MSB and TM2LSB will be auto reloaded to the TM2 set register again and restart the TM2. The TM2 will stop operating when the STTM2 bit3 is reset to 0.

The TM2 starts to count when the STTM2 register bit3 is set. When TM2 underflows, the STTM2 bit3 will be reset by hardware to stop TM2 if the auto-reload is disabled, but the STTM2 bit3 will not be reset if the auto-reload is enabled.

When the TM2 normal function is performed, the special function will be disabled automatically.

The format of the TM2 trigger condition register (TGTM2) is shown below:

TGTM2 register: (address = 02EH, default data = 0H)



W921E400A/W921C400

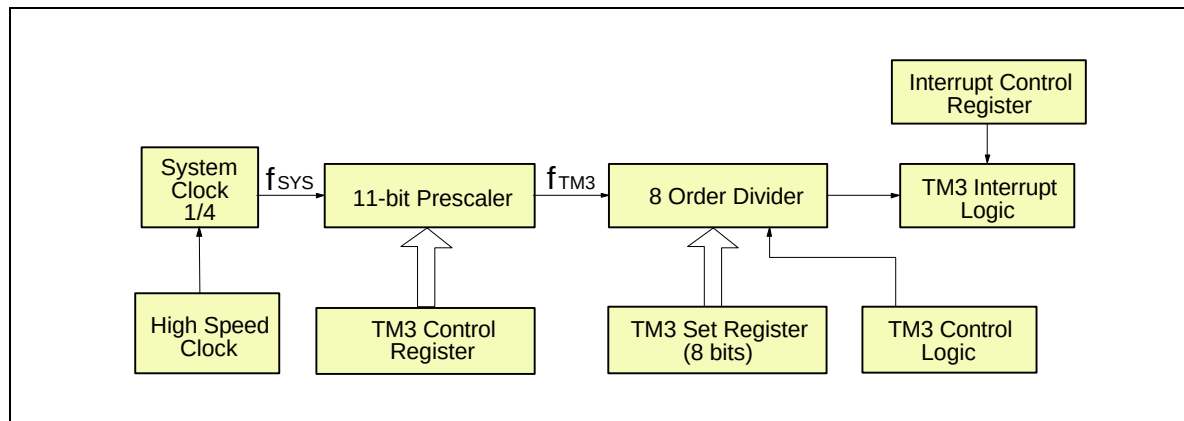


In the pulse/period width measurement mode the measuring-data is the 1'S complement of the exact data and the TM2 interrupt flag is set every 255 timer clock past or the 2nd trigger condition occurs. So the measuerd pulse/peirod width is $(255(N - 1) + \overline{TM2}) * T$, N is the number of interrupt flag occurs, $\overline{TM2}$ is the 1'S complement of timer2 register, T is the period of timer 2 clock. The special function input or output is from or to P5.1.

6.10.3 TM3

TM3 can perform the following functions:

1. 2 to19 order divider
2. Auto-reload timer



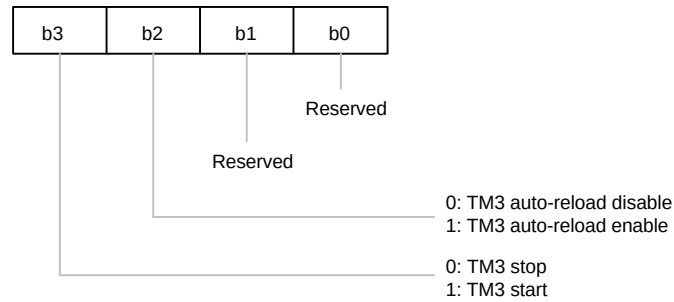
TM3CR register: (address = 02FH, default data = 0H)

b3	b2	b1	b0	Input frequency (f_{TM3})
0	0	0	0	$f_{sys}/2$ Hz
0	0	0	1	$f_{sys}/4$ Hz
0	0	1	0	$f_{sys}/8$ Hz
0	0	1	1	$f_{sys}/16$ Hz
0	1	0	0	$f_{sys}/32$ Hz
0	1	0	1	$f_{sys}/64$ Hz
0	1	1	0	$f_{sys}/128$ Hz
0	1	1	1	$f_{sys}/256$ Hz
1	0	0	0	$f_{sys}/512$ Hz
1	0	0	1	$f_{sys}/1024$ Hz
1	0	1	0	$f_{sys}/2048$ Hz

The TM3 set register is divided into TM3 MSB data register (TM3MSB register, address = 030H, default = 0FH) and TM3 LSB data register (TM3LSB register, address = 031H, default = 0FH).

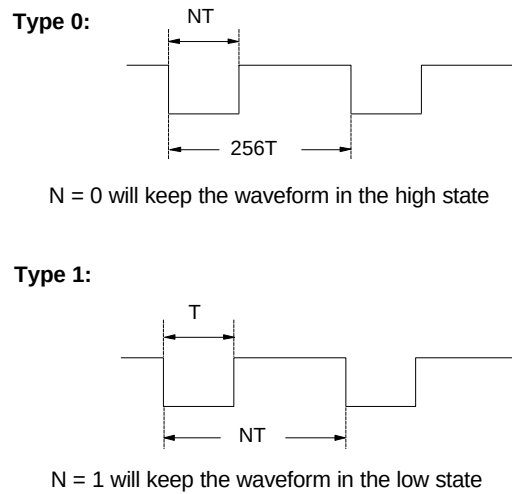
The format of the status of TM3 register (STTM3) is described below:

STTM3 register: (address = 032H, default data = 0H)



6.10.4 Arbitrary Waveform Generator

The TM2 have the arbitrary waveform generator circuit. It has function as the following description.



Note: N is the value stored in the TM2 Set Reg. (TM2MSB, TM2LSB)

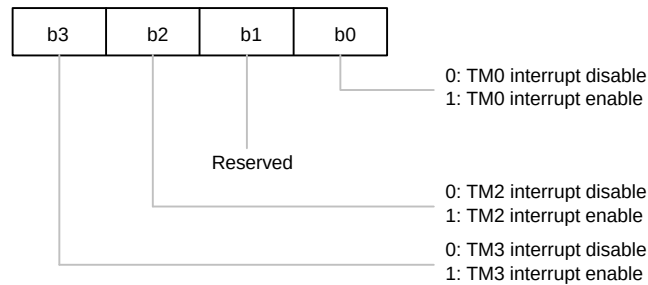
6.11 Interrupt

There are seven interrupt sources (two external and five internal sources) in the W921E400A/W921C400. All the pins of external sources (INT0 (P4.3) and port P4.2) are falling edge active. The priority of those interrupts is $INT0 > TM0 > TM2 > (\text{Comparator} / TM3) > P4.2 > SERIAL$.

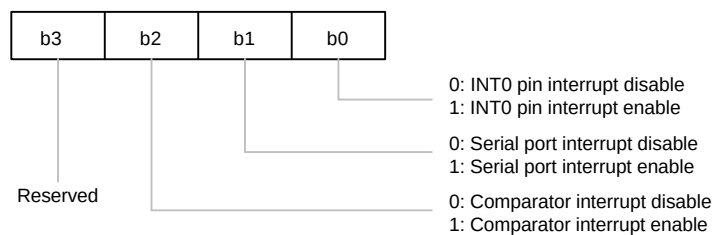
6.11.1 Interrupt Control Register

Which interrupt is enabled is controlled by the interrupt control register 1 to 3 (INTCT1 to INTCT3). The formats are shown below:

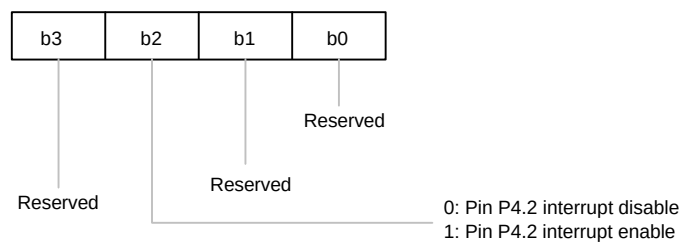
INTCT1 register: (address = 039H, default data = 0H)



INTCT2 register: (address = 03AH, default data = 0H)



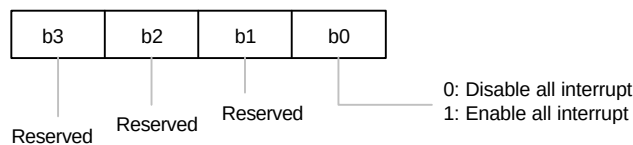
INTCT3 register: (address = 03BH, default data = 0H)



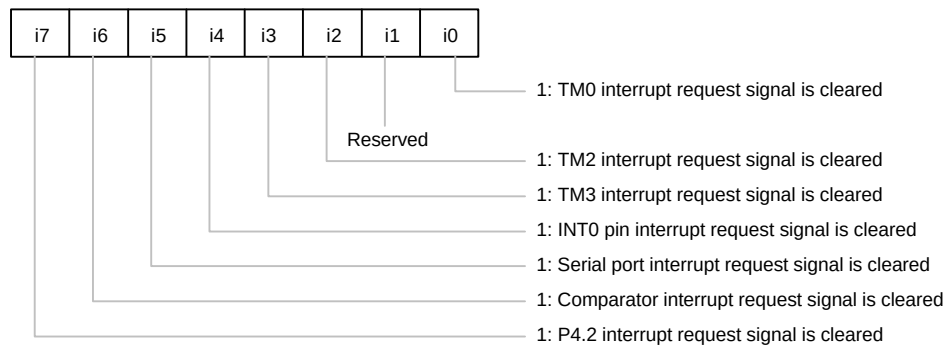
6.11.2 Interrupt Enable Flag

When the interrupt is enabled by the event, the program counter will jump to the interrupt address and the enable interrupt flag (ENINT) bit0 is cleared, at the same time, all the interrupt will be disabled. The only way to enable the interrupt again is to set the ENINT bit0 or execute the RTNI instruction.

ENINT register: (address = 034H, default data = 0H)



When the interrupt is enabled by the event, the individual interrupt request signal is cleared by the hardware automatically but the other interrupt request signals will remain the same condition. The only method of resetting the interrupt request signal is to execute the instruction CLR EVF, #I (I is a 8bits data, for example, CLR EVF, #00000001b instruction implies to clear TM0 interrupt request signal), it is a 2 words / 2 cycles instruction; the format of the immediate data is shown below.



6.12 Operating Mode

There are three types of operating mode in this chip — normal mode, hold mode and stop mode.

6.12.1 Normal Mode:

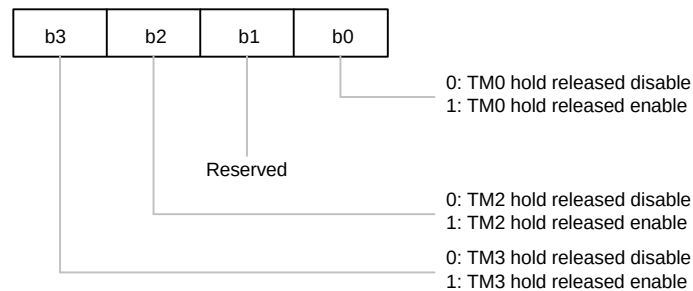
All functions works well and the μ C operates according to the clock generated by the system clock.

6.12.2 Hold Mode:

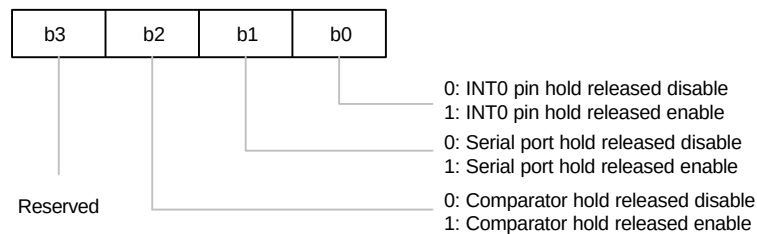
In hold mode, all operations of μ C cease, except for the operation of the oscillator, timer/counter, serial port and interrupt active pins. The μ C enters hold mode when the HOLD instruction is executed.

The hold mode can be released only by the $\overline{\text{RESET}}$ pin or the interrupt request signal. Before the device enters the hold mode, the hold mode release flag1, 2, 3 (HMRF1, 2, 3, address = 036H, 037H, 038H) must be set to define the hold mode release conditions. If interrupt condition is met and enabled in hold mode, the interrupt will be accepted to release hold mode and jump to interrupt vector to execute interrupt service routine. For more details, refer to the following flags and flow chart.

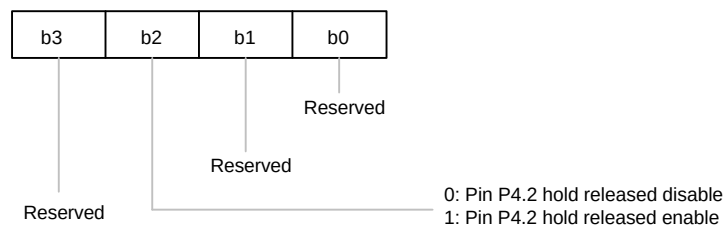
HMRF1 register: (address = 036H, default data = 0H)



HMRF2 register: (address = 037H, default data = 0H)

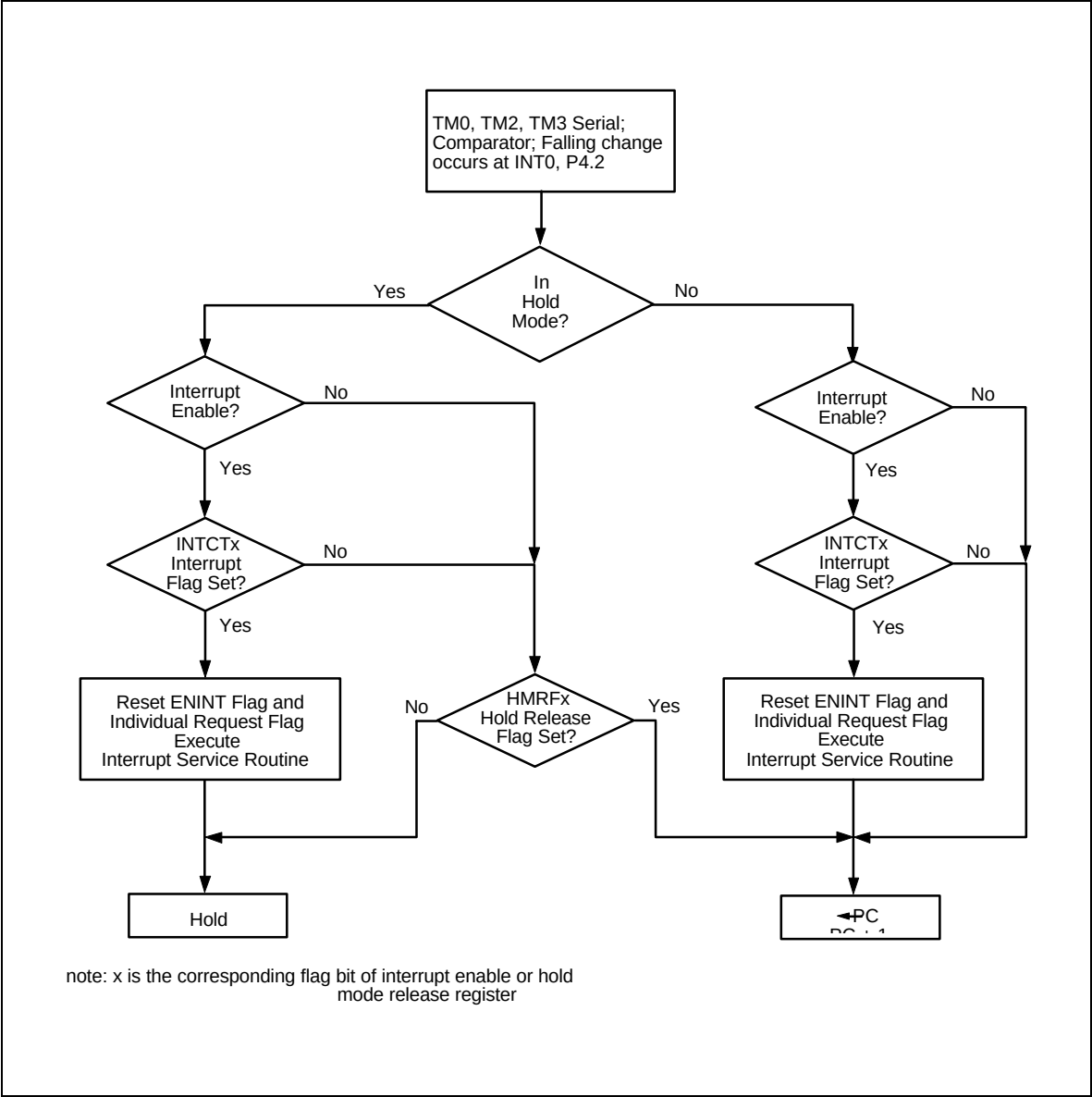


HMRF3 register: (address = 038H, default data = 0H)



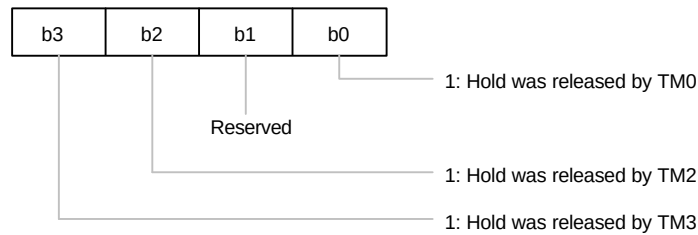


Hold mode operation flow chart

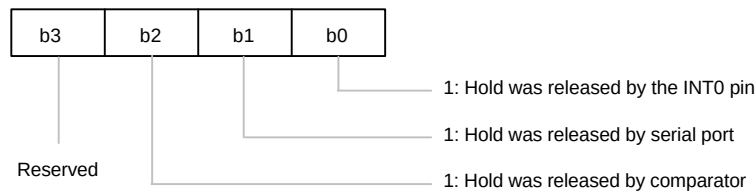


The hold released status flag1, 2, 3 (HRSTS1, 2, 3, address = 03CH, 03DH, 03EH) indicate by which interrupt source the hold mode has been released, and is loaded by hardware. When any bit of HRSTS1, 2, 3 is "1," the hold mode will be released and HOLD instruction is invalid. The bit descriptions are as follows:

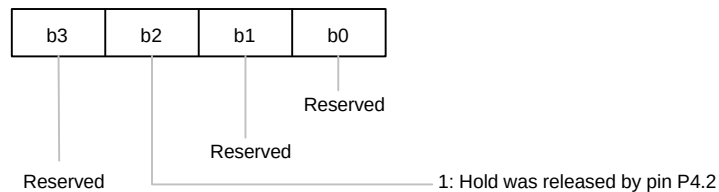
HRSTS1 register: (address = 03CH, read only, default data = 0H)



HRSTS2 register: (address = 03DH, read only, default data = 0H)



HRSTS3 register: (address = 03EH, read only, default data = 0H)



HRSTS1, 2 and 3 are read only registers and can be reset by the instruction CLR EVF, #I. When EVF has been reset, the corresponding bit of HRSTS_n (n = 1 to 3) is reset simultaneously.

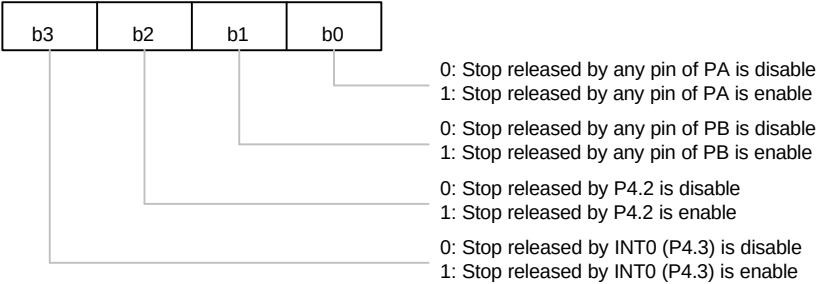
6.12.3 Stop Mode:

The μ C enters the stop mode only when the STOP instruction is executed. Because the oscillator is stopped, all functions in this chip are stopped.

The stop mode can be released by the RESET pin, INT0, P4.2, PA port or PB port. The stop condition release flag (STPRF, address = 035H) is the stop mode release control register.



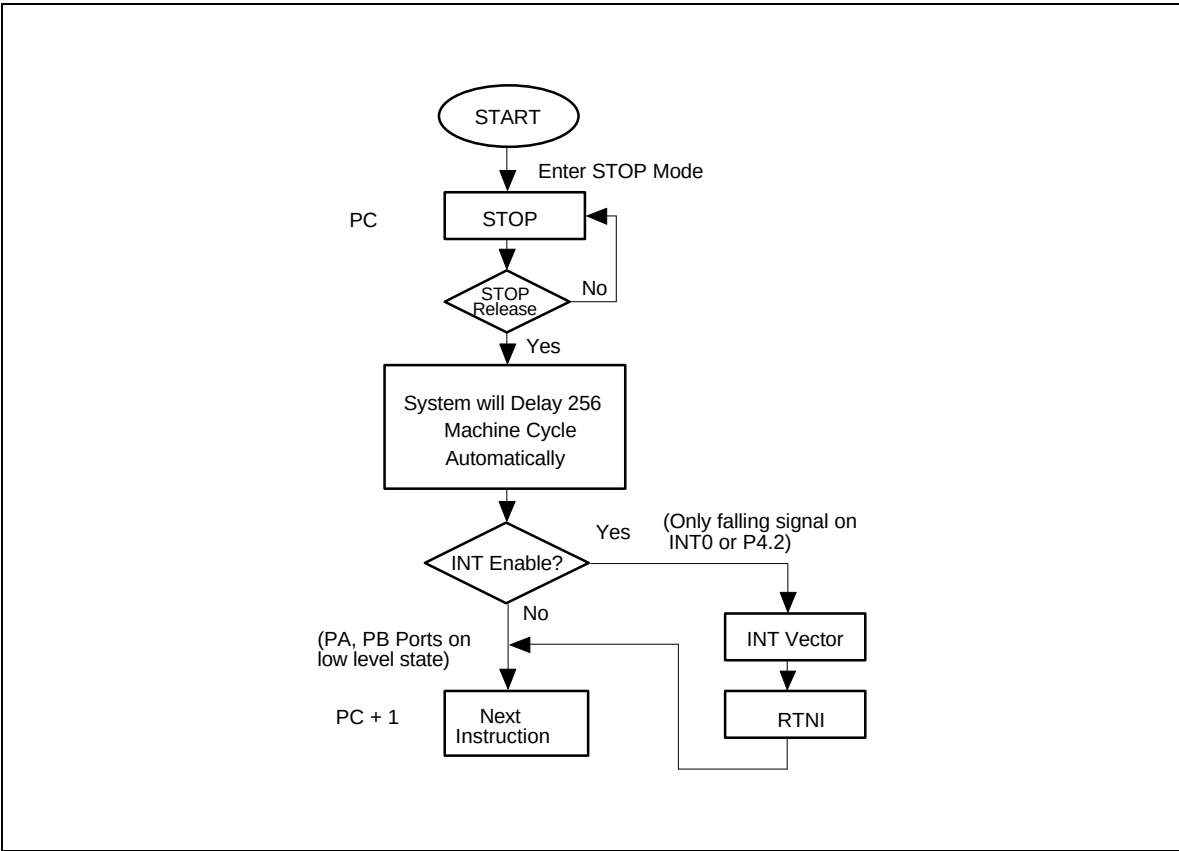
STPRF register: (address = 035H, default data = 8H)



When stop mode is active, if the stop condition release flag(STPRF) is set before the STOP instruction is executed, the low level signal on the P4, PA or PB ports will release the stop mode and a delay of 256 machine cycles occurs right aftr the stop mode is released, then the next instruction is executed or the program counter(PC) jumps to interrupt subroutine if the interrupt is enable and interrupt request exists.

The control flow chart is shown below:

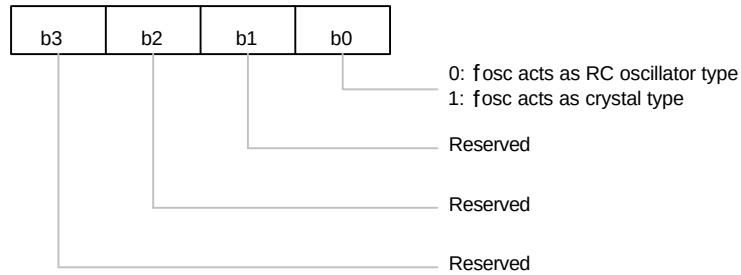
Stop mode operation flow chart



6.13 Initial Condition Register of EPROM Program Method

There is one 4-bit of the initial condition register (not part of the RAM) in W921E400A to control the micro-controller initial status after power-on. The format is described as following:

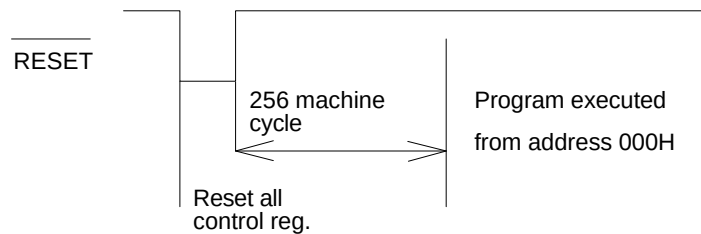
INI register: (initial value = 0FH)



6.14 Reset

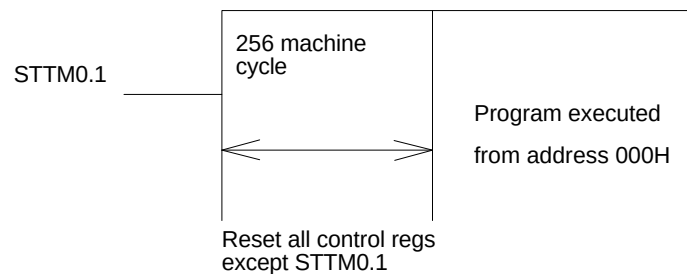
The W921E400A/W921C400 provides two reset methods, pull low $\overline{\text{RESET}}$ pin and watch dog timer reset.

6.14.1 Reset by $\overline{\text{RESET}}$



As $\overline{\text{RESET}}$ pin is pulled low, system and all control registers are reset to initial state. After $\overline{\text{RESET}}$ pin is in high level, system will delay 256 machine cycle time then program is executed from address 000H.

6.14.2 Reset by Watch Dog Timer



W921E400A/W921C400



7. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD} -V _{SS}	-0.3 to +7.0	V
Input/Output Voltage	V _{IL}	V _{SS} - 0.3	V
	V _{IH}	V _{DD} + 0.3	
	V _{OL}	V _{SS} - 0.3	
	V _{OH}	V _{DD} + 0.3	
Power Dissipation	P _D	120	mW
Operating Temperature	T _{OPR}	0 to +70	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8. ELECTRICAL CHARACTERISTICS

8.1 DC Characteristics

W921E400A EPROM TYPE

(V_{DD}-V_{SS} = 3.0V, F_{osc} = 4.0 MHz, T_A = 25° C, all outputs unloaded)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{DD}	—	2.8	3.0	5.5	V
Operating Current (Active Mode)	IOP1	Analog active V _{DD} = 5V, F _{OSC} = 4 MHz	—	9	12	mA
	IOP2	Analog disable V _{DD} = 5V, F _{OSC} = 4 MHz	—	5	7	mA
	IOP3	Analog active V _{DD} = 3V, F _{OSC} = 800 KHz	—	3.1	4.3	mA
	IOP4	Analog disable V _{DD} = 3V, F _{OSC} = 800 KHz	—	0.6	1.8	mA
	IOP5	Analog active V _{DD} = 3V, F _{OSC} = 400 KHz	—	1.0	2.0	mA
	IOP6	Analog disable V _{DD} = 3V, F _{OSC} = 400 KHz	—	0.4	1.2	mA

Publication Release Date: July 1999

W921E400A/W921C400



W921E400A EPROM Type DC Characteristics, continued

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Hold Mode Current	IHM1	VDD = 5V, FOSC = 4 MHz	–	1.2	3.5	mA
	IHM2	VDD = 3V, FOSC = 800 KHz	–	0.3	0.7	mA
	IHM3	VDD = 3V, FOSC = 400 KHz	–	0.25	0.5	mA
Stop Mode Current	ISM1	VDD = 5V, FOSC = 4 MHz	–	2.0	3.0	μA
	ISM2	VDD = 3V, FOSC = 800 KHz	–	1.0	3.0	μA
	ISM3	VDD = 3V, FOSC = 400 KHz	–	1.0	3.0	μA
Input High Voltage	VIH	–	0.7VDD	–	VDD	VDD
Input Low Voltage	VIL	–	0	–	0.3 VDD	VDD
Output High Voltage	VOH	IOH = -0.5 mA	VDD-1.0	–	–	V
Output Low Voltage	VOL1	IOL = 15 mA, port P2	–	–	2.0	V
	VOL2	IOL = 0.4 mA, other ports	–	–	0.4	
Input Leakage Current	VIL	VIN = 0V, <u>RESET</u> pin	–	–	1	μA
DTMF Output DC Level	VTDC	VDD = 2.8 to 5.5V	1.0	–	3.0	V
DTMF Distortion	THD	VDD = 2.8 to 5.5V	–	-30	-23	dB
DTMF Output Voltage	VTO	ROW Group, RL = 5 KΩ	130	150	170	mVrms
Pre-emphasis		COL/ROW	1	2	3	dB
D/A DC Reference Voltage	VREF	–	0	–	2/3	VDD
D/A Resoultion Voltage	VRSL	–	–	1/256	–	VDAC
Pull-high Resistor (P2, P4, P6, PA, PB)	RPH	VDD = 3V	–	400	–	KΩ

W921C400 MASK ROM TYPE

(V_{DD}–V_{SS} = 3.0V, F_{osc} = 4.0 MHz, T_A = 25° C, all outputs unloaded)

PARAMETER	SYM.	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Operating Voltage	VDD	4 MHz		2.4	-	5.5	V
		2 MHz		2.0	-	5.5	V
		400 KHz		2.0	-	5.5	V
Operating Current (Active Mode) (Analog all off)	IOP	VDD = 3V	4 MHz	--	1.0	--	mA
			2 MHz	--	0.7	--	mA
			400 KHz	--	0.4	--	mA
		VDD = 5V	4 MHz	--	2.5	--	mA
			2 MHz	--	2.2	--	mA
			400 KHz	--	1.5	--	mA
Hold Mode Current (Analog all off)	IHM1	VDD = 3V, Fosc = 4 MHz		--	0.5	--	mA
		VDD = 5V, Fosc = 4 MHz		--	2.0	--	mA
Stop Mode Current	ISM	VDD = 3V		–	1.0	3.0	μA
		VDD = 5V		–	1.0	3.0	μA
Input High Voltage	VIH	–		0.7 VDD	–	VDD	VDD
Input Low Voltage	VIL	–		0	–	0.3 VDD	VDD
Pull-high Resistor (P2, P4, P6, PA, PB, PC, PD)	RPH	VDD = 3V		–	400	–	KΩ
Output High Voltage	VOH	IOH = -0.5 mA		VDD – 1.0	–	–	V
Output Low Voltage	VOL1	IOL = 15 mA, port P2		–	–	2.0	V
	VOL2	IOL = 0.4 mA, Other ports		–	–	0.4	
Input Leakage Current	VIL	VIN = 0V, RESET pin		–	–	1	μA
DTMF Output DC Level	VTDC	VDD = 2.8 to 5.5V		1.0	–	3.0	V
DTMF Distortion	THD	VDD = 2.8 to 5.5V		-	-30	-23	dB
DTMF Output Voltage	VTO	ROW Group, RL = 5 KΩ		130	150	170	mVrms
Pre-emphasis		Col/Row VDD = 3.0 to 5.5V		1	2	3	dB
D/A DC Reference Voltage	VREF	–		0	–	2/3	VDD
D/A Resolution Voltage	VRSL	–		–	1/256	–	VDAC

W921E400A/W921C400



8.2 AC Characteristics

W921E400A EPROM TYPE

(V_{DD}-V_{SS} = 3.0V, F_{osc} = 4.0 MHz, T_A = 25° C, all outputs unloaded)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Frequency	FOSC1	OSCI, $\overline{\text{OSCO}}$	–	400	–	KHz
	FOSC2		–	800	–	KHz
	FOSC3		–	2	–	MHz
	FOSC4		–	3.58	–	MHz
	FOSC5		–	4	–	MHz
Instruction Cycle Time	T _I	One Machine Cycle	–	4/F _{osc}	–	S
Serial Port Data Ready Time	T _{DR}	–	200	–	–	nS
Serial Port Data Hold Time	T _{DH}	–	200	–	–	nS
$\overline{\text{RESET}}$ Active Width	T _{RAW}	–	2	–	–	TI
ROW 1 Frequency (697 Hz)	F _{ROW1}	FOSC = 4 MHz, 2 MHz, 800 KHz, 400 KHz	-0.5	–	+0.5	%
		FOSC = 3.58 MHz	-0.92	–	+0.92	
ROW 2 Frequency (770 Hz)	F _{ROW2}	same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
ROW 3 Frequency (852 Hz)	F _{ROW3}	"	-0.5	–	+0.5	%
			-0.92	–	+0.92	
ROW 4 Frequency (941 Hz)	F _{ROW4}	"	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 1 Frequency (1209 Hz)	F _{COL1}	"	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 2 Frequency (1336 Hz)	F _{COL2}	"	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 3 Frequency (1477 Hz)	F _{COL3}	"	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 4 Frequency (1633 Hz)	F _{COL4}	"	-0.5	–	+0.5	%
			-0.92	–	+0.92	
Oscillator Start Time	T _{OST}	$\overline{\text{OSCO}}$	–	2 ¹⁷ /F _{osc}	–	mS

W921E400A/W921C400



W921C400 MASK ROM TYPE

(V_{DD}–V_{SS} = 3.0V, F_{osc} = 4.0 MHz, T_A = 25° C, all outputs unloaded)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Frequency	FOSC1	OSCI, $\overline{OSCO}$	–	400	–	KHz
	FOSC2		–	800	–	KHz
	FOSC3		–	2	–	MHz
	FOSC4		–	3.58	–	MHz
	FOSC5		–	4	–	MHz
Instruction Cycle Time	T _I	One Machine Cycle	–	4/F _{osc}	–	S
Serial Port Data Ready Time	T _{DR}	–	200	–	–	nS
Serial Port Data Hold Time	T _{DH}	–	200	–	–	nS
$\overline{RESET}$ Active Width	T _{RAW}	–	2	–	–	T _I
ROW 1 Frequency (697Hz)	F _{ROW1}	FOSC = 4 MHz, 2 MHz, 800 KHz, 400 KHz	-0.5	–	+0.5	%
		FOSC = 3.58 MHz	-0.92	–	+0.92	
ROW 2 Frequency (770 Hz)	F _{ROW2}	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
ROW 3 Frequency (852 Hz)	F _{ROW3}	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
ROW 4 Frequency (941 Hz)	F _{ROW4}	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 1 Frequency (1209 Hz)	F _{COL1}	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 2 Frequency (1336 Hz)	F _{COL2}	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 3 Frequency (1477 Hz)	F _{COL3}	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
COL 4 Frequency (1633 Hz)	F _{COL4}	Same as ROW1	-0.5	–	+0.5	%
			-0.92	–	+0.92	
Oscillator Start Time	T _{OST}	$\overline{OSCO}$	–	2 ¹⁷ /F _{osc}	–	mS

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Revision A3



9. ADDRESSING MODE

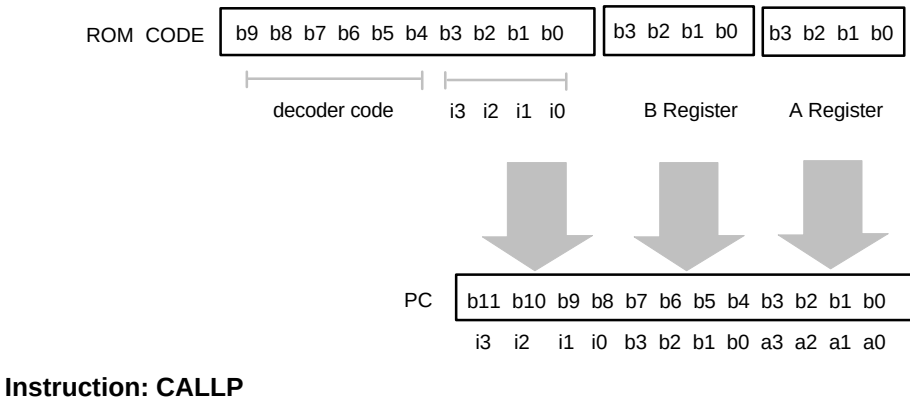
There are ROM, RAM, and Look-up table addressing modes in this chip.

9.1 ROM Addressing Mode

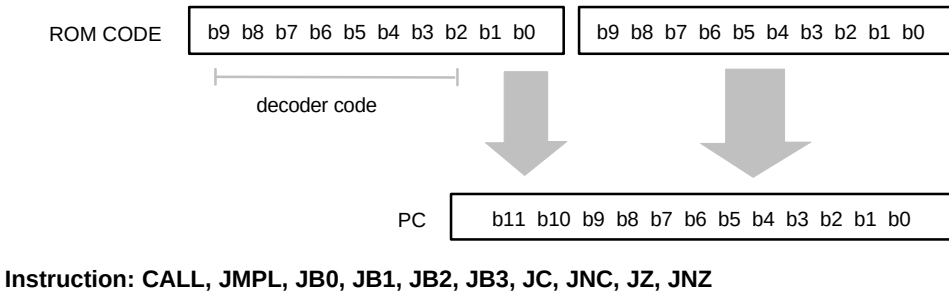
There are three types of ROM addressing mode in this chip:

- Indirect call addressing mode (0000H to 0FFFH)
- Long call/jump addressing mode (0000H to 0FFFH)

9.1.1 Indirect Call Addressing Mode: (1 word/2 cycles)



9.1.2 Long Call/Jump Addressing Mode: (2 words/2 cycles)

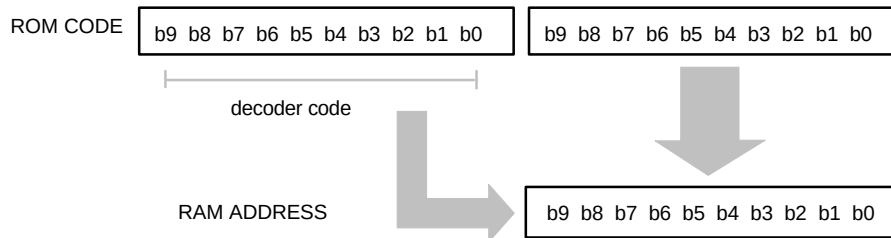


9.2 RAM Addressing Mode

There are three types of RAM addressing mode in this chip:

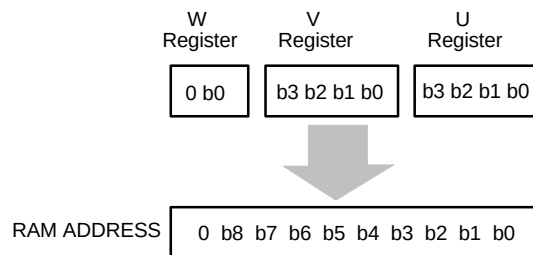
- Direct addressing mode
- Indirect addressing mode
- Working register addressing mode

9.2.1 Direct Addressing Mode: (2 words/2 cycles)



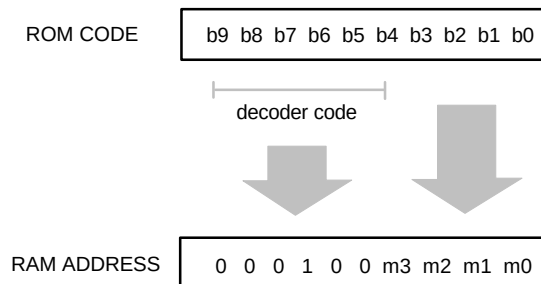
Instruction: MOV A, Mx; MOV B, Mx; MOV Mx, A; MOV Mx, B; ..., etc.

9.2.2 Indirect Addressing Mode: (1 word / 1 cycle)



Instruction: MOV A, @M; MOV B, @M; MOV @M, A; ..., etc.

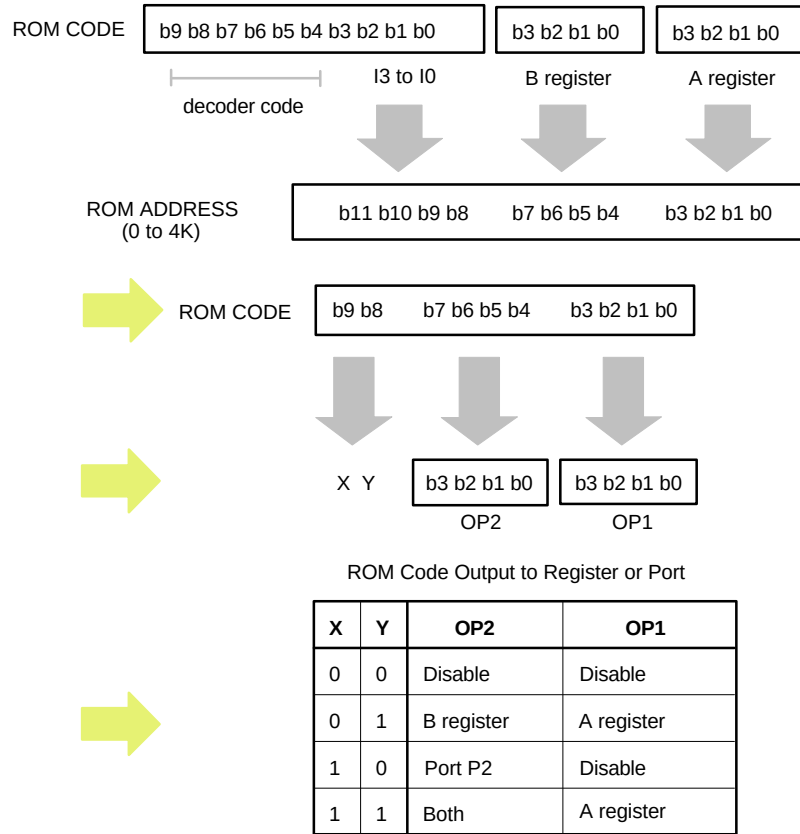
9.2.3 Working Register Addressing Mode: (1 word / 1 cycle)



Instruction: MOV A, WRn; MOV WRn, A; ..., etc.

9.3 Look-up Table Addressing Mode (1 word/2 cycles)

There is one special function look-up table addressing mode in this chip, the instruction is TBL I and the function is shown in the following table.



Example:

```

.
.
.

MOV    A, #03H
MOV    B, #01H
TBL     02H                ;A = 0CH, B = Port2 = 0DH
.
.
.

ORG    213H
DC      3DCH
.
.
.
  
```

W921E400A/W921C400



10. INSTRUCTION CODE MAP

b9 = 0

b8 = 0

MSB \ LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	MOV A, B	MOV A, Mx	MOV A, @M	MOV A, W	MOV A, V	MOV A, U		SRL A	INC B	ADD A, Mx	ADD A, @M		CLRB Mx, bit		
1	MOV B, A		MOV B, Mx	MOV B, @M					SRH A	INC DP	ADC A, Mx	ADC A, @M		CLRB @M, bit		
2	MOV Mx, A	MOV Mx, B							SLL A	DEC B	SUB A, Mx	SUB A, @M		SETB Mx, bit		
3	MOV @M, A	MOV @M, B							SLH A	DEC DP	SBC A, Mx	SBC A, @M		SETB @M, bit		
4	MOV W, A								RRC A		ANL A, Mx	ANL A, @M	CLR EVF	XCH A, B	MOV DP, #I	SOP
5	MOV V, A										ORL A, Mx	ORL A, @M				SIP
6	MOV U, A								RLC A	XRL A, B	XRL A, Mx	XRL A, @M	SET CF	XCH V, CV	HOLD	RTN
7										CMP A, B	CMP A, Mx	CMP A, @M	CLR CF	XCH U, CU	STOP	RTNI
8									ADD A, #I							
9									ADC A, #I							
A									SUB A, #I							
B									SBC A, #I							
C									ANL A, #I							
D									ORL A, #I							
E									XRL A, #I							
F									CMP A, #I							

☐ 1W/1C ☐ 1W/2C ☐ 1W/3C
☐ 2W/2C ☐ 2W/3C ☐ 3W/3C
☐ Undecided

W921E400A/W921C400



b9 = 1

b8 = 0

MSB \ LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8				JB0								JB1				
9				JB2								JB3				
A				JC								JNC				
B				JZ								JNZ				
C				JMPL								CALL				
D									CALLP							
E									TBL							
F																

☐ 1W/1C ☐ 1W/2C ☐ 1W/3C
☐ 2W/2C ☐ 2W/3C ☐ 3W/3C
☐ Undecided

W921E400A/W921C400



b9 = 1

b8 = 1

MSB \ LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0									MOV A, #I							
1									MOV B, #I							
2									MOV Mx, #I							
3									MOV @M, #I							
4			ADD A, WRn								ADC A, WRn					
5			SUB A, WRn								SBC A, WRn					
6			ANL A, WRn								ORL A, WRn					
7			XRL A, WRn								CMP A, WRn					
8									MOV A, WRn							
9									MOV A, Px							
A									MOV B, WRn							
B									MOV B, Px							
C									MOV WRn, A							
D									MOV Px, A							
E									MOV WRn, B							
F									MOV Px, B							

☐ 1W/1C ☐ 1W/2C ☐ 1W/3C
☐ 2W/2C ☐ 2W/3C ☐ 3W/3C
☐ Undecided

W921E400A/W921C400



11. INSTRUCTION SET SUMMARY

Machine code	Mnemonic	Function	A	B	U	V	W	Status	W/C	Memo
Arithmetic										
00 0000 1010, xxxxxxxxxxxx	ADD A, Mx	$A + Mx \rightarrow A$	A					Z, C	2/2	
11 0100 0 iii	ADD A, WRx	$A + WRx \rightarrow A$	A					Z, C	1/1	x = 0 ... 7
00 0000 1011	ADD A, @M	$A + @M \rightarrow A$	A		U	V	W	Z, C	1/1	
00 0001 1010, xxxxxxxxxxxx	ADC A, Mx	$A + Mx + C \rightarrow A$	A					Z, C	2/2	
11 0100 1 iii	ADC A, WRx	$A + WRx + C \rightarrow A$	A					Z, C	1/1	x = 0 ... 7
00 0001 1011	ADC A, @M	$A + @M + C \rightarrow A$	A		U	V	W	Z, C	1/1	
00 0010 1010, xxxxxxxxxxxx	SUB A, Mx	$A - Mx \rightarrow A$	A					Z, C	2/2	
11 0101 0 iii	SUB A, WRx	$A - WRx \rightarrow A$	A					Z, C	1/1	x = 0 ... 7
00 0010 1011	SUB A, @M	$A - @M \rightarrow A$	A		U	V	W	Z, C	1/1	
00 0011 1010, xxxxxxxxxxxx	SBC A, Mx	$A - Mx - C \rightarrow A$	A					Z, C	2/2	
11 0101 1 iii	SBC A, WRx	$A - WRx - C \rightarrow A$	A					Z, C	1/1	x = 0 ... 7
00 0011 1011	SBC A, @M	$A - @M - C \rightarrow A$	A		U	V	W	Z, C	1/1	
00 1000 iii i	ADD A, #I	$A + I \rightarrow A$	A					Z, C	1/1	
00 1001 iii i	ADC A, #I	$A + I + C \rightarrow A$	A					Z, C	1/1	
00 1010 iii i	SUB A, #I	$A - I \rightarrow A$	A					Z, C	1/1	
00 1011 iii i	SBC A, #I	$A - I - C \rightarrow A$	A					Z, C	1/1	
00 1010 0001	DEC A	$A - 1 \rightarrow A$	A					Z, C	1/1	SUB A, #1
00 0010 1001	DEC B	$B - 1 \rightarrow B$		B				Z, C	1/1	
00 0011 1001	DEC DP	$DP - 1 \rightarrow DP$			U	V	W	C	1/1	
00 1000 0001	INC A	$A + 1 \rightarrow A$	A					Z, C	1/1	ADD A, #1
00 0000 1001	INC B	$B + 1 \rightarrow B$		B				Z, C	1/1	
00 0001 1001	INC DP	$DP + 1 \rightarrow DP$			U	V	W	C	1/1	
Logic										
00 0100 1010, xxxxxxxxxxxx	ANL A, Mx	$A \wedge Mx \rightarrow A$	A					Z	2/2	
11 0110 0 iii	ANL A, WRx	$A \wedge WRx \rightarrow A$	A					Z	1/1	x = 0 ... 7
00 0100 1011	ANL A, @M	$A \wedge @M \rightarrow A$	A		U	V	W	Z	1/1	
00 0101 1010, xxxxxxxxxxxx	ORL A, Mx	$A \vee Mx \rightarrow A$	A					Z	2/2	
11 0110 1 iii	ORL A, WRx	$A \vee WRx \rightarrow A$	A					Z	1/1	x = 0 ... 7
00 0101 1011	ORL A, @M	$A \vee @M \rightarrow A$	A		U	V	W	Z	1/1	
00 0110 1010, xxxxxxxxxxxx	XRL A, Mx	$A \oplus Mx \rightarrow A$	A					Z	2/2	
11 0111 0 iii	XRL A, WRx	$A \oplus WRx \rightarrow A$	A					Z	1/1	x = 0 ... 7
00 0110 1011	XRL A, @M	$A \oplus @M \rightarrow A$	A		U	V	W	Z	1/1	
00 0111 1010, xxxxxxxxxxxx	CMP A, Mx	$A - Mx$						Z, C	2/2	
11 0111 1 iii	CMP A, WRx	$A - WRx$						Z, C	1/1	x = 0 ... 7

W921E400A/W921C400



Instruction Set, continued

Machine code	Mnemonic	Function	A	B	U	V	W	Status	W/C	Memo
00 0111 1011	CMP A, @M	A - @M			U	V	W	Z, C	1/1	
00 0110 1001	XRL A, B	$A \oplus B \rightarrow A$	A		B			Z	1/1	
00 0111 1001	CMP A, B	A - B						Z, C	1/1	
00 1100 1111	ANL A, #I	$A \wedge I \rightarrow A$	A					Z	1/1	
00 1101 1111	ORL A, #I	$A \vee I \rightarrow A$	A					Z	1/1	
00 1110 1111	XRL A, #I	$A \oplus I \rightarrow A$	A					Z	1/1	
00 1111 1111	CMP A, #I	A - I						Z, C	1/1	
00 1110 1111	NOT A	NOT A $\rightarrow$ A	A					Z	1/1	XRL A, #F
Move										
00 0000 0001	MOV A, B	B $\rightarrow$ A	A	B				Z	1/1	
00 0000 0010, xxxxxxxxxxxx	MOV A, Mx	Mx $\rightarrow$ A	A					Z	2/2	
00 0000 0011	MOV A, @M	@M $\rightarrow$ A	A		U	V	W	Z	1/1	
00 0000 0100	MOV A, W	W $\rightarrow$ A	A				W	Z	1/1	
00 0000 0101	MOV A, V	V $\rightarrow$ A	A			V		Z	1/1	
00 0000 0110	MOV A, U	U $\rightarrow$ A	A		U			Z	1/1	
00 0001 0000	MOV B, A	A $\rightarrow$ B	A	B				—	1/1	
00 0010 0000, xxxxxxxxxxxx	MOV Mx, A	A $\rightarrow$ Mx	A					—	2/2	
00 0011 0000	MOV @M, A	A $\rightarrow$ @M	A		U	V	W	—	1/1	
00 0100 0000	MOV W, A	A $\rightarrow$ W	A				W	—	1/1	
00 0101 0000	MOV V, A	A $\rightarrow$ V	A			V		—	1/1	
00 0110 0000	MOV U, A	A $\rightarrow$ U	A		U			—	1/1	
00 0001 0010, xxxxxxxxxxxx	MOV B, Mx	Mx $\rightarrow$ B		B				—	2/2	
00 0001 0011	MOV B, @M	@M $\rightarrow$ B		B	U	V	W	—	1/1	
00 0010 0001, xxxxxxxxxxxx	MOV Mx, B	B $\rightarrow$ Mx		B				—	2/2	
00 0011 0001	MOV @M, B	B $\rightarrow$ @M		B	U	V	W	—	1/1	
11 0000 1111	MOV A, #I	I $\rightarrow$ A	A					Z	1/1	
11 0001 1111	MOV B, #I	I $\rightarrow$ B		B				—	1/1	
11 0010 1111, xxxxxxxxxxxx	MOV Mx, #I	I $\rightarrow$ Mx						—	2/2	
11 0011 1111	MOV @M, #I	I $\rightarrow$ @M			U	V	W	—	1/1	
11 1000 nnnn	MOV A, WRn	WRn $\rightarrow$ A	A					Z	1/1	
11 1001 xxxx	MOV A, Px	Px $\rightarrow$ A	A					Z	1/1	
11 1010 nnnn	MOV B, WRn	WRn $\rightarrow$ B		B				—	1/1	
11 1011 xxxx	MOV B, Px	Px $\rightarrow$ B		B				—	1/1	
11 1100 nnnn	MOV WRn, A	A $\rightarrow$ WRn	A					—	1/1	
11 1101 nnnn	MOV Px, A	A $\rightarrow$ Px	A					—	1/1	
11 1110 xxxx	MOV WRn, B	B $\rightarrow$ WRn		B				—	1/1	

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Instruction Set, continued

Machine code	Mnemonic	Function	A	B	U	V	W	Status	W/C	Memo
11 1111 xxxx	MOV Px, B	B → Px		B					1/1	
10 0xxx iiii	MOV PMx, #I	I → PMx							1/1	Mode of Port 2 to 6
Serial I/O										
00 0100 1111	SOP	—							*1	
00 0101 1111	SIP	—							*1	
Rotate or Shift										
00 0000 1000	SRL A	An→An-1, 0→A3	A					Z	1/1	n = 3 to 1
00 0001 1000	SRH A	An→An-1, 1→A3	A					Z	1/1	n = 3 to 1
00 0010 1000	SLL A	An→An+1, 0→A0	A					Z	1/1	n = 0 to 2
00 0011 1000	SLH A	An→An+1, 1→A0	A					Z	1/1	n = 0 to 2
00 0100 1000	RRC A	An→An-1, A0→C, C→A3	A					Z, C	1/1	n = 3 to 1
00 0110 1000	RLC A	An→An+1, A3→C, C→A0	A					Z, C	1/1	n = 0 to 2
Branch										
10 1000 00aa, aaaaaaaaaa	JB0 addr	Addr → PC							2/2	
10 1000 10aa, aaaaaaaaaa	JB1 addr	Addr → PC							2/2	
10 1001 00aa, aaaaaaaaaa	JB2 addr	Addr → PC							2/2	
10 1001 10aa, aaaaaaaaaa	JB3 addr	Addr → PC							2/2	
10 1010 00aa, aaaaaaaaaa	JC addr	Addr → PC							2/2	
10 1010 10aa, aaaaaaaaaa	JNC addr	Addr → PC							2/2	
10 1011 00aa, aaaaaaaaaa	JZ addr	Addr → PC							2/2	
10 1011 10aa, aaaaaaaaaa	JNZ addr	Addr → PC							2/2	
10 1100 00aa, aaaaaaaaaa	JMPL addr	Addr → PC							2/2	Long jump
10 1100 10aa, aaaaaaaaaa	CALL addr	Addr → PC							2/2	
10 1101 aaaa	CALLP addr	@Addr → PC	A	B					1/2	Indirect address call
10 1110 aaaa	TBL addr		A	B				Z	1/2	Look-up table

*1: Depends on the SRMNR, SRLNR register

W921E400A/W921C400



Instruction Set, continued

Machine code	Mnemonic	Function	A	B	U	V	W	Status	W/C	Memo
Other										
00 0110 1111	RTN	Stack → PC							1/3	
00 0111 1111	RTNI	Stack → PC, Z, C						Z, C	1/3	ENINT active again
00 0000 0000	NOP	—							1/1	
00 0110 1110	HOLD	—							1/1	
00 0111 1110	STOP	—							1/1	
00 0001 11bb	CLRB @M, bit	0 → @M(b)			U	V	W		1/1	
00 0000 11bb, xxxxxxxxxxxx	CLRB Mx, bit	0 → Mx(b)							2/2	
00 0011 11bb	SETB @M, bit	1 → @M(b)			U	V	W		1/1	
00 0010 11bb, xxxxxxxxxxxx	SETB Mx, bit	1 → Mx(b)							2/2	
00 0111 1100	CLR CF	0 → C						C	1/1	
11 0000 0000	CLR A	0 → A	A					Z	1/1	MOV A, #0
00 0100 1100, 00iiiiiii	CLR EVF, #I	—							2/2	
00 0110 1100	SET CF	C = 1						C	1/1	
00 0100 1110, iiiiiiiiii	MOV DP, #I	I → DP			U	V	W		2/2	
00 0111 1101	XCH U, CU	U ↔ CU			U				1/1	
00 0110 1101	XCH V, CV	V ↔ CV				V			1/1	
00 0100 1101	XCH A, B	A ↔ B	A	B				Z	1/1	

*DP = {W, V, U}

*@M = {@W, V, U}

*@Addr = {I, B, A} to be a target address for the CALLP instruction

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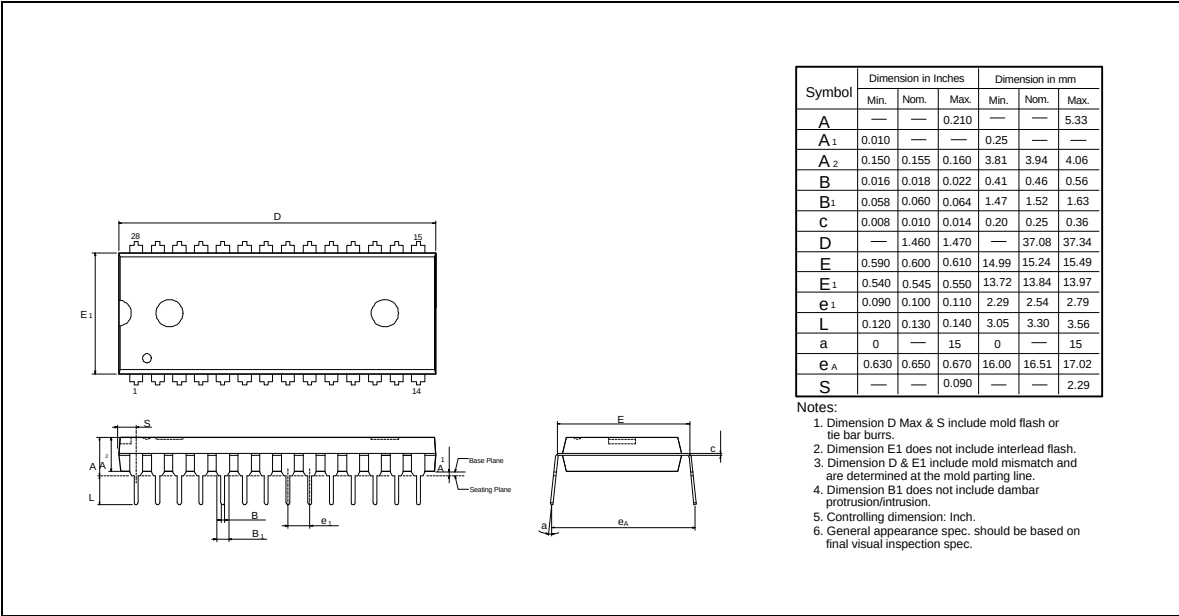
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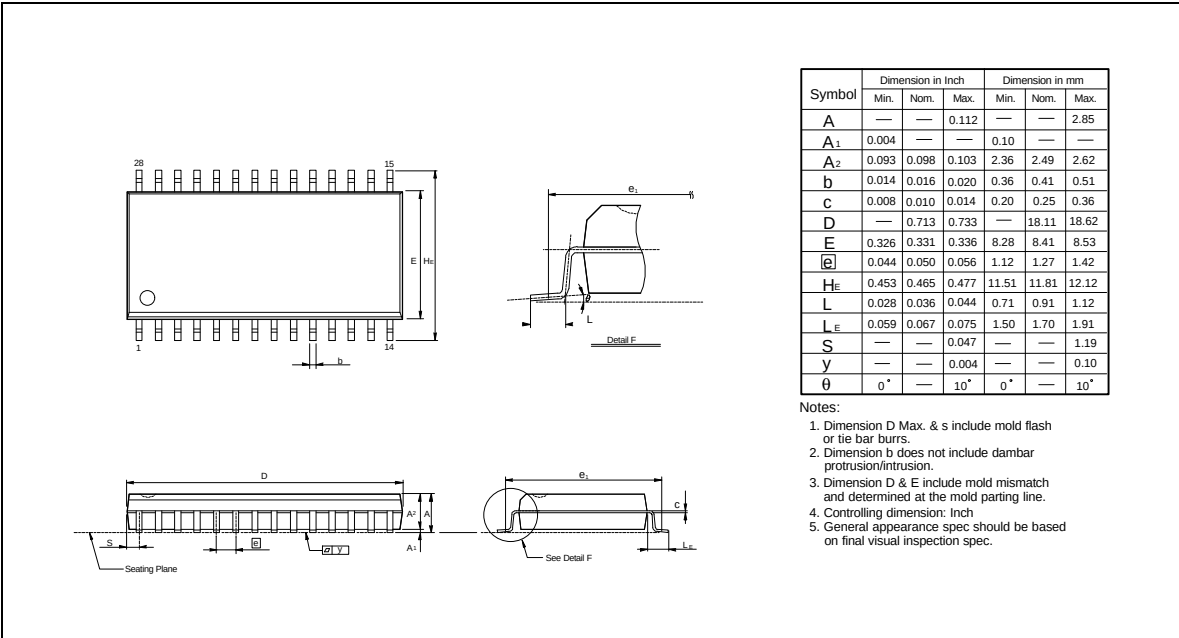


12. PACKAGE DIMENSIONS

28-pin DIP



28-pin SOP



W921E400A/W921C400



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Note: All data and specifications are subject to change without notice.