Winbond Electronics Corp.

HIGH FIDELITY *POWER SPEECH*ä

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Revision A5

I. GENERAL DESCRIPTION

W583xxx is fabricated using the Winbond CMOS process. The W583xxx family is a new member of the *PowerSpeech*ä synthesizer series, with voice quality which is even better than before. The W58300 is a ROMless chip that can support up to maximal 16M bits memory size; the voice length can reach 8.5 minutes. When combined with flash memory W55F05 or W55F20, this chip can be used to demonstrate W583xxx series products like the W583M02, W58S30, W583S10, etc.

The W583xxx family has adopted the same architecture as the *PowerSpeech*ä synthesizers while replacing the 4-bit ADPCM algorithm with Winbond's high fidelity speech synthesis algorithm to produce better quality voice. W58xxx provides IR(infrared) function, CPU interface and voice output in DAC current or PWM type.

According different voice duration, there are 11 bodies in W583xxx family, list them below.

PART NO.	**W583S10**	**W583S15**	**W583S20**	**W583S25**	**W583S30**	**W583S40**
Duration	10 sec	15 sec	20 sec	25 sec	30 sec	40 sec
ROM (K bits)	384	640	768	896	1024	1472
PART NO.	**W583S50**	**W583S60**	**W583S80**	**W583S99**	**W583M02**	
Duration	50 sec	60 sec	80 sec	99 sec	120 sec	
ROM (K bits)	1760	2048	3072	3520	4096	

Note: (1)The voice durations are estimated by 6.4 KHz sampling rate

(2)W583S10 provides less I/O pins, and do not provide crystal oscillator.

There are 3 bodies in W583x-xx family for two chip solution, list as following.

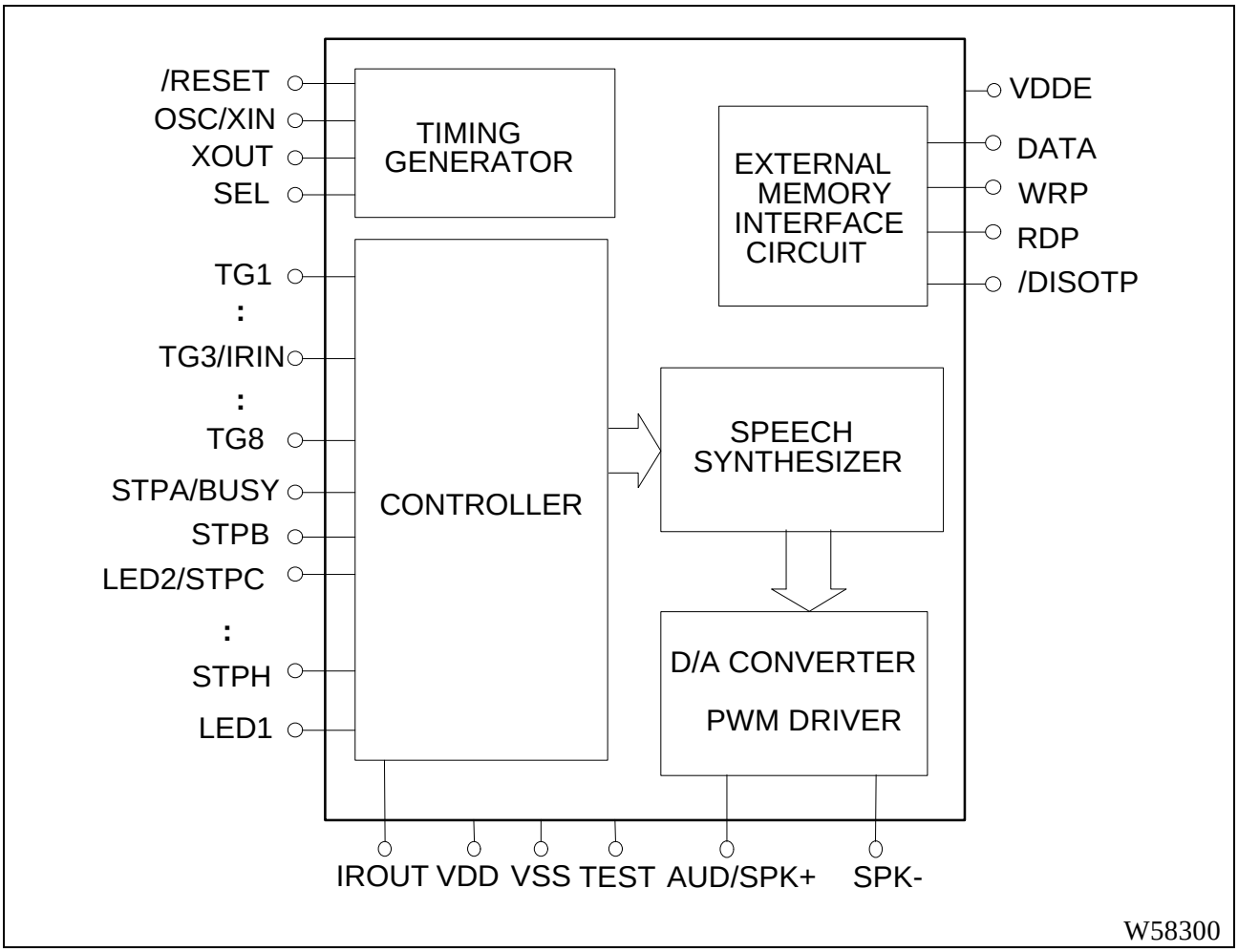
Product #	Duration	ROM	Chip Set Configuration
W583S-03	3 seconds	128 Kbits	W58300 + W55F01
W583M-03	3 minutes	6 Mbits	W58300 + W55M06
W583M-04	4 minutes	8 Mbits	W58300 + W55M08

II. FEATURES

- New high fidelity speech synthesis algorithm
- Direct drive speaker by PWM output or Built-in 8-bit D/A converter
- Wide operating voltage range: 2.4 - 5.5 Volts
- Addressing capability up to 16M bits (W58300)
- IR interface for command Transmission and Receiving
- TX, INC and MV instructions provided
- 8 trigger inputs - with separate control of falling/rising edge trigger
- 8 STOP outputs
- Supports CPU interface operation
- Pad option for Ring or Crystal oscillator
- Symbolic compiler supported

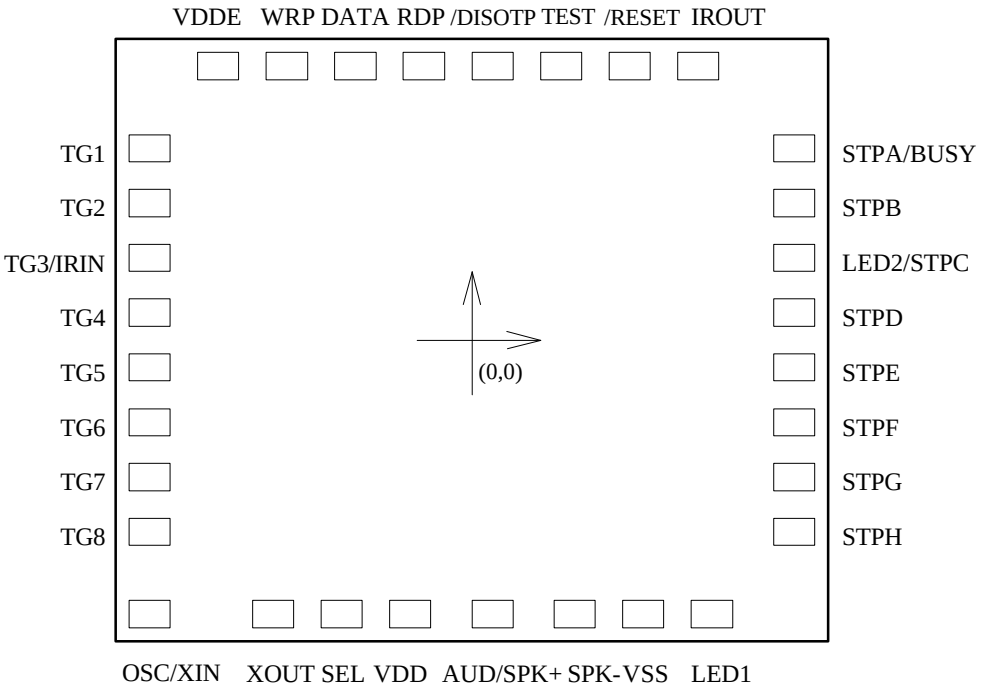
- Instruction cycle ≤ 400 μS typically
- Section control provided in each voice section
  - Variable frequency: 4.8/6/8/12 KHz
  - LED: ON/OFF
- Eight general-purpose registers R0 - R7
- Number of interrupt vector/label up to 2,048
- Register control instead of various mask options

III. BLOCK DIAGRAM (W58300)

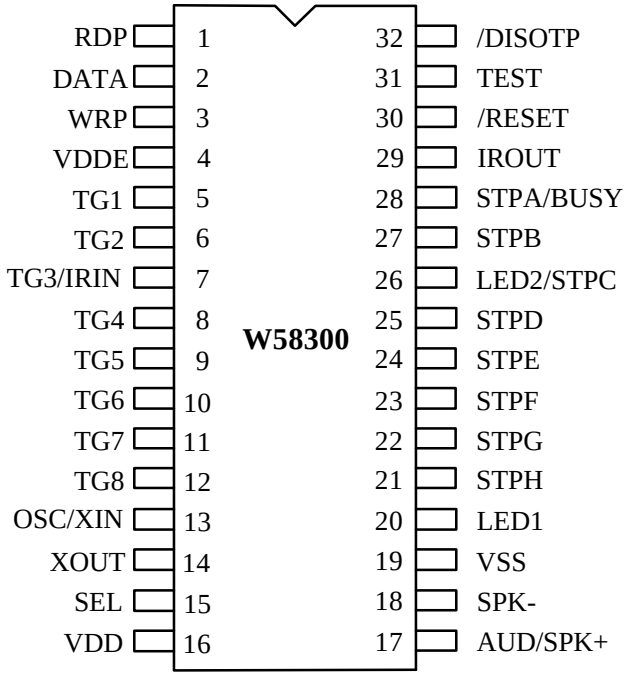


IV. PAD DIAGRAM & PIN CONFIGURATION

IV.1 PAD DIAGRAM (W58300)



IV.2 PIN CONFIGURATION (W58300)



The 32-pin P-DIP package will be used for evaluation and demo purposes.

V. PIN DESCRIPTION (W58300)

Name	I/O	Description
LED1	O	LED1 output
TEST	I	Test pin, internally pulled low
TG1	I	Direct trigger input 1, internally pulled high
TG2	I	Direct trigger input 2, internally pulled high
TG3/IRIN	I	Direct trigger input 3 or IR input, internally pulled high. Once this pin is pulled low, the oscillation circuit is active even the chip enters standby mode.
TG4	I	Direct trigger input 4, internally pulled high
TG5	I	Direct trigger input 5, internally pulled high
TG6	I	Direct trigger input 6, internally pulled high
TG7	I	Direct trigger input 7, internally pulled high
TG8	I	Direct trigger input 8, internally pulled high
STPA/BUSY	O	STOPA or Busy signal
STPB	O	STOPB
LED2/STPC	O	LED2 output or STOPC
STPD	O	STOPD
STPE	O	STOPE
STPF	O	STOPF
STPG	O	STOPG
STPH	O	STOPH
IROUT	O	IR signal output, active low
VSS	-	Negative power supply
/RESET	I	Reset all, function as POR, internally pulled high.
AUD/SPK+	O	Current type output or PWM output for speaker
SPK-	O	PWM output
VDD	-	Positive power supply. One 0.1μF capacitor must be added between V_{DD} and V_{SS}.
VDDE	-	Positive power supply for serial interface
OSC/XIN	I	Ring oscillator input or crystal input
XOUT	I/O	Crystal input or oscillator clock output for cascade application
SEL	I	Ring/Crystal oscillator selection, internally pulled high. Floating for Ring and grounded for crystal.
WRP	O	Write pulse for serial interface
DATA	I/O	DATA for serial interface
RDP	O	Read pulse for serial interface
/DISOTP	I	Disable all of the serial interface pins

V.1 TG1 - TG8

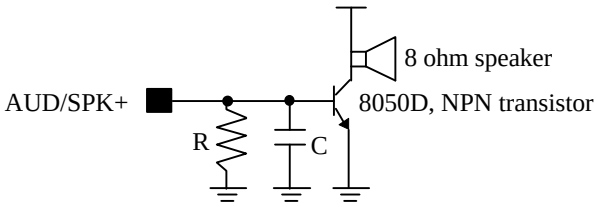
Internally pulled high by a PMOS device with an equivalent resistance of around 500KΩ. After debounced by 20-40mS, the direct trigger inputs start to execute the corresponding interrupt vectors, which are interrupt vectors 0,1,2,3,8,9,10,11 for the falling edge triggers and interrupt vectors 4,5,6,7,12,13,14,15 for the rising edge triggers of the TG1-TG8, respectively. The priority is set by internal H/W as TG1F > TG1R > TG2F > TG2R > TG3F > TG3R > TG4F > TG4R > TG5F > TG5R > TG6F > TG6R > TG7F > TG7R > TG8F > TG8R.

W583xxx implements CPU interface and IR(Infrared) function by some of the trigger pins. See FUNCTION DESCRIPTION for further details.

TG3 is not only the trigger input but also the IR input pin in W583. Because of this multi-purpose function, TG3 has special characteristic from other trigger pins. It is that if power is on and TG3 is pulled low, the oscillator will keep the oscillation even the play statement is end ("END" instruction is executed) and TG3 is disabled. That is to say, **the "END" instruction will not stop oscillator if TG3 is grounded**. For this reason, TG3 is not suitable used as an option input pin that TG3 is always tied to ground.

V.2 AUD/SPK+ and SPK-

The AUD/SPK+ pin is a current-type voice output when MODE1 register programmed as AUD output, which is connected to the output of the internal D/A converter. The full scale output of the 8-bit D/A converter is 5mA, which is able to drive the external 8-Ω speaker through the amplification of a low-power NPN transistor with a β of 120-160. Usually, an 8050D transistor is appropriate.

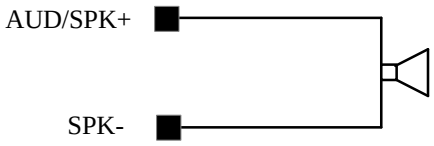


The shunt resistor R in the above figure is used to adjust the current that enters into the base of the NPN transistor for driving the external speaker without distortion, which is often encountered in such a simple amplification scheme under large input current conditions.

Two factors cause distortion, one is the saturation phenomenon of the transistor due to larger I_B, the other one is the introduction of R that cuts small signals out of the original waveform. A typical value of the shunt resistor is around 510Ω-1KΩ. The smaller the resistance, the smaller the current enters the transistor and vice versa..

The capacitor C is used for low-pass filtering the unwanted high-frequency noises that are generated from the D/A converter during sample transitions. Users may adjust the capacitance to reach better perceptual hearing. It could be simply omitted without affecting the voice quality too much.

Another case is AUD/SPK+ and SPK- act as PWM(Pulse Width Modulation) outputs. In this case DAC will be disabled. SPK+ and SPK- can directly drive a speaker without any extra component. One of these two pins will keep high in a sampling period while the other producing a low pulse with pulse width proportional to the deviation of recovery PCM to DC value.



V.3 STPA - STPH

For Stop output, these pins are inverted-type stages. User may define different Stop outputs at certain timing slot by programming *.out file of the *PowerSpeech*ä synthesizer. After compilation, the Stop signals will be controlled by the internal STOP register, which can be manipulated by register operation. Typically, the Stop signals are used to drive external components, like motors, LEDs, light bulbs, etc.

V.4 IROUT

For IR purpose, the IROUT will generate Pulse Position Modulation(PPM) waveform with or without 38 KHz (75% duty) carrier when "TX Rn" instruction is executed if hardware IR is selected. If S/W IR is selected, the IROUT will generate PPM waveform with 38 KHz (75% duty) carrier according the programming on STC bit.

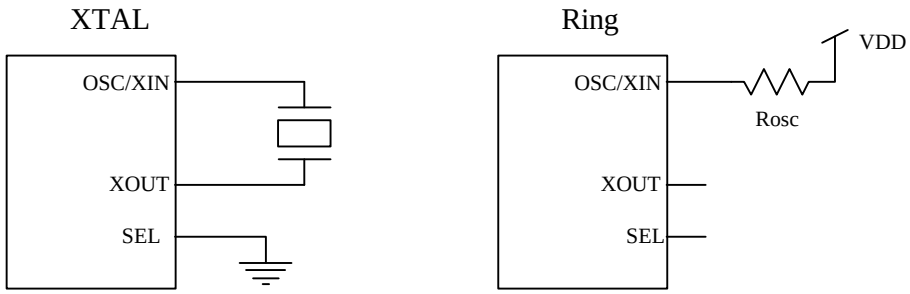
V.5 OSC/XIN, XOUT and SEL

A ring or crystal oscillator is used to generate the master frequency of around 1.5 MHz or 3 MHz.

Ring oscillator will be active when SEL pin is floating. The OSC/XIN pin is connected directly to VDD by way of an Rosc resistor, which is used to provide a bias current for the ring oscillator. For achieving a stable oscillation frequency over a wide operating voltage range, which is defined to be 2.4V-5.5V, the internal oscillator has to abide by the requirements of frequency deviation listed in the AC Spec.

Crystal oscillator will be selected when SEL pin is tied to VSS. A 1.5 MHz or 3 MHz crystal is suggested to be added between OSC/XIN and XOUT.

For the application adopting DAC driver voice output and ring oscillator, 1.5 MHz oscillator is suggested.



V.6 WRP, RDP & DATA

These three pins function the same as pins of the same name in previous *PowerSpeech*ä synthesizers designed to communicate with external serial memory devices, such as OTPs, SRAMs, and Flash EPROMs. They provide "what you see is what you get" emulation.

V.7 /DISOTP

This pin ensures downward compatibility with the W5280 family. It is used to disable the serial interface pins of the W583xxx, WRP, RDP, and DATA, in order to program an OTP or Flash EPROM without disconnecting the interface pins in advance. This is a useful convenience feature. /DISOTP is pulled high internally.

V.8 /RESET

Active low reset input with an internal pull-high resistance of 500 KΩ. The falling edge of the /RESET pin will reset the W583xxx totally, just like the POR condition. Right at the rising edge of the /RESET input, the W583xxx starts to awake and continues to undergo the POI process.

Originally, the /RESET pin is used to function as a last resort to rescue the POR issue, which is encountered in some occasions where the internal POR circuit of the W583xxx cannot operate properly. If customers failed to discharge the VDD to ground level and re-power up the W583xxx, it may function abnormally, causing unpredictable operations. Users may then reset the W583xxx by sending a pulse through the /RESET pin to re-start the operation from the very beginning: POI. Maybe, this is the safest way to get around all the annoying POR issues.

V.9 VDD

Positive power supply. In order to prevent possible power noises generated during motor driving from interfering the proper operations of the internal POR circuit, which is essential to the POI (Power On Initialization) process of the *PowerSpeech*ä synthesizers, two approaches are being adopted in the W583xxx: one is to use /RESET pin, which is described in detail elsewhere, to fully reset the internal circuits for a brand new start; the other is to place VDD and VSS apart as far as possible to reduce the possibility of noise induction.

In order for the W583xxx to process the POI correctly, the VDD has to drop low enough and rise quite quickly to initiate the internal POR circuit for generating the required pulse.

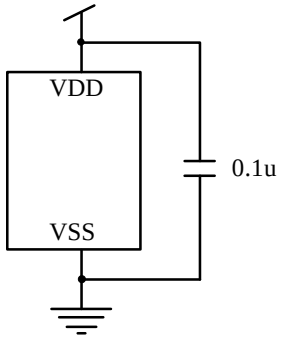
Special care goes to the discharge of VDD to nearly ground level to ensure proper operations.

V.10 VDDE

VDDE is the power of external memory which might be higher than VDD. For example W58300 operates at VDD=2.5V but external memory devices work at VDDE=4.5V.

V.11 VSS

Negative power supply. In order to let W583xxx work properly, it is necessary to add 0.1µF capacitor between VDD(VDD and VDD1 in W583xxx) and VSS.



VI. FUNCTIONAL DESCRIPTION

The W583xxx is a derivative of Winbond's *PowerSpeech*ä synthesizers, which are becoming dominant in the consumer market, especially for toy applications.

There are 8 trigger inputs and 8 STOP outputs. The maximal software key pad number by scanning matrix is up to 8*9=72 keys. There are 8 general purpose registers, R0-R7. R0-R7 can apply not only for "LD" and "JP" instructions but also for "MV" instruction. Only R0 can apply for "INC" instruction. CPU interface is the same as the W581xx series. IR interface is a new feature in *PowerSpeech*ä . You can use IR interface to transmit and receive a command. For example, when X chip executes the "TX R1" instruction, the Pulse Position Modulation waveform (with 38 KHz carrier) outputs from IROUT pin to drive a photo diode. Y chips within a certain distance will receive the IR signal through an IR receiver module to TG3 pin and execute a "JP" instruction to the interrupt vector/label pointed by R1 of X chip.

There are two kinds of events that can cause the W583xxx to enter the POI (Power On Initialization) process: one is power on, and the other is direct trigger from /RESET pin. The interrupt vector 32 is allocated for this special event, and its priority is above all, that is, no triggers can override the POI process if they all happen simultaneously. During the POI process, triggers can then override it successfully, provided the EN0, EN1 and MODE0, MODE1 registers are set properly.

If more than two events happen simultaneously, the priority that is set by the internal H/W is: POI > TG1F > TG1R > TG2F > TG2R > TG3F > TG3R > TG4F > TG4R > TG5F > TG5R > TG6F > TG6R > TG7F > TG7R > TG8F > TG8R > "JP" instruction.

VI.1 POWER ON INITIALIZATION

As usual in previous *PowerSpeech*ä synthesizers, the W583xxx automatically executes the POI(Power On

Initialization) process upon power up or the depression of /RESET pin. The interrupt vector dedicated for POI is allocated at "32" just the same as W527x/W528x series.

Upon power up, the W583xxx resets itself to initial values by generating a POR(Power On Reset) pulse internally. To start the POI process, the W583xxx follows almost the same procedures of a trigger, except for the longer power on debounce time about 160mS.

During POI process, certain triggers can override to take over if the EN0 or EN1 register is set to enable those triggers properly. Take the following example, after MODE0 and MODE1 registers are set to their appropriate values according to customers' configuration, the EN0 register is set to enable the falling-edge triggers of TG1 and TG2.

Therefore, during the reproduction of voice sections, like Voice1, Voice2, Voice3, and Voice4, triggers TG1F and TG2F may terminate the normal operation of POI process and start a new trigger later on.

```
W583M02
        FREQ2
        LED1
        VOUT_PWM
POI:
        LD MODE0, 0x03
        LD MODE1, 0xF2
        LD EN0, 0x03
        LD STOP, 0xC5
        Voice1 + 2*Voice2 + 8*Voice3
        JP EXIT @TG3_LOW
        Voice4
EXIT:
        END
```

To prevent the hang-up problem, there is another way that can cause W583xxx to enter power on initialization. Once all the trigger pins are disabled (EN0 and EN1 are loaded with "0"s) before "END" instruction being executed, the W583xxx will start the POI process.

The default settings of all W583xxx registers upon power on are given in "Register Definition and Control" section.

VI.2 INTERRUPT VECTOR ALLOCATION

The W583xxx provides a total of 8 trigger inputs to interface with the outside world directly. After being debounced, the W583xxx responds to each edge of a valid trigger with a interrupt vector, provided that the associated enable flag of that particular edge is set previously. The triggered input then starts to execute the interrupt vector by overwriting current operations, if any. The debounce time of trigger input is around 20-40mS or 160µs-320µs dependent on MODE0.4.

For direct trigger inputs, there are 16 interrupt vectors allocated for eight TG pins: interrupt vectors 0, 1, 2, 3, 8, 9, 10 and 11 are for falling edge triggers, while interrupt vectors 4, 5, 6, 7, 12, 13, 14 and 15 are used for the rising edge triggers.

Note that even the page mode configuration is the mode more than one page, those trigger sources listed in the following table always force the chip to jump to the interrupt vectors in Page 0. If the trigger source is from TG input, the PAGE register is not changed although the chip jumps to the interrupt vectors in Page 0. If the trigger source is POI, PAGE register is reset.

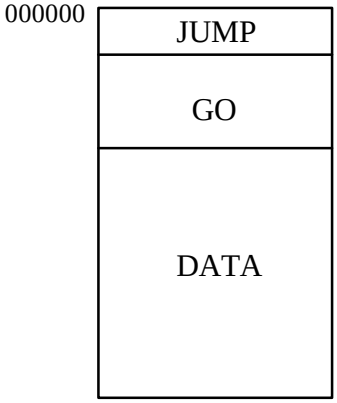
Interrupt Vector	Trigger Source	Interrupt Vector	Trigger Source
0	TG1F	8	TG5F
1	TG2F	9	TG6F
2	TG3F	10	TG7F
3	TG4F	11	TG8F
4	TG1R	12	TG5R
5	TG2R	13	TG6R
6	TG3R	14	TG7R
7	TG4R	15	TG8R
32	POI	-	-

VI.3 NEW SPEECH SYNTHESIZER

The speech synthesizer used for the W583xxx is a new algorithm for *PowerSpeech*ä to enhance the sound quality. This kind of new algorithm is a frame based algorithm. The quantization width is encoded by frame rather than by sample like ADPCM.

VI.4 ROM ORGANIZATION

The ROM can be partitioned into three parts, JUMP, GO, and DATA as depicted below



The JUMP region is for the interrupt vector/label. Each JUMP instruction occupies 32 bits which only 20 bits are used. Four of the 20 bits in JUMP instruction are used for global repeat. Thus, a maximum of 16 global play time can be achieved. Combined with the PAGE register, the number of interrupt vector/label can up to 2048.

The GO region includes the instruction or information of voice data, miscellaneous control bits. Each GO instruction also occupies 32 bits. The GO can be located on the memory up to 1M bits (including JUMP region). That is, the maximum address of GO can up to 1M bits while the JUMPs have used the lower address region. The DATA region saves the voice data which are used by the GO.

VI.5 SECTION CONTROL

The section control information are hidden in GO instruction. For detail usage, please refer to "Program Example" section.

VI.5.1 VARIABLE FREQUENCY CONTROL

The Fosc can be divided proportionally to get a corresponding sample rate of 4.8/6/8/12 KHz for the reproduction of

compressed voice data.

Declaration	Sample Rate(KHz)
FREQ0	4.8
FREQ1	6
FREQ2	8
FREQ3	12

VI.5.2 LED CONTROL

Customers may use the LED0/LED1 declaration to control the LEDs.

Declaration	LED ON/OFF
LED0	OFF
LED1	ON

VI.6 REGISTER DEFINITION AND CONTROL

The register file of the W583xxx is composed of 14 registers, including 8 general purpose registers and 6 special purpose registers. They are defined to facilitate the operations for various purposes. The default setting values of the registers are given in the following table.

Register	Name	Default Setting
General Register	R0-R7	00100000B
Special Register	EN0, EN1	11111111B
	MODE0, MODE1	11111111B
	STOP	11111111B
	PAGE	00000000B

VI.6.1 MODE0 Register

Bit	Description	Definition	Register Control Declaration
7	LED mode	1: Flash	-
		0: DC	-
6	LED2/STPC pin selection	1: LED2 output	-
		0: STPC output	-
5	IR output	1: Hardware control IR output	-
		0: STPC control IR output	-
4	Debounce time	1: Long	-
		0: Short	-
3, 1,0	Reserved		-
2	STPA/BUSY pin selection	1: STPA output	STPA
		0: BUSY output	BUSY

MODE0.7 controls the output type of LED1 (and LED2) pin. MODE0.6 controls the configuration of LED2/STPC pin. MODE0.5 controls the output source of IR. If hardware control IR output is selected, IR output can have signal with carrier or without carrier which is selected by MODE1.0. MODE0.4 controls the trigger pin debounce time. MODE0.2 controls the behavior of the STPA/BUSY pin which is usually used as Busy signal in CPU mode.

VI.6.2 MODE1 Register

Bit	Description	Definition	Register Control Declaration
7, 6, 1	Reserved		-
5	LED Flash type	1: Alternate	LED_ASYN
		0: Synchronous	LED_SYN
4	LED1 section control	1: YES	LED1_S_CTL
		0: NO	LED1_S_OFF
3	LED2 control	1: SECTION control	LED2_S_CTL
		0: STPC control	LED2_STC_CTL
2	LED1 volume control	1: OFF	LED_VOL_OFF
		0: ON	LED_VOL_ON
0	IR output format	1: IR output carrier with duty cycle 75%	-
		0: IR output without carrier	-

MODE1.5 is for LED flash type control. MODE1.4 is for LED1 section control ON/OFF. MODE1.3 is for LED2 Section/STPC control. MODE1.2 is for LED1 volume control. MODE1.0 is for IR output with or without carrier and this bit is useful only MODE0.5 is "1". For STPC control IR output (MODE0.5 is 0), the IR output always has 38 KHz carrier signal no matter what the setting of MODE1.0 is.

VI.6.3 PAGE Register

Bit	7	6	5	4	3	2	1	0
PAGE	-	-	-	PG4	PG3	PG2	PG1	PG0

Bits 5-7 of PAGE register are reserved, bits 0-4 are used for page selection. The user must setup the page mode configuration described in the Option Control Function section. Once the page mode is decided, the working page is selected by the bits 0-4 of PAGE register. Hence, the user can execute "LD PAGE, value" instruction to change the working page of the interrupt vector/label. Not all of the bits 0-4 of PAGE register are used in different page modes; they are listed below.

Page Mode	PG4	PG3	PG2	PG1	PG0
1-page	×	×	×	×	×
8-page	×	×	√	√	√
16-page	×	√	√	√	√
32-page	√	√	√	√	√

Where "×" means don't care and "√" means must be set properly.

Note that if PAGE register is changed by instruction in a global repeat loop, the global repeat will not be completely finished because the chip will jump to the page selected by PAGE register.

VI.6.4 EN0, EN1 Registers

Bit	7	6	5	4	3	2	1	0
EN0	TG4R	TG3R	TG2R	TG1R	TG4F	TG3F	TG2F	TG1F
EN1	TG8R	TG7R	TG6R	TG5R	TG8F	TG7F	TG6F	TG5F

A "1" means "enabled", while a "0" means "disabled" for that edge of the particular TG pin. For example, the instruction "LD EN0, 0x0F" enables all the falling edge triggers of TG1-TG4, while disabling all the rising edge triggers of TG1-TG4. The user can modify the EN0 and EN1 registers during operation of the W583xxx to achieve various kinds of trigger functions, like retriggerable or not, one shot or level hold play mode, etc.

That is to say, users can change the contents of EN0, EN1 register during synthesis at will to determine which trigger pin is to be enabled or disabled for its falling/rising edge.

VI.6.5 STOP Register

Bit	7	6	5	4	3	2	1	0
STOP	STH	STG	STF	STE	STD	STC	STB	STA

The STOP register is used to control the status of the STPA-STPH pins. For example STB bit, the corresponding bit 1, of the STOP register is used to drive the output buffer of STPB pin, an inverted stage, to show its logic status.

VI.6.6 R0-R7 Registers

These eight registers function as general purpose registers. They can be used to hold the interrupt vector/label. R0 is a special register which can be incremented by "INC" instruction.

VI.7 OPTION CONTROL FUNCTION

There are four types of option that can be determined by a declaration in the user's program file, but can not be controlled by register.

Function	Option Control Declaration	Definition
Page mode configuration	DEFPAGE 1	256 labels for 1 page, 1 page in total (1-page mode)
	DEFPAGE 8	256 labels for 1 page, 8 pages in total (8-page mode)
	DEFPAGE 16	128 labels for 1 page, 16 pages in total(16-page mode)
	DEFPAGE 32	64 labels for 1 page, 32 pages in total (32-page mode)
Operation mode	NORMAL	Normal mode operation
	CPU	CPU mode operation
Oscillator frequency	OSC_3MHZ	3 MHz oscillator
	OSC_1.5MHZ	1.5 MHz oscillator
Voice output type	VOUT_DAC	DAC (AUD) output
	VOUT_PWM	PWM output

"DEFPAGE" decides the page operation mode of W583xxx. The default setting of the page mode is 1-page mode. The 8-page, 16-page or 32-page mode must be declared in order to reach the interrupt vectors/labels from 257 to 2048 when the interrupt vector/label is larger than 256.

The W583xxx can communicate with an external microprocessor through the simple serial CPU interface, which is the same as the W581xx series. The CPU interface consists of the TG1, TG2, and STPA/BUSY pins. "NORMAL" and "CPU" decide whether the operation mode of W583xxx will be normal mode or CPU mode.

"OSC_3MHZ" and "OSC_1.5MHZ" select the frequency of the system clock. "VOUT_DAC" and "VOUT_PWM" select the voice output type. For DAC voice output, "OSC_1.5MHZ" option is suggested to have lower frequency deviation.

VI.8 SYMBOLIC COMPILER

In order to alleviate the burden of the *.out programming load for the W583xxx, the compiler has been designed to be a symbolic compiler, which accepts not only the commonly used interrupt vector/label numbers, but also the symbolic labels that are adopted in almost any commercial μC compilers. Some unique features of the symbolic compiler are listed below:

(1) Directives provided for various purposes:

Define option control, DEFPAGE 1/8/16/32, NORMAL/CPU, OSC_3MHZ/OSC_1.5MHZ, VOUT_DAC/VOUT_PWM.

Define section control, LED0/LED1, FREQ0/FREQ1/FREQ2/FREQ3.

Define register control, LED_ASYN/LED_SYN, LED1_S_CTL/LED1_S_OFF, LED2_S_CTL/LED2_STC_CTL, LED_VOL_OFF/LED_VOL_ON, STPA/BUSY.

(2) Symbolic interrupt vector and label.

VI.9 PWM OUTPUT

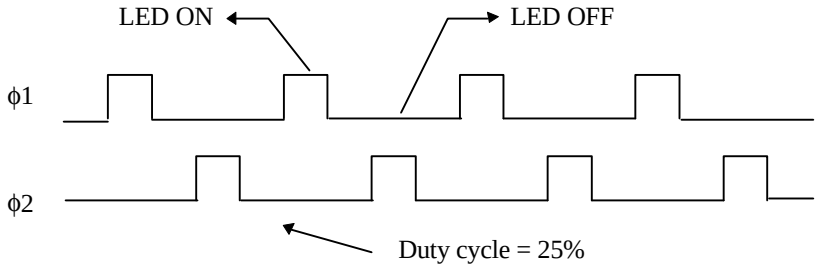
If we select the voice output as PWM type (by Option Control) , the output of AUD/SPK+ and SPK- is a hardware generated PWM (Pulse Width Modulation) waveform. The initial PCM value is 80H. We do not need any head or tail in PWM output mode to connect voice. In AUD(DAC) output mode, we do need head and tail to prevent AUD output abrupt change. The power consumption of PWM output is far less than AUD output.

VI.10 LED OPERATION

The LED1 pin can flashes with 3Hz flash or DC output. The LEDs can also be section-controlled by each GO instruction. In addition to LED1 pin, LED2/STPC pin can also be programmed as LED2 output.

VI.10.1 Flash with 3Hz

The 3Hz clock is phase divided into two LED sources, which are 180° out of phase, in order to facilitate the synchronous/alternate features.



The ϕ1 clock is applied to LED1 output pin definitely. For flashing synchronously of the LEDs, the ϕ1 clock is also connected to LED2. For flashing alternately, the ϕ2 clock is connected to LED2. In other words, LED outputs flash synchronously with the ϕ1 clock or flash alternately in two groups, one is LED1 with ϕ1 and the other is LED2 with ϕ2.

VI.11 SAMPLE RATE

The sample rate for voice reproductions can be determined by two methods: one is to vary the external resistor ROSC, the other is to change the control bits for variable frequency effects. The former method is to adjust the master frequency of the whole chip, while the latter is to divide the master frequency by different divisors to get the 4.8/6/8/12 KHz sample rate under the typical condition of Fosc = 1.5 MHz or 3 MHz.

Normally, customers have to reproduce the voices at the same sample rate as recordings' in order to get the original voice outputs. The maximum sample rate allowed for the W583xxx is 12 KHz.

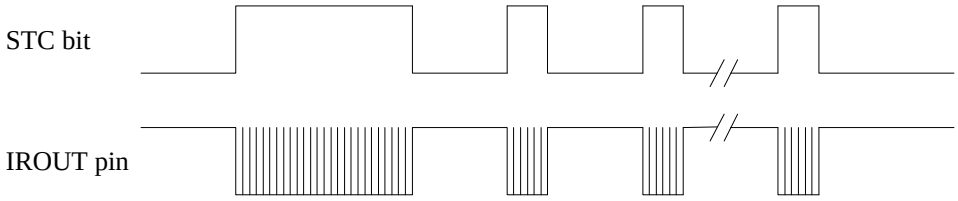
During developing phases of application codes, customers may use Winbond's speech download board or W55F05, W55F20 to evaluate the functions and voice quality. Be aware that the sample rate could not be set above 12 KHz, which is the maximum limitation of the W583xxx, even though it can work normally. This is because there is a fundamental difference of ROM structure between evaluation tools and real chips.

VI.12 IR INTERFACE

There are 2 kinds of IR interface provided in W583xxx. They are selected by bit MODE0.5.

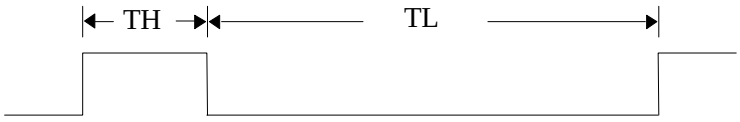
The first one is hardware IR interface which transmits an equivalent "JP Rn" instruction to the receiver by "TX Rn" instruction and hardware through IROUT pin. The receiver hardware will receive the signal through TG3/IRIN pin and generate an JUMP signal and then jump to the interrupt vector/label directed by the transmitter. For example, there are two W583xxxs called X and Y chip. Suppose that the data within R1 register of X chip are 100. When X chip executes "TX R1" instruction, a particular signal will output from IROUT pin to drive an IR transmitter. An IR receiver module is placed in front of the transmitter will receive the IR signal and output a filtered signal to TG3/IRIN pin of Y chip. After receiving signal, Y chip will jump to label 100 of the specific page corresponding to the setting of PAGE register. The major mission of IR interface is to transmit and receive COMMAND rather than DATA.

The second IR interface is achieved by software programming. By programming STC bit, IROUT pin will have the signal with 38 KHz carrier. The IROUT pin will output a signal with 38 KHz frequency and 75% duty cycle if STC bit is set. If STC bit is cleared, IROUT pin will keep in high. Users have to program the receiver by themselves. The relation between STC bit and IROUT are shown below.



VI.12.1 H/W IR Protocol

The output protocol of hardware defined IR begins with a Start bit followed by 9 Data bits(1 data byte, MSB first, and 1 parity bit), and Stop bit. The Start bit is typically composed of 1mS High(TH) and 6.5mS Low(TL). Data bit '1' is composed of 1mS High and 4mS Low. Data bit '0' and Stop bit are composed of 1mS High and 2mS Low. It's called pulse position modulation. The IROUT pin will keep high in TH duration and output 38 KHz carrier with 75% duty cycle in TL duration. Receiver module will recover the original waveform by filtering the 38 KHz carrier out.

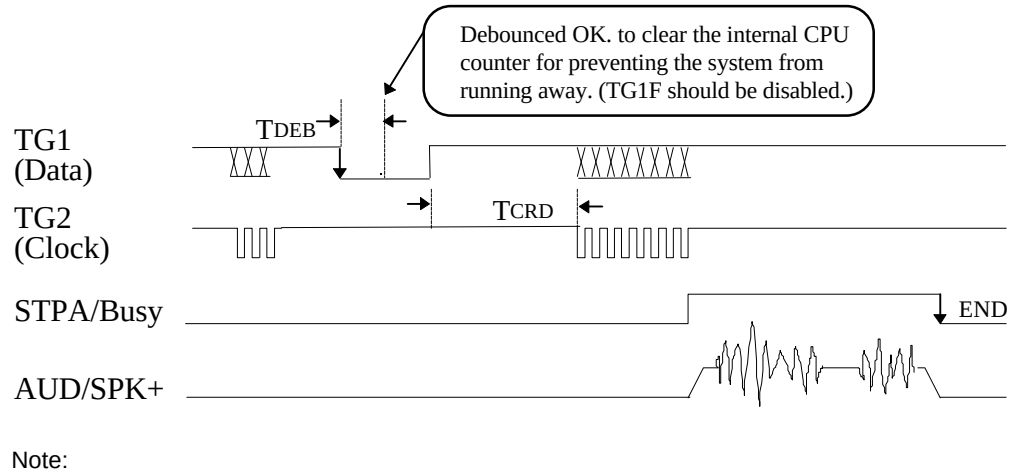


Parameter	Description	Min.	Typ.	Max.	Unit
TD0	Data "0" period		3000		µS
THD0	Data "0" high time	800	1000	1200	µS
TLD0	Data "0" low time	1600	2000	2400	µS
TD1	Data "1" period		5000		µS
THD1	Data "1" high time	800	1000	1200	µS
TLD1	Data "1" low time	3200	4000	4800	µS
TSTR	Start bit period		7500		µS
THSTR	Start bit high time	800	1000	1200	µS
TLSTR	Start bit low time	5200	6500		µS

VI.13 CPU INTERFACE

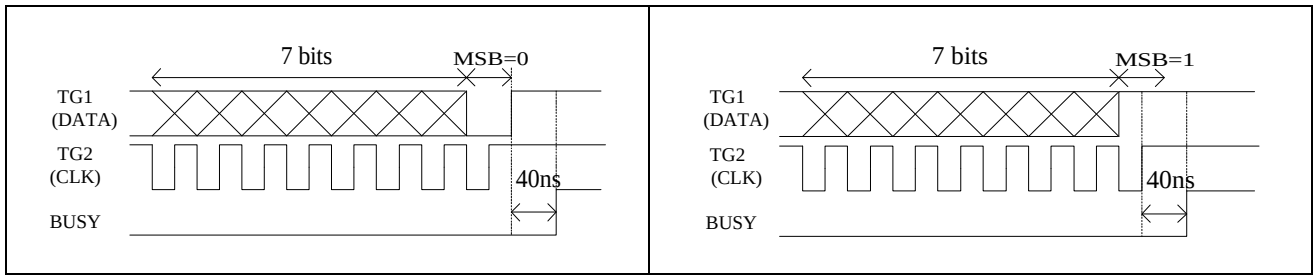
The W583xxx can communicate with an external microprocessor through a simple serial CPU interface. This

function is similar to the W581xx series. The W583xxx CPU interface consists of TG1, TG2 and STPA/BUSY pins, which are shown below:



Note:
1. TDEB means the "Debounce time".
2. TCRD is the "CPU Reset Delay" time. This should be more than 2.6 µS.
3. The "Clock" frequency of the TG2 pin can be set in the range: 10 KHz - 1 MHz.

Busy signal will output "high" after the end of transmission. The rising timing of Busy signal is dependent on the MSB of data output on TG1(Data) pin. If MSB is "1", Busy will rise after the last rising edge of TG2(Clock) pin. If MSB is "0", Busy will rise after the rising edge that TG1(Data) returns to high.



To place the W583xxx in CPU mode, program the code according to the following example.

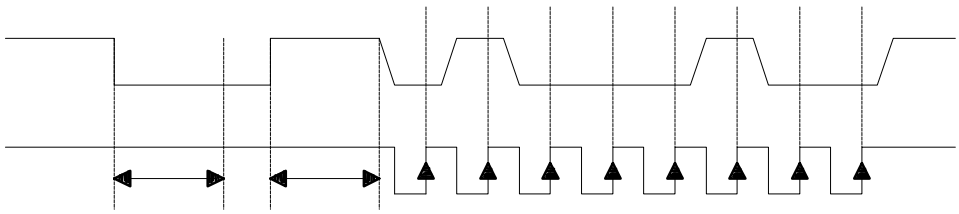
```
W583M02
CPU                    ; Reserved word, used as a directive to notify the compiler for post processing.
LED1
FREQ2

POI:
    LD EN0, 0x00
    H5+voice1+T5
```

```
        END
34:                             ; Direct trigger or CPU interrupt.
        H5+voice2+T5
        END
```

The default operating mode of the W583xxx is normal, or manual trigger mode, which is identified by the "Normal" and "CPU" option control. To enter the CPU mode, the "CPU" declaration must be inserted in the declaration region of program (*.out). In CPU mode, bit MODE0.2, which is defined as STPA or BUSY selection for the STPA/BUSY pin, will be selected as "0" (BUSY output) automatically by the compiler unless otherwise specified explicitly by the STPA directive. The CPU, STPA, and BUSY directives can appear only in the first paragraph of the *.out files so that the compiler will automatically interpret them as Stop definitions in the POI interrupt vector. If these directives are placed elsewhere, an error message will be issued during the compilation process.

In the program example shown above, the external µC will transfer one byte data "34" to W583xxx. The number 34 (Decimal) is equal to 00100010b (Binary). The interface timing is shown below.



<1> When TG1 is pulled low, the W583xxx stops playing voice or executing instruction and waits for data from the external µC.
<2> If TG1 is debounced OK, the W583xxx will clear the CPU receiving buffer.
<3> 8-bit data are transferred by TG1 (Data) and TG2 (Clock). LSB is sent firstly.
<4> TG1 returns to high and starts the CPU interrupt service. In this case W583M02 will play the H51+voice2+T51 sections and the STPA/BUSY pin is pulled high during the playing period.

The STPA/BUSY pin is normally set as the STPA output in normal mode after power up or the /RESET pin is triggered, if the MODE0.2 bit is not altered or no "BUSY" declaration is invoked in the *.out files. In CPU mode, the STPA/BUSY pin usually functions as a handshaking signal, called BUSY, that is used to check the busy status. However, in CPU mode the STPA/BUSY pin can also be configured as an STPA output. Moreover, in normal mode this pin can also be configured as a BUSY signal. So customers should consider carefully what type of output signal is desired from the STPA/BUSY pin.

The BUSY signal goes to high, indicating the W583xxx is busy, after eight consecutive clocks have been successfully transmitted from the external µC and TG1 has returned to high. It returns to low state after an END instruction is encountered, provided there are no more global repeats. See the timing diagrams for further details. In normal mode, the BUSY signal also goes to high after a trigger is debounced successfully and stays high until the W583xxx returns to the standby state. Normal mode and CPU mode may both be used in the same application, if necessary.

The TG1 pin, which is pulled high with a 500KΩ resistor, should be kept high during non-transmission periods to reduce power consumption. The external µC should be connected to the W583xxx by an inverted-type output port for better noise immunity. In CPU mode, the W583xxx stops operating upon the falling edge of the TG1 pin. For the CPU interface to work normally, TG1F should be disabled. So, one suggestion is that TG1F, TG1R, TG2F, and

TG2R should all be disabled in CPU mode.

The master frequency of the external µC, and hence the clock rate of TG1 and TG2, tends to vary among different vendors and applications.

VI.14 SERIAL INTERFACE

The W58300 is connected with external memory devices (serial SRAMs or Flash EPROMs) through the same serial interface used in previous *PowerSpeech*ä products, via the WRP, RDP, and DATA pins.

For evaluation purpose, the ROM file can be stored in any of the serial memory devices mentioned above for "what you hear is what you get," results without mask tooling procedures involving substantial NRE (non-recurring engineering) charges. After a successful evaluation in Winbond's coding environment, customers can request volume production.

The WRP pin is used to send out addresses between shift registers, which are located in the W583xxx and the external memory devices, to access program instructions and speech data, while the RDP pin is used to read data back from the addressed memory space. The DATA pin is thus bidirectional: it serves as an input pin during read operation and an output pin during address writing.

The clock rate of the WRP and RDP pins used for the serial interface is 384 KHz @SR = 6 KHz, provided the oscillation frequency is 3 MHz. For other oscillation frequencies produced by adjusting ROSC, the clock rate changes proportionally.

VII. INSTRUCTION SET

There are two types of instruction in the W583xxx family, unconditional and conditional instructions. The first type of instructions are executed immediately after they are issued. The second type of instructions are executed only when the conditions specified in the instruction are satisfied. All the instructions are listed in the following table.

The cycle time required for instruction execution is reduced greatly to speed up the W583xxx. Normally, under the condition of SR(sample rate) = 6 KHz, the cycle time is no greater than 400µs.

Unconditional		Conditional		
JP	G	JP	G	@STS
JP	Rn	JP	Rn	@STS
LD	ENi, value	LD	ENi, value	@STS
LD	MODEi, value	LD	MODEi, value	@STS
LD	STOP, value	LD	STOP, value	@STS
LD	PAGE, value	LD	PAGE, value	@STS
LD	Rn, value	LD	Rn, value	@STS
END		END		@STS
MV	Rn, Rm	MV	Rn, Rm	@STS
INC		INC		@STS
TX	Rn	TX	Rn	@STS

Legend: G: Interrupt vector/label, 8-bit constant data
Rn: R0-R7
Rm: R0-R7
Eni: EN0, EN1
MODEi: MODE0, MODE1
value: 8-bit data
@STS can be the following: @TGn_HIGH for n=1-8, @TGn_LOW for n=1-8, @LAST.

VII.1 JP

VII.1.1 JP G

Instruct the device to jump directly to the interrupt vector/label corresponding to the constant value G indicated. The value of interrupt vector/label may range from 0 to 255. If the page mode configuration is 16 or 32 page mode, the value of interrupt vector/label may only range from 0 to 127 or 0 to 63.

VII.1.2 JP Rn

Instruct the device to jump to whatever interrupt vector/label indicated by the value currently stored in register Rn. If the page mode configuration is 16 or 32 page mode, one MSB or two MSBs of Rn will be ignored while "JP Rn" is executed.

VII.2 LD

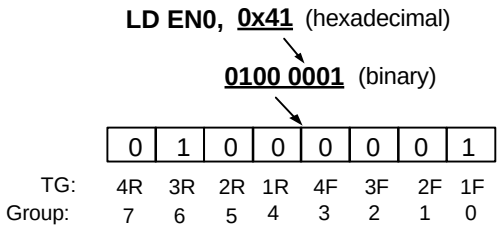
VII.2.1 LD Rn, value

Load one 8-bit data into the register Rn where n can be 0-7.

VII.2.2 LD ENi, value

Load one 8-bit data into the register ENi, where "i" can be 0 or 1. This instruction is used to define the trigger interrupt settings by loading the operand message into register ENi.

Example :



(a). When the rising edge of TG3 (3R) is activated, the EN0 register will cause TG3 to interrupt the current playing state and jump immediately to interrupt vector 6, the interrupt vector that corresponds to 3R.

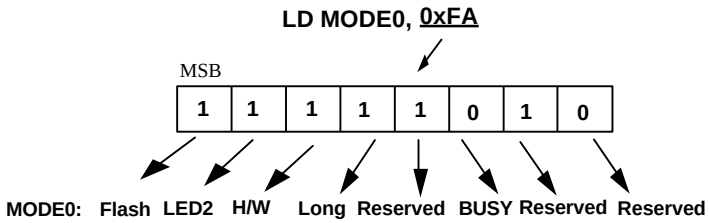
(b). When the falling edge of TG1 (1F) goes active, the EN0 register will cause TG1 to interrupt the current playing state and jump immediately to interrupt vector 0, the interrupt vector that corresponds to 1F.

(c). No action will be taken when the other trigger pins are pressed, because the corresponding bits are set to "0"s.

VII.2.3 LD MODEi, value

Load one 8-bit data into the register MODEi, where "i" can be 0 or 1. This instruction is used to define operation configuration among various operating modes.

Example :



(a). The LED is set as a flash type, with the flash frequency 3 Hz.

(b). LED2/STPC pin is configured as the LED2 output.

(c). The IR output is hareware controlled.

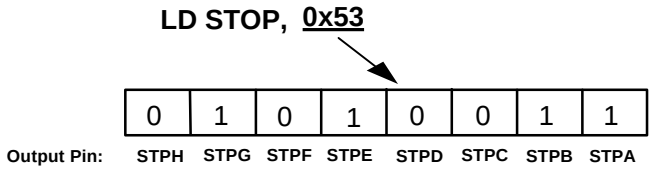
(d). Select the long debounce time.

(e). STPA/BUSY pin is configured as BUSY output.

VII.2.4 LD STOP, value

Load one 8-bit data into the register STOP. This instruction is used to set the output levels of the Stop output. When a particular bit of STOP register is set to "0," the corresponding Stop output will be an active low output.

Example :



(a). The STPA, STPB, STPE, and STPG output pins will be high.

(b). The STPC, STPD, STPF, and STPH output pins will be low.

VII.2.5 LD PAGE, value

Load one 8-bit data into the register PAGE. Although the *"value*" is an 8-bit data, its range is dependent on the page mode configuration of the declaration in user's program file (*.out). For example, if the declaration is "DEFPAGE 16," the page mode is 16-page mode, the *"value*" to be loaded to PAGE register can only be the range from 0 to 15.

VII.3 MV

MV Rn, Rm : The data in Rm register are copied into Rn register and the data in Rm are unchanged. "m" and "n" can be 0-7, but "m" and "n" cannot be the same.

VII.4 INC

Increase the data in R0 register by one. Note that "INC" instruction can only operate on R0.

VII.5 TX

TX Rn : The data in Rn are transmitted out through IROUT pin by IR interface protocol. In order to let W583xxx be working before the transmission end, the "END" instruction cannot follow the "TX Rn" instruction immediately. Usually one period of silence is added after "TX Rn."

VII.6 END

This instruction instructs the chip to cease all activity immediately. Generally, "END" instruction will stop the oscillator. But, if TG3 is pulled low, "END" instruction will not stop the oscillator. Hence, in order to force W583xxx to enter standby mode, user must release TG3 to "high" before the execution of "END" instruction.

VII.7 @STS

There is a symbol @STS at the end of notation of one conditional instruction. The @STS can be one of the three kinds of conditions.

(a). @LAST: When the last global repeat sound cycle is finished, the instruction execution begins.
(b). @TGn_HIGH: When the n-th trigger pin is keeping at "High" voltage level, the instruction execution begins.
(c). @TGn_LOW: When the n-th trigger pin is keeping at "Low" voltage level, the instruction execution begins.

VIII. PROGRAMMING EXAMPLE

VIII.1 Play Statement

We use play statement to define the combination of playback sound. The following is an example of a play statement format:

```
i:N
H5x+m1*(A_fl+m2*(B_fl+m3*(C_fl+m4*D_fl))+[1FFF0])+...T5x
END
```

(1). " i" defines the interrupt vector/label.

(2). "N" defines the number of global repeats (from 1 to 16).

(3). "m1", "m2" and "m3" define the number of local repeats (from 1 to 8).

(4). "A", "B", "C", and "D" are files containing converted voice data (*.wmd) for W583xxx.

(5). "*_fl*" is the section control setting, and the parameters "*f*" and "*l*" are defined below:

f : Sampling Frequency definition (default value: *f*=1)

f	3	2	1	0
Frequency	12 KHz	8 KHz	6 KHz	4.8 KHz

l : LED Status definition (default value: *l*=0)

l	1	0
LED Status	On	Off

Note 1: If the section control setting is not defined, the default values will be used. For example, in the speech equation "H51+A+T51", if the "A" sound is played, the default values are used. These values are 6 KHz sampling frequency (*f*=1), and LED Off (*l*=0).

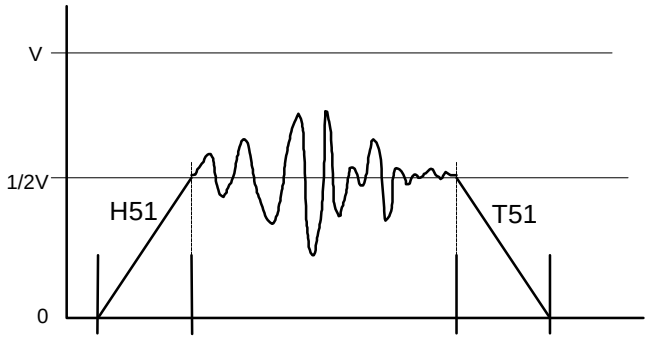
Note 2: If the section control setting is defined, both the "*f*" and "*l*" digits must be defined together.

Example:
1. "H51+A_2+T51": This is a wrong speech equation since only one digit (*f*) of section control is defined.
2. "H51+A_21+T51": This is a correct speech equation with section control. The sampling frequency is 8 KHz (*f*=2), the LED is On (*l*=1).

(6). [1FFF0] is a period of silence of length 1FFF0 (around 5.4 seconds under the 6 KHz sampling frequency condition). The maximum silence length in one "[ ]" is [FFFFF], that is 1M bits, around 43.7 seconds under the 6 KHz sampling frequency condition. Note that the maximum length is different under different sampling frequency condition. Another syntax for silence is to express time duration directly by second or millisecond, like [21.3 sec], [132.5 msec]. Of course the length cannot exceed the maximum silence length. The maximal values in second under different sampling rate are listed below:

Sample Rate	4.8 KHz	6 KHz	8 KHz	12 KHz
Maximal Value	54.61 sec	43.69 sec	32.76 sec	21.84 sec

(7). "H5x" and "T5x", x ranges from 1 to 5, are the Head file and Tail file with the data format for W583xxx. They are inserted only the voice output type is AUD output. **If PWM output is selected (by Option Control Declaration), H5x and T5x are not needed**. These two files can be used to eliminate the popping sound which may occur when the sound starts and stops. The following is a sample waveform:



(8). Flexible combination of unlimited "( )": This feature can be used in writing speech equations. This feature reduces the program editing time but does not save the program memory space.

Example:

eq1: H5x+2*(A+2*(B+2*(C+3*D)))+T5x
eq2: H5x+A+B+C+3*D+C+3*D+B+C+3*D+C+3*D+A+B+C+3*D+C+3*D+B+C+3*D+C+3*D+T5x

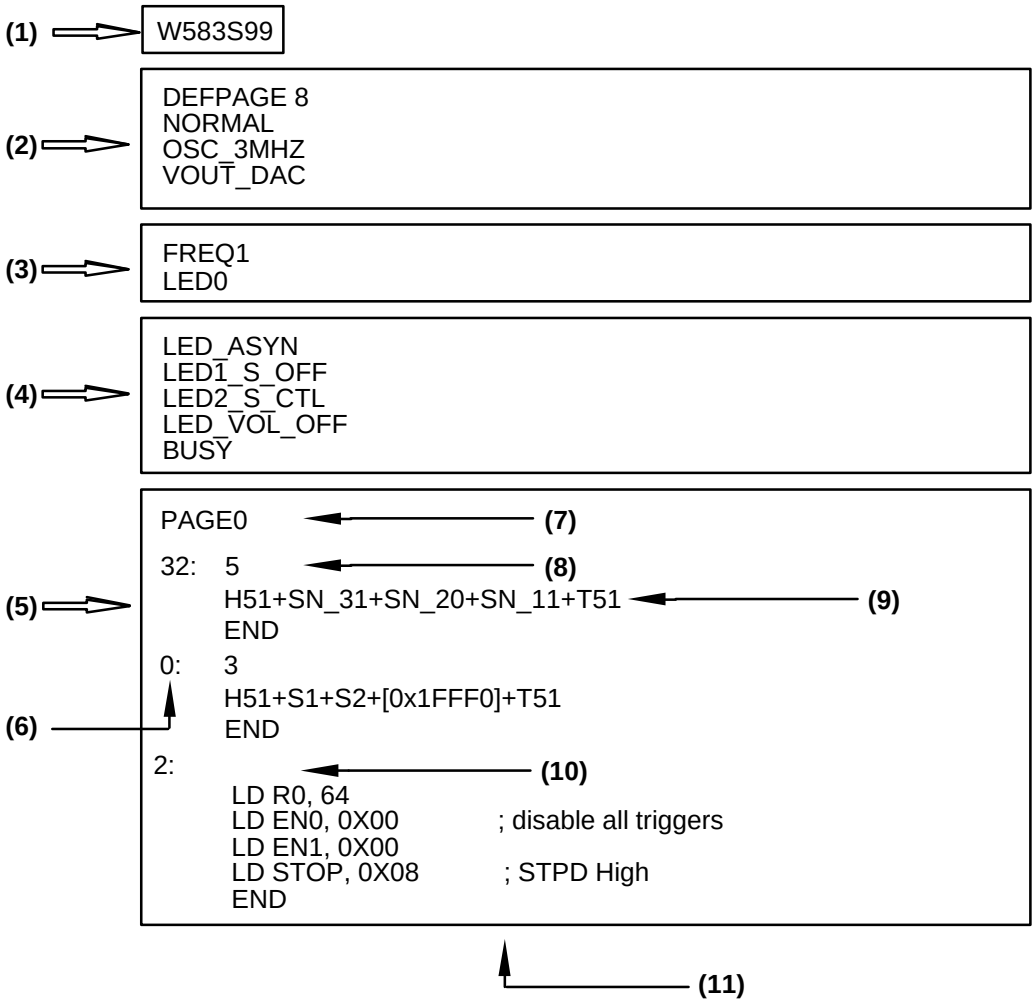
These two speech equations are the same. After being complied, these two speech equations will occupy the same program memory size. Note that eq1 is much easier to write and understand than eq2. There is no limit in the number of "( )". However, each pair of "( )" must be written on the same line.

VIII.2 Programmable Power-on Initialization

Whenever the W583xxx *PowerSpeech*ä is powered on, the programs contained in the interrupt vector 32 will be executed immediately. Programs can therefore be written into this interrupt vector to set the initial power-on state. If the user does not wish to execute any programs at power-on, an "END" instruction should be entered in interrupt vector 32.

VIII.3 *PowerSpeech*ä Program Format

The W583xxx *PowerSpeech*ä has a programming language to define the product functions. An example of the W583xxx *PowerSpeech*ä program format is shown below. Explanatory notes follow the example.



Legend:

(1) **Chip Body**: User must first defines the *PowerSpeech*ä body to be used, or else an error message will appear during compiation. For exmple, W583M02, W58S99, W58S20, etc are allowed .

(2) **Option Control Declaration:** State the option control function in this region. These declarations will decide the the corresponding function in the chip and they cannot be changed in user's program.

Declaration	Option Control Function	Comment
DEFPAGE 1	1-page mode	default
DEFPAGE 8	8-page mode	
DEFPAGE 16	16-page mode	
DEFPAGE 32	32-page mode	
NORMAL	Normal mode	default
CPU	CPU mode	
OSC_3MHZ	3 MHz system clock	default
SOC_1.5MHZ	1.5 MHz system clock	
VOUT_DAC	DAC type voice output	default
VOUT_PWM	PWM type voice output	

(3) **Section Control Declaration:** State the section control in this region. The section control can be changed in the SPEECH equation.

Declaration	Section Control Function	Comment
FREQ0	4.8 KHz sample rate	
FREQ1	6 KHz sample rate	default
FREQ2	8 KHz sample rate	
FREQ3	12 KHz sample rate	
LED0	LED Off	default
LED1	LED On	

(4) **Register Control Declaration:** State the register control in this region. The user can use register control declaration or "LD" instruction to get the wanted setting since MODE0 and MODE1 registers are user programmable. The different between these two methods is that once the user use Register Control Declaration to get the wanted setting, he is not able to change the setting by "LD" instruction in the program.

Declaration	Register Control Function
LED_ASYN	Refer to MODE1 register
LED_SYN	
LED1_S_CTL	
LED1_S_OFF	
LED2_S_CTL	
LED2_STC_CTL	
LED_VOL_OFF	
LED_VOL_ON	
STPA	Refer to MODE0 register
BUSY	

(5) **Program Block**: Application program and speech operations are written in this area, including the following:
Define interrupt vector/label.
Determine the number of global repeats.
Describe speech equations.
Define the register values and instructions.

Note 1: The maximum program memory size that W58300 can reach is 16M bits.

Note 2: Every GO instruction occupies 32 bits, and every interrupt vector/label also occupies 32 bits.

Note 3: The GO instruction can include the following contents:
(a). Any instruction listed in INSTRUCTION SETS section.
(b). Any speech data file(*.wmd) for the speech equation.

For example, in the speech equation: "H51+A+B_21+C+T51", there are a total of 5 GO instructions: H51, A, B_21, C, and T51.

Note 4: The GO instruction does not include the Declarations. One example is listed below.

```
W583S60          ; Body define, 0 GO instruction
FREQ3            ; Declaration, 0 GO instruction
```

```
32:                          ; POI interrupt vector, 32 bits
  LD EN0, 0x0F               ; 32 bits, 1 GO instruction
  LD STOP, 0x10              ; 1 GO instruction
  END                        ; 1 GO instruction
0: 3                         ; interrupt vector, 32 bits.
  LD EN0, 0x00               ; 1 GO instruction
  LD STOP, 0x1F              ; 1 GO instruction
  H51+3*A+B_21+C+[1A000]+T51
                             ; Speech equation, total with 6 GO instructions. Include:
                             ; H51, 3*A, B_21, C, [1A000], and T51.
  LD STOP, 0x10              ; 1 GO instruction
  LD EN0, 0x0F               ; 1 GO instruction
  END                        ; 1 GO instruction
1:                           ; 32 bits
  H51+A+B+C_30+[1A000]+D+E+T51
                             ; 8 GO instructions:  H51, A, B, C_30, [1A000], D, E, and T51
  END                        ; 1 GO instruction
2:                           ; 32 bits
  JP 100 @TG4_LOW            ; 1 GO instruction
  END                        ; 1 GO instruction
100:                         ; 32 bits
  H51+3*(A+2*B)+T51          ; Equal to: H51+A+2*B+A+2*B+A+2*B+T51, total with 8 GO
                             ; instructions.
  END                        ; 1 GO instruction
```

In the program example shown above, there are a total of 34 GO instructions and 101 interrupt vector/label (= 100+1, because the maximum label to be used is 100). The total program memory size (the voice data are not included) for this program is 4,320 bits (34*32+101*32=4,320).

Note 5: To use the 16M bits program memory more efficiently, the following suggestions can be followed:
(a). The labels should be used consecutively and without skipping. For example: 0, 1, 2, 3,...., 99..., is better than 0, 1, 50, 51, ..., 99, ...
(b). If the program includes several interrupt vector/labels, then the interrupt vector/label with the most GO instructions is better to be placed at the end of the program.

(6) **Interrupt Vector/Label**: Define the interrupt vector/label.

Product	interrupt vector/label	TG interrupt vector	Power-on interrupt vector
W583xxx	0-255*	0-15	32

* The PAGE register must be used in order to access the interrupt vector/label that exceeds 255.

The interrupt vector can also be expressed by symbolic label. There are several reserved words for interrupt vectors 0-15 and 32 of Page 0, list them below.

Interrupt Vector	0	1	2	3	4	5	6	7	32
Symbol	TG1F	TG2F	TG3F	TG4F	TG1R	TG2R	TG3R	TG4R	POI
Interrupt Vector	8	9	10	11	12	13	14	15	-

Symbol	TG5F	TG6F	TG7F	TG8F	TG5R	TG6R	TG7R	TG8R	-

(7) **Page Start**: If the page mode configuration is not 1-page mode, the user must insert Page Start (PAGE0, PAGE1, ...) to separate the interrupt vector/label into different pages.

(8) **Global Repeat**: The global repeat number can be the range from 1 to 16. This number must be placed on the same line as the interrupt vector/label.

(9) **Play Statement**: They are used to define the combination of playback sound.

(10) **Blank**: An interrupt vector/label must be followed by one full blank line without any instruction or speech equation except the global repeat.

(11) **Note**: A semicolon (";") is used to distinguish characters that are not part of the program. Characters written to the right of the semicolon are not considered as part of the program.

VIII.4 Virtual Dual Engine

W583xxx is a single engine chip in hardware. It cannot change the output pin during voice playing. Because of the short instruction cycle time of W583xxx, it is possible to insert one instruction into one voice playing period. By means of this skill, W583xxx can achieve the virtual dual engine purpose.

The method is to separate the original voice, called Sound, into several segments of voice properly, called Sound0, Sound1 and Sound2. User can utilize Winbond Speech Coding System to accomplish the separation of voice. Assume DAC voice output is selected, the program for playing of the voice is

```
H51+Sound+T51
```

If we want to change the Stop output between Sound0 and Sound1, and also change the Stop output between Sound1 and Sound2, the program can be the following.

```
H51+Sound0
LD STOP, 0x05
Sound1
LD STOP, 0x0A
Sound2+T51
```

VIII.5 Some Examples

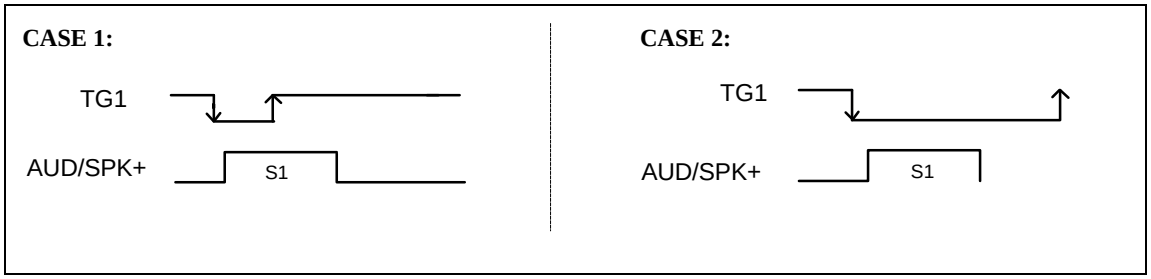
In this section we will present several programming examples for the W583xxx *PowerSpeech*ä chips. The user's programs should be written in ASCII code using a text editor. After being compiled, the sound effects resulting from the programs can be tested by using a Winbond demo board. We choose DAC type voice output in the examples.

VIII.5.1 Four Playing Modes Setting

A. One-Shot Trigger Mode

```
0:                          ; TG1 falling edge interrupt vector
      LD EN0, 0x01          ; Enable TG1 falling edge input only
       H51+Sound1+T51
       END
```

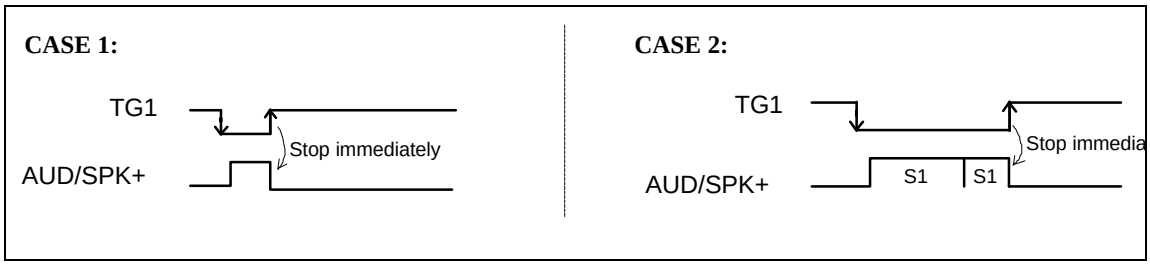
Timing diagram:



B. Level Hold Trigger Mode

```
0:                          ; TG1 falling edge interrupt vector
      LD EN0, 0x11          ; Enable TG1 falling and rising edge input
      H51+Sound1+T51
      JP 0
4:                          ; TG1 rising edge interrupt vector
      END
```

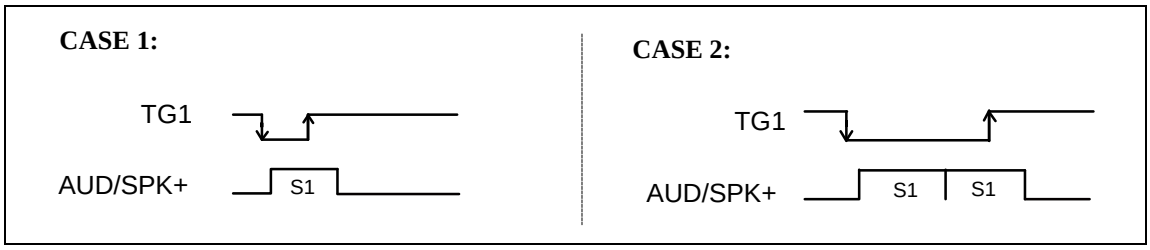
Timing diagram:



C. Completed Cycle Level Hold

```
0:                          ; TG1 falling edge interrupt vector
      LD EN0, 0x01          ; Enable TG1 falling edge input only
      H51+Sound1+T51
      JP 0 @TG1_LOW         ; If TG1 state is low, jump to 0
      END
```

Timing diagram:

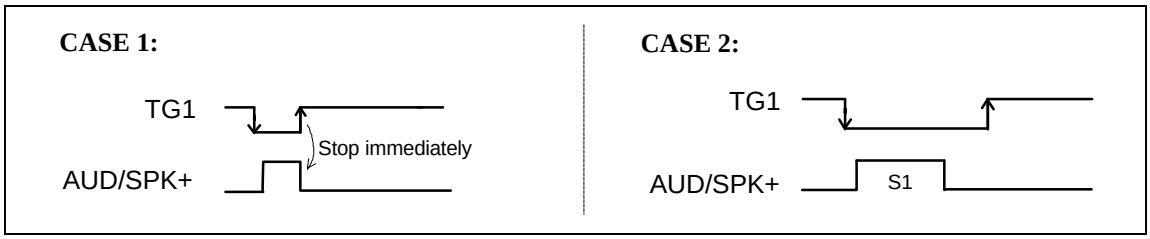


D. Single Cycle Level Hold

```
0:                      ; TG1 falling edge interrupt vector
  LD EN0, 0x11          ; Enable TG1 falling and rising edge input
  H51+Sound1+T51
  END
4:
```

END

Timing diagram:



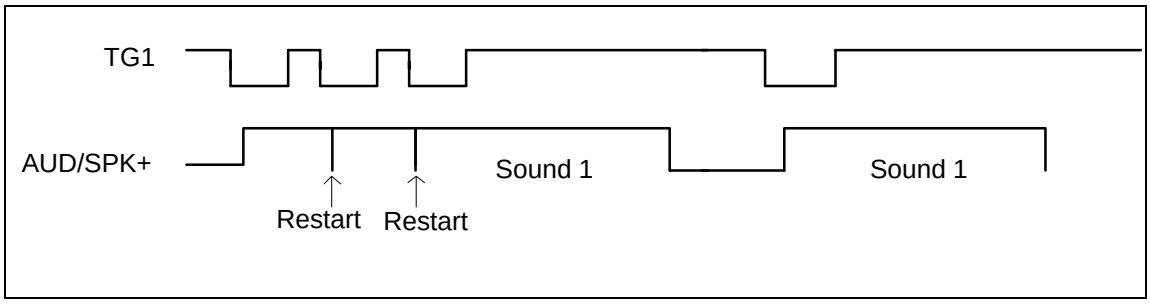
VIII.5.2 Retriggerable And Non-retriggerable Setting

A. Retriggerable

0:

LD EN0, 0x01
:
:
END

Timing diagram:

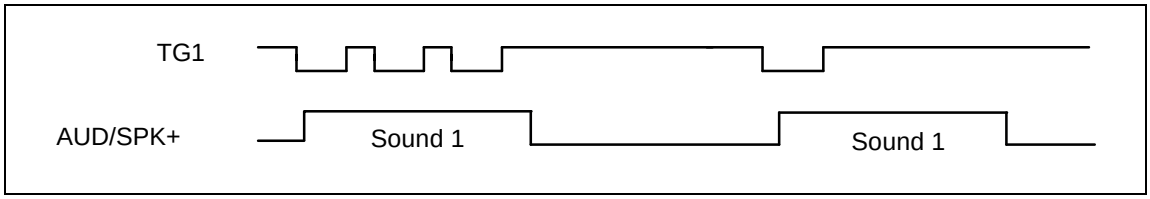


B. Non-Retriggerable

0:

LD EN0, 0x00
:
:
LD EN0, 0x11
END

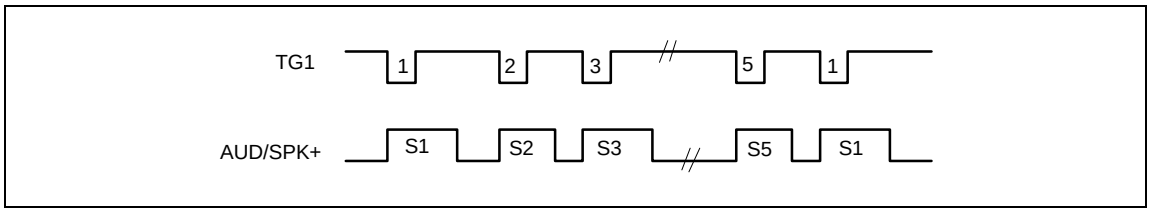
Timing diagram:



VIII.5.3 Serial Playing Mode (5 Segments)

```
W583M02
32:
    LD R0, 16
    LD EN0, 0x01
    END
0:
    JP R0
16:
    INC
    H51+S1+T51
    END
17:
    INC
    H51+S2+T51
    END
18:
    INC
    H51+S3+T51
    END
19:
    INC
    H51+S4+T51
    END
20:
    LD R0, 16
    H51+S5+T51
    END
```

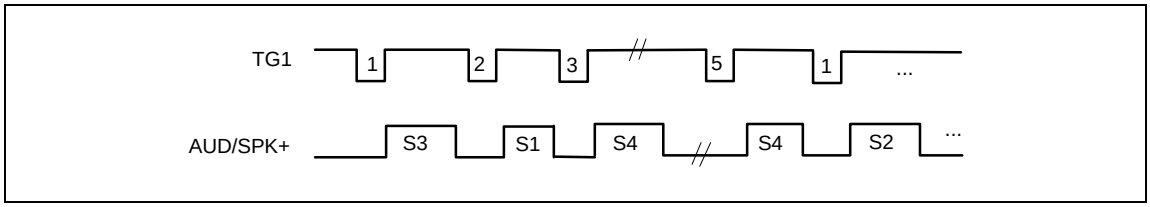
Timing diagram:



VIII.5.4 S/W Random (1)

```
W583S60
32:
    LD EN0, 0x01
    LD R0, 16
    END
0:
    LD EN0, 0x00
    JP R0
16:
    JP 26 @TG1_HIGH
17:
    JP 27 @TG1_HIGH
18:
    JP 28 @TG1_HIGH
19:
    JP 29 @TG1_HIGH
    JP 16
26:
    H51+S1+T51
    LD R0, 17
    JP 31
27:
    H51+S2+T51
    LD R0, 16
    JP 31
28:
    H51+S3+T51
    LD R0, 19
    JP 31
29:
    H51+S4+T51
    LD R0, 18
31:
    LD EN0, 0x01
    END
```

Timing diagram:

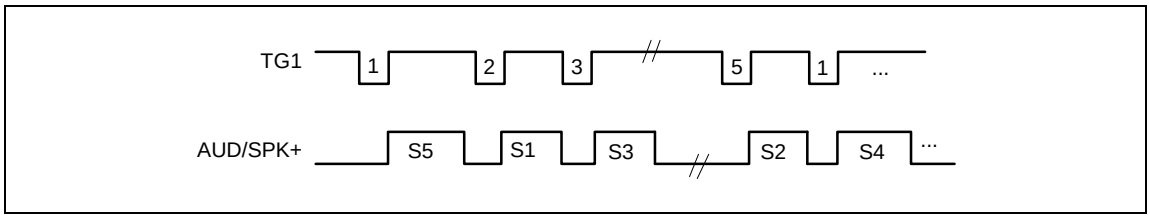


VIII.5.5 S/W Random (2)

```
W583S80
32:
    LD EN0, 0x11
    END
0:
    LD R0, 16
    [300]
    LD R0, 17
    [300]
    LD R0, 18
    [300]
    LD R0, 19
    [300]
    LD R0, 20
    [300]
    JP 0
4:
    JP R0
```

```
16:
    H51+S4+T51
    END
17:
    H51+S1+T51
    END
18:
    H51+S5+T51
    END
19:
    H51+S3+T51
    END
20:
    H51+S2+T51
    END
```

Timing diagram:



VIII.5.6 More Than One PAGE

```
W583S80
DEFPAGE 8                   ; select 8-page mode
OSC_1.5MHZ                  ; change oscillator frequency to 1.5 MHz
FREQ2                       ; sample rate 8 KHz

PAGE0                       ; declare page 0 start
21:                         ; label 21 of page 0
     H51+[3D00]+T51
     END
22:
    LD PAGE, 1              ; change page setting
    JP 21                   ; jump to label 21 in page 1 instead of page 0
```

```
255:
…
…
PAGE1                          ; declare page 1 start
21:                            ; label 21 of page 1
     H51+sound_11+T51
     END
19:
…
…
…
PAGE2                          ; declare page 2 start
…
…
```

VIII.6 APPLICATION EXAMPLES

In this section we will present several special application examples. **The power, 0.1μ capacitor and oscillator circuit are omitted in all of the application circuits.**

VIII.6.1 Power-on Trigger

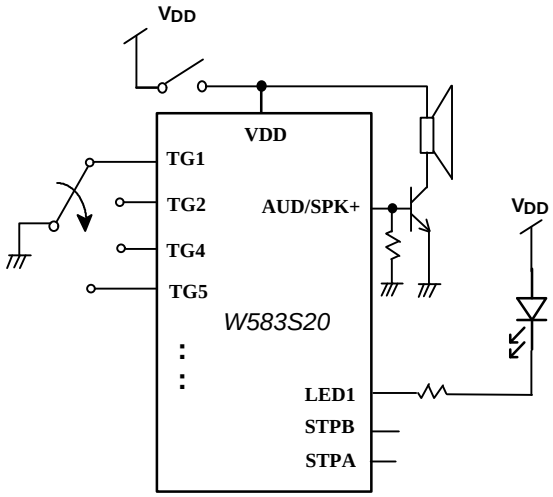
If one of the trigger pins is grounded, then the sound corresponding to that trigger will be played out at power-on.

Program:

```
W583S20
32:
     LD EN0, 0x00
     LD EN1, 0x00
     JP 16 @TG1_LOW
     JP 17 @TG2_LOW
     JP 18 @TG3_LOW
     JP 19 @TG4_LOW
     LD EN0, 0x0F
 0:
16:
     H51+S1+T51
     LD EN0, 0x0F
     END
 1:
17:

     H51+S2+T51
     LD EN0, 0x0F
     END
 2:
18:
     H51+S3+T51
     LD EN0, 0x0F
     END
 3:
19:
     H51+S4+T51
     LD EN0, 0x0F
     END
```

Application Circuit



Note: TG3/IRIN pin is not suitable for this kind application. Because of the special characteristic of TG3, if TG3 is grounded, the oscillator will keep working even the play statement is end and TG3 is disabled. If TG3 is used in this category application, it will cause the power consumption problem if power is not turned off. User has to avoid the happenings of similar application for TG3.

VIII.6.2 Matrix Input Application

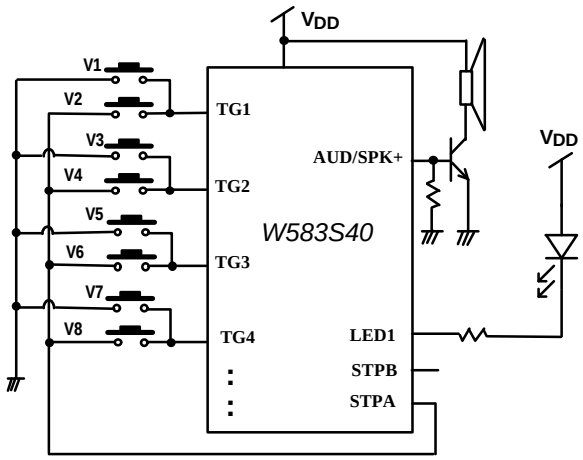
In this application, we use 4 trigger input pins and one output pin to organize the matrix with 8 inputs. User can follow this application to expand to more inputs by using more trigger input pins and output pins.

Program:

```
W583S40
32:
    LD STOP, 0x00          ; STPA set to low level
    LD EN0, 0x0F           ; One Shot play mode
    END
0:
    LD STOP, 0x01          ; STPA set to high level
    JP 18 @TG1_HIGH        ; check high
    H51+V1+T51             ; play V1
    LD STOP, 0x00          ; STPA set to low level
    END
18:                        ; pseudo trigger pin
    H51+V2+T51             ; play V2
    LD STOP, 0x00          ; STPA set to low level
    END
1:
    LD STOP, 0x01          ; STPA set to high level
    JP 19 @TG2_HIGH        ; check high
    H51+V3+T51             ; play V3
    LD STOP, 0x00          ; STPA set to low level
    END
19:                        ; pseudo trigger pin
    H51+V4+T51             ; play V4
```

```
    LD STOP, 0x00              ; STPA set to low level
    END
2:
    LD STOP, 0x01              ; STPA set to high level
    JP 20 @TG3_HIGH            ; check high
    H51+V5+T51                 ; play V5
    LD STOP, 0x00              ; STPA set to low level
    END
20:                            ; pseudo trigger pin
    H51+V6+T51                 ; play V6
    LD STOP, 0x00              ; STPA set to low level
    END
3:
    LD STOP, 0x01              ; STPA set to high level
    JP 21 @TG4_HIGH            ; check high
    H51+V7+T51                 ; play V7
    LD STOP, 0x00              ; STPA set to low level
    END
21:                            ; pseudo trigger pin
    H51+V8+T51                 ; play V8
    LD STOP, 0x00              ; STPA set to low level
    END
```

Application Circuit



Delay time: V1~V8: 2ms + debounce time

VIII.6.3 IR Application

In this application, we use "TX Rn" instruction to transmit the IR signal through IROUT pin, and we can get the filtered IR signal through TG3/IRIN pin.

Program (I), Transmit :

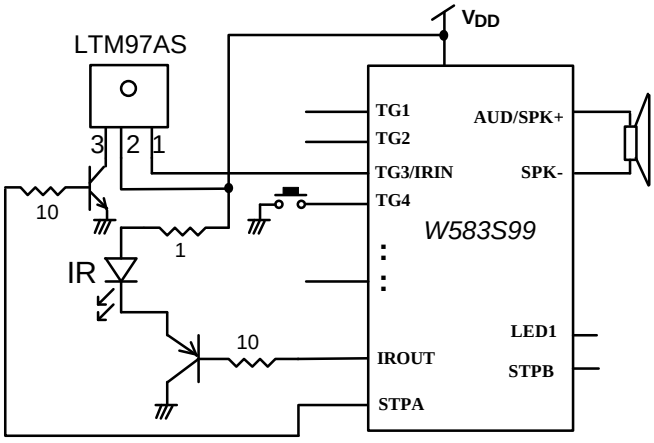
```
W583M02
VOUT_PWM
32:
    LD EN0, 0x03               ; Enable TG1, TG2
    END
```

```
0:
    LD R1, 21
    TX R1                    ; Data "21" are transmitted
    [25000]                  ; Add silence before END
    END
1:
    LD R1, 22
    TX R1                    ; Data "22" are transmitted
    [25000]                  ; Add silence before END
    END
```

Program (II), Receive :

```
W583M02
VOUT_PWM                     ; PWM type voice output
32:
    LD EN0, 00001000B        ; enable TG4 falling edge
    LD STOP, 00000001B       ; enable receive module
    JP 20
3:  LD STOP, 00000001B       ; enable receive module
    sound0
    JP 20
21:                          ; if receive "21", play sound1, sound2
    sound1+sound2
    JP 20
22:                          ; if receive "22", play sound3, sound4
    sound3+sound4
    JP 20
20:
    8*[65000]                ; waiting IR signal in this period
    LD STOP, 0000000B        ; disable receive module
    END
```

Application Circuit



IX. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	VDD - VSS	-	-0.3 - +7.0	V
Input Voltage	VIN	All Inputs	VSS-0.3 - VDD+0.3	V
Storage Temp.	TSTG	-	-55 - +150	℃
Operating Temp.	TOPR	-	0 - +70	℃

NOTE:
Operating the device under conditions beyond those indicated above may cause permanent damage or affect device reliability.

X. ELECTRICAL CHARACTERISTICS

(TA=25°C, VSS=0V, VDD=4.5V unless otherwise specified.)

X.1 DC PARAMETERS

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		2.4	3	5.5	V
Input Voltage	Vil		VSS-0.3	-	0.3×VDD	V
	Vih		0.7×VDD	-	VDD	
Standby Current	Isb1	VDD=3V, All I/O pins unconnected, No Playing			1	μA
	Isb2	VDD=5V, All I/O pins unconnected, No Playing			1	μA
Operating Current (Ring type)	IOP1	VDD=3V, No Load			500	μA
	IOP2	VDD=5V, No Load			1	mA
Operating Current (Crystal type)	IOP3	VDD=3V, No Load			600	μA
	IOP4	VDD=5V, No Load			1.2	mA
Input Current of TG1-TG8 pins	Iin1	VDD=3V, Vin=0V			-8	μA
Input Current of TEST pin	Iin2	VDD=3V, Vin=3V			50	μA
Input Current of SEL, /RESET and /DISOTP	Iin3	VDD=3V, Vin=0V			-8	μA
SPK (D/A Full Scale)	Idac	VDD=4.5V, Rl=100Ω	-4.0	-5.0	-6.0	mA
Output Current of STPA-STPH	IOL1	VDD=3V, Vout=0.4V	0.8			mA
	IOH1	VDD=3V, Vout=2.7V	-0.8			mA
Output Current of SPK+, SPK-	IOL2	VDD=3V, Rl=8Ω	100			mA
	IOH2		-100			mA
Output Current of WRP, RDP and DATA	IOL3	VDD=3V, Vout=0.4V	0.8			mA
	IOH3	VDD=3V, Vout=2.7V	-0.8			mA

X.2 AC PARAMETERS

ITEM	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation Frequency (ICE chip W58300)	Fosc1	Ring oscillator, Rosc=270KΩ	2.7	3	3.3	MHz
		Ring oscillator, Rosc=560KΩ	1.3	1.5	1.7	
Oscillation Frequency	Fosc2	Ring oscillator, Rosc=750KΩ	2.7	3	3.3	MHz

(Production chip W583xxx)		Ring oscillator, Rosc=1.6MΩ	1.3	1.5	1.7	
Oscillation Frequency Deviation by Voltage Drop	$\frac{\Delta Fosc}{Fosc}$	$\frac{F(3V)-F(2.4V)}{F(3V)}$			7.5	%
Instruction Cycle Time	Tins	Fosc = 3 MHz, SR = 6 KHz		1/3		mS
POI Delay Time	TPD			160		mS
Long Debounce Time	TDEBL	Fosc = 3 MHz, SR = 6 KHz	50			mS
Short Debounce Time[1]	TDEBS		400			µS

1. For ring oscillator only.

X.3 REFERENCE TABLE OF RESISTOR FOR RING OSCILLATOR

W58300 ICE chip	W583xxx Production chip	Fosc@4.5V
220 KΩ	620 KΩ	
240 KΩ	680 KΩ	3MHz more
270 KΩ	750 KΩ	typical 3MHz
300 KΩ	820 KΩ	3MHz less
330 KΩ	910 KΩ	
510 KΩ	1.4 MΩ	1.5MHz more
560KΩ	1.6 MΩ	typical 1.5 MHz
620KΩ	1.8 MΩ	1.5MHz less

Winbond Electronics Corp.

REVISION HISTORY

VER.	DATE	EDITOR	DESCRIPTION
A1	Sep. 1998	S.T. Chang	Initial Issued
A2	Jan. 1999	S.T. Chang	II FEATURES Operating voltage range: 2.4 - 5.5 Volts V.1 TG1-TG8 Add description on TG3/IRIN V.4 IROUT Add description VI.2 INTERRUPT VECTOR ALLOCATION Add description VI.6.1 *MODE0 Register* Bit 0 reserved Add description on MODE0.5 VI.6.2 *MODE1 Register* Add description on MODE1.0 VI.6.3 *PAGE Register* Add description VI.6.4 *EN0, EN1 Registers* Bits 0-3 Symbol change VI.12 IR INTERFACE Add S/W IR waveform VI.12.1 *H/W IR Protocol* AC parameter change VI.13 CPU INTERFACE Add description, timing diagram VII.6 END Add description because of the special characteristic of TG3/IRIN pin VIII.1 PLAY STATEMENT Add maximal value of silence in second VIII.6.6 Power-on Trigger Add notes X.1 DC PAREMETERS Change Data X.2 AC PAREMETERS Change Data
A3	Feb. 1999	S.T. Chang	Change W583XX to W583xxx in whole document I. General Description Add ROM size table X.1 AC PAREMETERS Change data of parameter Fosc2 X.3 REFERENCE TABLE OF RESISTOR FOR RING OSCILLATOR Add this section
A4	Apr. 1999	S.T. Chang	Change W55Fxx to W55F05, W55F20 in whole document V.5 OSC/XIN, XOUT and SEL Add application circuit V.11 VSS

			Add 0.1μF capacitor description VI.13 CPU INTERFACE Revise program in example
A5	Oct. 1999	Sophia Ho	Add three bodies with two chips solution W583S-03 W58300+W55F01 W583M-03 W58300+W55M06 W583M-04 W58300+W55M08