Winbond Electronics Corp.

HIGH FIDELITY *POWER SPEECH* ä

GENERAL DESCRIPTION

The W523Sxx family are programmable speech synthesis ICs that utilize Winbond's new high fidelity voice synthesis algorithm to generate all types of voice effects with high sound quality.

The W523Sxx's LOAD, JUMP, MOVE and INC commands as well as ten programmable registers provide powerful user-programmable functions that make this chip suitable for an extremely wide range of speech IC applications.

The W523Sxx family includes 14 kinds of bodies that are the same except for the voice duration shown below:

PART #	**W523S08**	**W523S10**	**W523S12**	**W523S15**	**W523S20**	**W523S25**	**W523S30**
Duration	8 sec	10 sec	12 sec	15 sec	20 sec	25 sec	30 sec
ROM	288 K	384 K	480 K	640 K	768 K	896 K	1024 K
PART #	**W523S40**	**W523S50**	**W523S60**	**W523S70**	**W523S80**	**W523S99**	**W523M02**
Duration	40 sec	50 sec	60 sec	70 sec	80 sec	100 sec	120 sec
ROM	1472 K	1760 K	2048 K	2560 K	3072 K	3520 K	4096 K

Note: 1. The voice durations are estimated by 6.4 KHz sampling rate.
2. The ICE chip is W58300

FEATURES

- o Wide operating voltage range: 2.4 - 5.5 volts for both DAC and PWM output
- o New high fidelity synthesis algorithm
- o Either PWM mode or D/A converter mode can be selected for AUD output
- o Provides 4 direct trigger inputs that can easily be extended to 24 matrix trigger inputs
- o Two trigger input debounce times (50 mS or 400 uS) can be set
- o Provides up to 2 LEDs and 5 STOP outputs
- o Flexible functions programmable through the following:
  - ■ *LD (Load), JP (Jump), MV (Move) and INC (Increase) commands*
  - ■ *Four general purpose registers: R0, R1, R2 and R3*
  - ■ *Six special purpose registers: EN0, EN1, MODE0, MODE1, STOP and PAGE*
  - ■ *Conditional instructions: @LAST, @TGn_HIGH or LOW, where, n = 1,2,5 or 6*
  - ■ *Speech equations*
  - ■ *END instruction*
- o Supports CPU interface operation
- o Symbolic compiler supported
- o Instruction cycle ≤ 400 μS typically
- o Section control for
  - ■ *Variable frequency: 4.8/6/8/12 KHz*
  - ■ *LED: ON/OFF*
- o Up to 256 voice groups can be used in single page mode; or extended to 2,048 voice groups in multi page mode, such as 8-page, 16-page and 32-page.

Publication Release Date: Oct. 2000
Revision A1

PAD LIST and DESCRIPTION

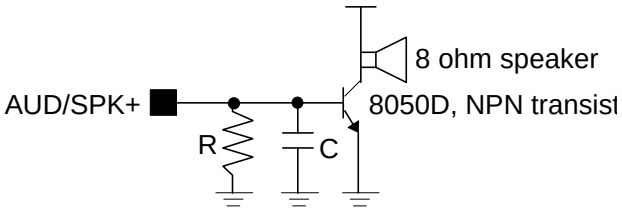
Name	I/O	Description
OSC	I	Ring oscillator input
VDD1	-	Positive power supply
TEST	I	Test pin
/RESET	I	Active low to reset all devices as Power On Reset (POR) function.
TG1	I	Trigger input 1. Low active.
TG2	I	Trigger input 2. Low active.
TG5	I	Trigger input 5. Low active.
TG6	I	Trigger input 6. Low active.
VSS1	-	Negative power supply
LED1	O	LED1 output
STPA/BUSY	O	STOP signal A output or BUSY signal output
STPB	O	STOP signal B output
LED2/STPC	O	LED2 output or STOP signal C output
STPD	O	STOP signal D output
STPE	O	STOP signal E output
AUD/SPK+	O	Current type output or PWM output for driving Speaker
SPK-	O	PWM output for driving Speaker
VSS2	-	Negative power supply
VDD2	-	Positive power supply

TG1 – TG4

Internally pulled high by a PMOS device with an equivalent resistance of around 500KΩ. After debounced by 40 mS, the direct trigger inputs start to execute the corresponding voice groups, whose number are 0, 1, 8, 9 for the falling edge triggers and 4, 5, 12, 13 for the rising edge triggers of the TG1, TG2, TG5 and TG6 respectively.

AUD/SPK+ and SPK-

The AUD/SPK+ pin is a current-type voice output when declaring as AUD output in option control, which is connected to the output of the internal D/A converter. The full scale of output of the 8-bit D/A converter is 5mA, which is able to drive the external 8-Ω speaker through the amplification of a low-power NPN transistor with a β of 120-160. Usually, an 8050D transistor is appropriate.

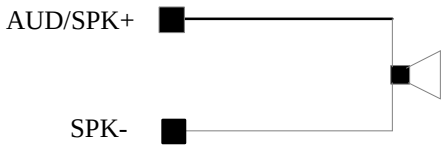


The shunt resistor R in the above figure is used to adjust the current that enters into the base of the NPN transistor for driving the external speaker without distortion, which is often encountered in such a simple amplification scheme under large input current conditions.

Two factors cause distortion, one is the saturation phenomenon of the transistor due to larger I_B, the other one is the introduction of R that cuts small signals out of the original waveform. A typical value of the shunt resistor is around 510Ω-1KΩ. The smaller the resistance, the smaller the current enters the transistor and vice versa..

The capacitor C is used for low-pass filtering the unwanted high-frequency noises that are generated from the D/A converter during sample transitions. Users may adjust the capacitance to reach better perceptual hearing. It could be simply omitted without affecting the voice quality too much.

Another case is AUD/SPK+ and SPK- act as PWM (Pulse Width Modulation) outputs. In this case DAC will be disabled. SPK+ and SPK- can directly drive a speaker without any extra component as below diagram.



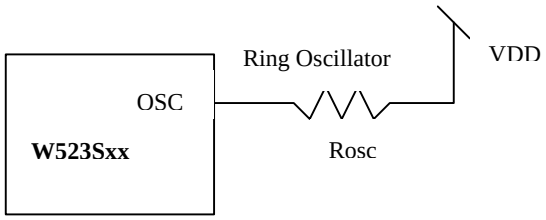
STPA - STPE

For STOP outputs, these pins are inverted-type stages. User may define different STOP outputs at certain timing slot by programming *.out file of the *PowerSpeech ä* synthesizer. After compilation, the Stop signals will be controlled by the internal STOP register, which can be manipulated by register operation. Typically, the Stop signals are used to drive external components, like motors, LEDs, light bulbs, etc.

OSC

A ring oscillator is used to generate the master frequency of around 1.5 MHz or 3 MHz.

The OSC pin is connected directly to VDD by way of a Rosc resistor, which is used to provide a bias current for the ring oscillator.



Note:

Rosc = 1.2M ohm for 3 MHz application.

Rosc = 2.4M ohm for 1.5 MHz application.

/RESET

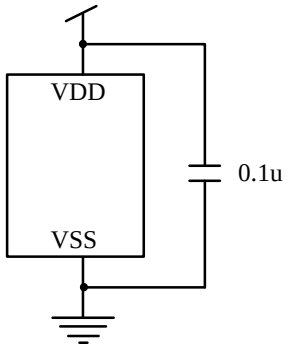
Active low reset input with an internal pull-high resistance of 500 KΩ. The falling edge of the /RESET pin will reset the whole W523Sxx devices, just like the Power On Reset (POR) condition. Right at the rising edge of the /RESET input, the W523Sxx starts to awake and continues to undergo the Power On Initialization (POI) process.

VDD (VDD1 and VDD2)

Positive power supply: In order to prevent possible power noises generated during motor driving from interfering the proper operations of the internal POR circuit, which is essential to the POI process of the *PowerSpeech ä* synthesizers, two approaches are being adopted in the W523Sxx: one is to use /RESET pin, which is described in detail elsewhere, to fully reset the internal circuits for a brand new start; the other is to place VDD and VSS apart as far as possible to reduce the possibility of noise induction.

VSS (VSS1 and VSS2)

Negative power supply: In order to let W523Sxx work properly, it is necessary to add a 0.1μF~10μF capacitor between VDD and VSS.



FUNCTIONAL DESCRIPTION

INSTRUCTION SET

The W523Sxx family *PowerSpeech ä* program instruction sets include unconditional instructions and conditional instructions. Most of these instructions are programmed by writing “LD (Load)”, “JP (Jump)” and “MV (Move)” commands and by modifying the content of the R0 ~ R3, EN0/EN1, STOP, MODE0/MODE1 registers.

Registers

R0 ~ R3 register

There are 4 general-purpose registers in W523Sxx, R0, R1, R2 and R3. They are 8-bit register that stores the entry values of from 0 to 255 voice groups. The structure of these registers is shown below:

Bit:	7	6	5	4	3	2	1	0
Rn:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

The default value is "0010 0000" in binary format. This value is equal to 32 in decimal format.

EN0 and EN1 register

Both of EN0 and EN1 are 8-bit register that stores the rising/falling edge enable or disable status information for all trigger pins, which determines whether each trigger pin is retriggerable, non-retriggerable, overwrite or non-overwrite. The 8-bit structure of this register and the rising or falling edge of the triggers corresponding to each bit are shown below:

EN0:

Bit:	7	6	5	4	3	2	1	0
TG:	X	X	2R	1R	X	X	2F	1F

EN1:

Bit:	7	6	5	4	3	2	1	0
TG:	X	X	6R	5R	X	X	6F	5F

The digits 1, 2, 5 and 6 in "TG:" row represent triggers 1, 2, 5 and 6 respectively; "F" represents the rising edge; and "R" represents the falling edge. When any one of the eight bits is set to "1", the rising or falling edge of the corresponding trigger pin can be enabled, interrupting the current state.

"X" indicates a "don't care" bit.

The default value is shown as below:

EN0: XX11 XX11 in binary format.

EN1: XX11 XX11 in binary format.

STOP register

The STOP register stores "STOP" output status information to determine the voltage level of each stop output pin. The 8-bit structure of this register and the stop output pin corresponding to each bit are shown below:

STOP:

Bit:	7	6	5	4	3	2	1	0
STOP:	X	X	X	STPE	STPD	STPC	STPB	STPA

The default value for the STOP register is "XXX1 1111" in binary format.

MODE0 and MODE1 registers

The MODE0 and MODE1 registers are used to store operand information to select among various operating modes as show below:

MODE0 Register:

BIT	DESCRIPTION	DEFINITION
7	LED mode	1: Flash
		0: DC
6	LED2/STPC	1: LED2 output
		0: STPC output
5	X	Don' t care
4	Debounce time	1: Long debounce time (50 mS)
		0: Short debounce time (400 uS)
3	X	Don' t care
2	STPA/BUSY	1: STPA output
		0: BUSY output (CPU mode)
1	X	Don' t care
0	X	Don' t care

Bit 7 is used to determine the output status of LED1 and/or LED2: Flash alternate or synthronous output, or DC (LED will be lit constantly without flash).
Bit 6 determines whether the output pin (i.e., pad 12) acts as an LED output or STOP output pin.
Bit 4 is used to determine whether the debounce time for all trigger inputs is long (around 50 mS) or short (around 350 uS).
Bit 2 determines whether the output pin (i.e., pad 10) acts as STOP output pin or BUSY output for CPU mode operation.
Bit 5, 3, 2, 0: Don' t care bits.

MODE1 Register:

BIT	DESCRIPTION	DEFINITION	Declaration
7	X	Don' t care	
6	X	Don' t care	
5	LED Flash type	1: Alternate	LED_ASYN
		0: Synthronous	LED_SYN
4	LED1 section control	1: Yes	LED1_S_CTL
		0: No	LED1_S_OFF
3	LED2 control	1: Section control	LED2_S_CTL
		0: STPC control	LED2_STC_CTL
2	LED1 volume control	1: Off	LED_VOL_OFF
		0: On	LED_VOL_ON

1	X	Don' t care
0	X	Don' t care

Bit 5 is used to determine the flash type of LED1 and/or LED2: Flash alternate or synthronous output.
Bit 4 determines whether the output pin (i.e., pad 12) acts as an LED output or STOP output pin.
Bit 3 is used to determine whether the debounce time for all trigger inputs is long (around 50 mS) or short (around 350 uS).
Bit 2 determines whether the output pin (i.e., pad 10) acts as STOP output pin or BUSY output for CPU mode operation.
Bit 7, 6, 1, 0: Don' t care bits.

PAGE Register

Bit	7	6	5	4	3	2	1	0
PAGE	-	-	-	PG4	PG3	PG2	PG1	PG0

The bits 0 ~ 4 in PAGE register are used for page selection. Once the page mode being defined (referring to the below section of "Option Control Function"), the working page is selected by the bits 0 ~ 4 in the PAGE register. Hence, the user can execute "LD PAGE, value" instruction to change the working page of the voice entry group. Not all of the bits 0 ~ 4 of PAGE register are used in different page mode. They are listed as below table:

Page Mode	PG4	PG3	PG2	PG1	PG0
1-page	×	×	×	×	×
8-page	×	×	√	√	√
16-page	×	√	√	√	√
32-page	√	√	√	√	√

Where "×" means don't care and "√" means must be set properly.

Note that if PAGE register is changed by instruction in a global repeat loop, the global repeat will not be completely finished because the chip will jump to the page selected by PAGE register.

POWER ON INITIALIZATION

Whenever the W523Sxx is powered on or pressed /RESET pin, the programs contained in the 32nd voice group will be executed immediately. Thus the user can write programs into this group to set the initial power-on state. If the user does not wish to execute any programs at power-on, an "END" instruction should be entered in the group 32.

VOICE GROUP ENTRY ALLOCATION

The W523Sxx provides 4 triggers as interface with the outside world directly. In the wake of being de-bounced, the W523Sxx responds to each edge of a valid trigger with a voice group entry point, provided that the associated enable flag of that particular edge is set previously. The triggered input then starts to execute the interrupt vector by overwriting current operations. The de-bounce time of trigger input is around 20-40mS or 160μs-320μs depending on the forth bit of MODE0 setting.

For direct trigger inputs, there are 8 interrupt vectors allocated for four trigger pins which is shown as below table:

Interrupt Vector	*Trigger Source*	
0	TG1F	Falling edge
1	TG2F	
8	TG5F	
9	TG6F	
4	TG1R	Rising edge
5	TG2R	
12	TG5R	
13	TG6R	

Interrupt vectors 0, 1, 8, 9 are reserved for falling edge triggers, and interrupt vectors 4, 5, 6, 12, 13 are reserved for rising edge triggers.

OPTION CONTROL FUNCTION

There are four types of option that can be determined by a declaration in the user's program file, but cannot be controlled by register.

Function	Option Control Declaration	Definition
Page mode definition	DEFPAGE 1	256 labels for 1 page, 1 page in total (1-page mode)
	DEFPAGE 8	256 labels for 1 page, 8 pages in total (8-page mode)
	DEFPAGE 16	128 labels for 1 page, 16 pages in total (16-page mode)
	DEFPAGE 32	64 labels for 1 page, 32 pages in total (32-page mode)
Normal or CPU mode	NORMAL	Normal mode operation
	CPU	CPU mode operation
Oscillator frequency definition	OSC_3MHZ	3 MHz oscillator
	OSC_1.5MHZ	1.5 MHz oscillator
Voice output setting	VOUT_DAC	DAC (AUD) output
	VOUT_PWM	PWM output

(1). "Page mode definition" decides the page operation mode of W523Sxx. The default setting of the page mode is 1-page mode. The 8-page, 16-page or 32-page mode must be declared in preceded to expand the entry point from 257 up to 2048.

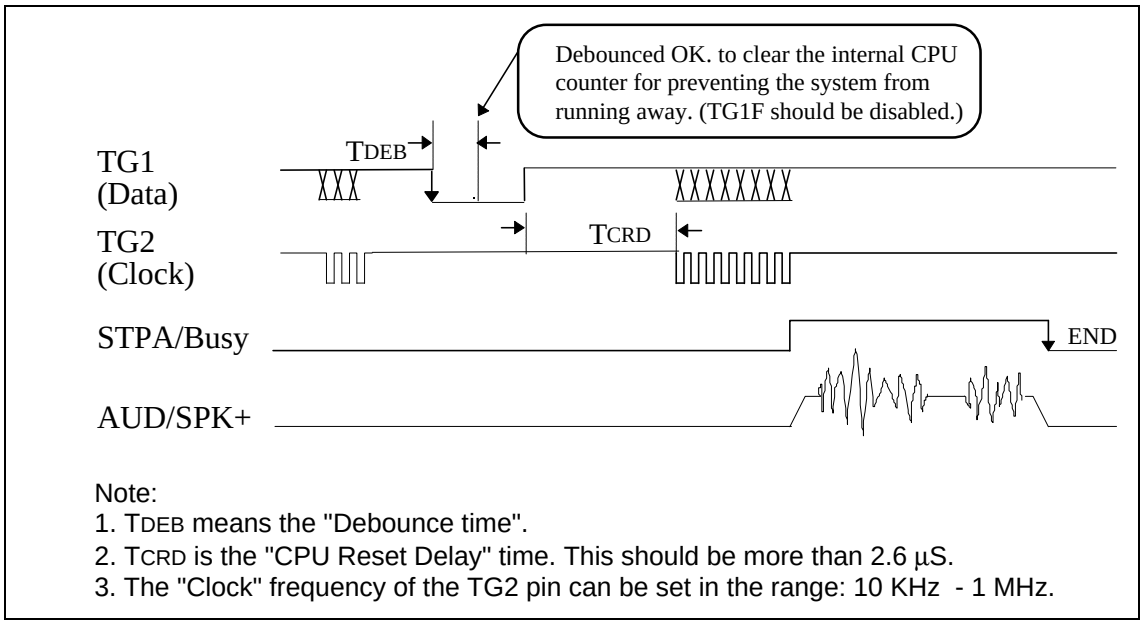
(2). "Normal or CPU mode" is defined to set the device's operation being the defaulted normal mode or CPU mode. In CPU mode, the TG1 and TG2 of the device can be as a CPU interface to cope with another micro-controller in the outside world. About the detail operation and timing diagram in the CPU mode, please refer to the "CPU Interface" section below.

(3). "Oscillation frequency definition" is designed for selecting the frequency of the system clock as 3 MHz (OSC_3MHZ) or 1.5 MHz (OSC_1.5MHZ).

(4). "Voice output setting" is designed for user to select the voice output type as DAC output mode (VOUT_DAC) or PWM output mode (VOUT_PWM).

CPU INTERFACE

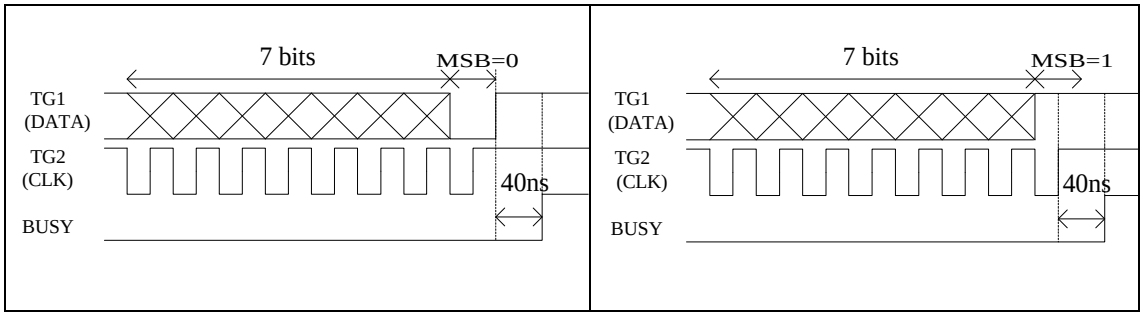
The W523Sxx can communicate with an external microprocessor through a simple serial CPU interface. The W523Sxx CPU interface consists of TG1, TG2 and STPA/BUSY pins, whose timing diagrams are shown below:



Note:
1. TDEB means the "Debounce time".
2. TCRD is the "CPU Reset Delay" time. This should be more than 2.6 µS.
3. The "Clock" frequency of the TG2 pin can be set in the range: 10 KHz - 1 MHz.

Busy signal will output "high" after the end of transmission. The rising timing of Busy signal is dependent on the MSB of data output on TG1 (DATA) pin.

As the timing diagrams showing below, in case the MSB is "1" (see right side of below diagrams), the "BUSY" pin's signal will be risen after the last rising edge of TG2 (CLK) pin and in the wake of more than 40 nS; in case the MSB is "0" (see left side of below diagrams), the "BUSY" pin's signal will be risen after the rising edge that TG1(Data) returns to high and in the wake of more than 40 nS.



To place the W523Sxx in CPU mode, program the code according to the following example.

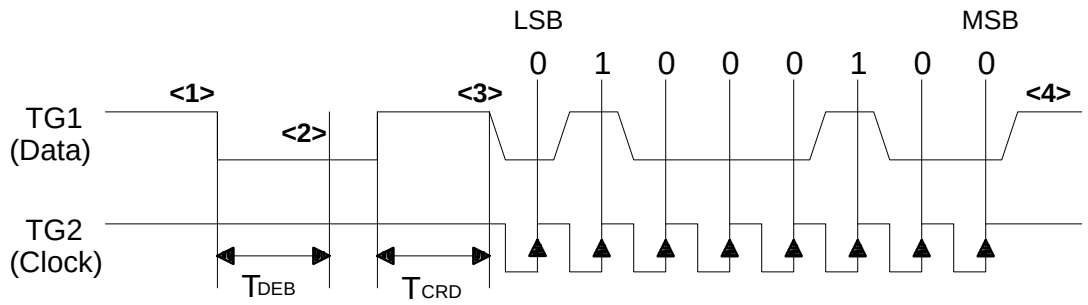
```
W523S60
CPU        ; Reserved word, used as a directive to notify the compiler for post processing.
LED1
FREQ2

POI:
    LD EN0, 0x00
    H5+voice1+T5
    END
```

```
34:             ; Direct trigger or CPU interrupt.
        H5+voice2+T5
        END
```

The defaulted operating mode of the W523Sxx is normal mode, which is identified by the "NORMAL" and "CPU" option control. To enter the CPU mode, the "CPU" declaration must be inserted in the declaration region of program (*.out). In CPU mode, the third bit of MODE0 will be set as "0" (BUSY output) automatically by the compiler unless otherwise specified explicitly by the STPA directive. The CPU, STPA, and BUSY directives can appear only in the first paragraph of the *.out files so that the compiler will automatically interpret them as Stop definitions in the POI interrupt vector. If these directives are placed elsewhere, an error message will be issued during the compilation process.

In the program example shown above, the external μC will transfer one byte data "34" to W523Sxx. The number 34 (Decimal) is equal to 00100010b (Binary). The interface timing is shown below.



<1> When TG1 is pulled low, the W523Sxx stops playing voice or executing instruction and waits for data from the external μC.
<2> If TG1 is debounced OK, the W523Sxx will clear the CPU receiving buffer.
<3> 8-bit data are transferred by TG1 (Data) and TG2 (Clock). LSB is sent firstly.
<4> TG1 returns to high and starts the CPU interrupt service. In this case W523S60 will play the H51+voice2+T51 sections and the STPA/BUSY pin is pulled high during the playing period.

The STPA/BUSY pin is normally set as the STPA output in normal mode after power up or the /RESET pin is triggered, if the MODE0.2 bit is not altered or no "BUSY" declaration is invoked in the *.out files. In CPU mode, the STPA/BUSY pin usually functions as a handshaking signal, called BUSY, that is used to check the busy status. However, in CPU mode the STPA/BUSY pin can also be configured as an STPA output. Moreover, in normal mode this pin can also be configured as a BUSY signal. So customers should consider carefully what type of output signal is desired from the STPA/BUSY pin.

The BUSY signal goes to high, indicating the W523Sxx is busy, after eight consecutive clocks have been successfully transmitted from the external μC and TG1 has returned to high. It returns to low state after an END instruction is encountered, provided there are no more global repeats. See the timing diagrams for further details. In normal mode, the BUSY signal also goes to high after a trigger is debounced successfully and stays high until the W523Sxx returns to the standby state. Normal mode and CPU mode may both be used in the same application.

The TG1 pin, which is pulled high with a 500KΩ resistor, should be kept high during non-transmission periods to reduce power consumption. The external μC should be connected to the W523Sxx by an inverted-type output port for better noise immunity. In CPU mode, the W523Sxx stops operating upon the falling edge of the TG1 pin. For the CPU interface to work normally, TG1F should be disabled. Suggest TG1F, TG1R, TG2F, and TG2R should all be disabled in CPU mode.

INSTRUCTION SET

There are two types of instruction in the W523Sxx family, unconditional and conditional instructions. The first type of instruction is executed immediately after they are issued and the second one is executed only when the condition specified in the instruction is satisfied. All of these instructions are listed in the following table.

Unconditional		Conditional		
JP	G	JP	G	@STS
JP	Rn	JP	Rn	@STS
LD	ENi, value	LD	ENi, value	@STS
LD	MODEi, value	LD	MODEi, value	@STS
LD	STOP, value	LD	STOP, value	@STS
LD	PAGE, value	LD	PAGE, value	@STS
LD	Rn, value	LD	Rn, value	@STS
END		END		@STS
MV	Rn, Rm	MV	Rn, Rm	@STS
INC		INC		@STS

Legend: *G: Interrupt vector/label*
Rn: R0-R3
Rm: R0-R3
Eni: EN0, EN1
MODEi: MODE0, MODE1
value: 8-bit data, ranges from 0 to 255
@STS can be the following: @TGn_HIGH for n=1,2,5,6, @TGn_LOW for n=1,2,5,6, and @LAST.

The cycle time to execute an instruction is around 400μs at the condition of sample rate equals to 6 KHz.

Jump (JP) Command:

JP G

Instruct the device to jump directly to the voice group entry (value or label) corresponding to the value or label, G, indicated. The voice group entry value may range from 0 to 255.

i.e., If the PAGE register is set as 16 or 32-page mode, the voice group entry value may range from 0 to 127 or 0 to 63 respectively for every page.

JP Rn (n=0~3)

Instructs device to jump to whatever voice group entry value is indicated by the value currently stored in register Rn. The voice group value may range from 0 to 255.

i.e., If the PAGE register is set as 16 or 32-page mode, the voice group entry value may range from 0 to 127 or 0 to 63 respectively for every page.

Load (LD) Command:

LD Rn, value (n=0~3)

This instruction is used to load a voice group entry value into the register Rn, where n can be 0-3. The voice group value may range from 0 to 255.

i.e., If the PAGE register is set as 16 or 32-page mode, the voice group entry value may *range from*

0 to 127 or 0 to 63 respectively for every page.

LD ENi, operand (I=0, 1)

This instruction is used to define the trigger interrupt settings by loading the operand message into register ENi.

a. The operand is an 8-bit value that can be entered in decimal (default) or hexadecimal (with "0x" as a prefix).

b. ENi is an 8-bit register that is used to enable/disable the rising/falling edge of each of the four trigger inputs.

c. When any one of the eight bits is set to "1" (default), the corresponding trigger will interrupt the current state at the edge indicated and execute the corresponding "interrupt vector/label". When the bits are set to "0", the triggers will be disabled.

d. The 8-bits correspond to the rising/falling edges of the triggers and the voice group entry addressing correspond to the interrupt vectors as follows:

EN0 bit:	7	6	5	4	3	2	1	0
TG:	X	X	2R	1R	X	X	2F	1F
Vector:	X	X	5	4	X	X	1	0
EN1 bit:	7	6	5	4	3	2	1	0
TG:	X	X	6R	5R	X	X	6F	5F
Vector:	X	X	13	12	X	X	9	8

where "nR/F" represents the rising/falling edge of the n-th trigger pin, and "X" represents "don't care"

<Example>: The instruction "LD EN0, 0x41" and "LD EN1, 0x03" is programmed.

Explanation:

a. For EN0, "41" is a hexadecimal value equal to the binary value "0100 0001"

b. These 8 bits of data represent the following trigger interrupt settings:

EN0 bit:	0	1	0	0	0	0	0	1
TG:	X	X	2R	1R	X	X	2F	1F
Vector:	X	X	5	4	X	X	1	0

c. For EN1, "20" is a hexadecimal value equal to the binary value "0010 0000"

d. These 8 bits of data represent the following trigger interrupt settings:

EN0 bit:	0	0	1	0	0	0	0	0
TG:	X	X	6R	5R	X	X	6F	5F
Vector:	X	X	13	12	X	X	9	8

Result:

a. When the falling edge of TG1 (1F) is activated, the EN0 register will cause TG1 to interrupt the current playing state and jump immediately to voice group "0", the interrupt vector that corresponds to 1F.

b. When the rising edge of TG6 (6R) goes active, the EN1 register will cause TG6 to interrupt the current playing state and jump immediately to voice group "13", the interrupt vector that corresponds to 6R.

c. No action will be taken when the other trigger pins are pressed, because the corresponding bits are set to "0".

LD STOP, value

This instruction loads the operand message into the STOP register to set the output status of the STOP output pins, STPA~STPE. When a particular bit of STOP register is set to "1", the corresponding STOP pins will be an active high output; when a bit is set to "0", the corresponding STOP pins will be a low output. The default value of the STOP register is "XXX1 1111".

<Example>: The instruction "LD STOP, 0x53" is programmed.

Explanation:

a. "53" is a hexadecimal value equal to a binary value of "0101 0011

b. These 8 bits of data represent the following settings:

Operand:	0	1	0	1	0	0	1	1
STOP:	X	X	X	STPE	STPD	STPC	STPB	STPA

Result:

a. The STPA, STPB and STPE will be high outputs.

b. The STPC and STPD will be low outputs.

c. The seventh bit "1" is a "don't care" bit and so has no effect on the stop signal output setting.

LD MODEi, operand (I=0, 1):

This instruction is used to select various operating modes by loading an operand message into the MODE0 and/or MODE1 registers from each of pairs of modes. The pairs of modes and the corresponding bits are as follows:

Bit:	7	6	5	4	3	2	1	0
MODE0:	Flash/DC	LED2/STPC	X	Long/Short	X	STPA/BUSY	X	X
Description:	LED mode	Pin selection	Don't care	Debounce time	Don't care	Pin selection	Don't care	Don't care

Bit:	7	6	5	4	3	2	1	0
MODE1:	X	X	Alter./Sync.	ON/OFF	Section/STPC	OFF/ON	X	X
Description:	Don't care	Don't care	LED flash type	LED1 section control	LED2 control	LED1 volume control	Don't care	Don't care

A "1" for one of these bits selects the first of the pair of modes indicated; a "0" selects the second of the pair. The initial value of the MODE0 and MODE1 registers are "11X1 X1XX" and "XX11 11XX" respectively.

i.e., "Alter." means "Alternate"; "Sync." means "Synchronous"

<Example>: The instructions "LD MODE0, 0xEF" and "LD MODE1, 0x00" are programmed.

Explanation:

a. "EF" is a hexadecimal value equal to a binary value of "1110 1111", and "00" is equal to binary value of "0000 0000".

b. These 8 bits of data represent the following settings:

Bit:	7	6	5	4	3	2	1	0
Operand:	1	1	1	0	1	1	1	1
MODE0:	Flash/DC	LED2/STPC	X	Long/Short	X	STPA/BUSY	X	X

Bit:	7	6	5	4	3	2	1	0
Operand:	0	0	0	0	0	0	0	0
MODE1:	X	X	Alter./Sync.	ON/OFF	Section/STPC	OFF/ON	X	X

Result:

In MODE0:

a. In bit 7, the LED (LED1and/or LED2) is set as "Flash" mode.

b. In bit 6, the "LED2/STPC" output pin is defined as "LED2" output function.

c. In bit 4, the trigger pins debounce time is set as "Short", that is around 400 uS.

d. In bit 2, the "STPA/BUSY" pin is defined as "STPA" output function. (i.e., The "BUSY" output mode is suitable for the "CPU mode" operation.)

e. The bit 5, 3, 1 and 0 are "Don't care" bits, so has no effect on the MODE setting no mater "0" or "1".

In MODE1:

a. In bit 5, the LED1 and LED2 will be in "Synchronous" mode as flashing.

b. In bit 4, the LED1 section control is set as "OFF" state, thus the LED1 cannot be controlled by voice sections independently in the PowerSpeech equation.

c. In bit 3, the LED2 pin is defined as "STPC control", thus, the LED2 output will be ON (or OFF) depending on the STPC output bit is set as "1" (or "0").

d. In bit 2, the LED1 volume control is set as "ON", thus the LED1' s on/off state is according to voice volume level.

e. The bit 7,6,1 and 0 are "Don't care" bits, so has no effect on the MODE setting no mater "0" or "1".

LD PAGE, value

This instruction is used to load an 8-bit data into the register PAGE. Although the *"value*" is an 8-bit data, its range is dependent on the page mode configuration of the declaration in user's program file (*.out). For example, if the declaration is "DEFPAGE 16", the PAGE mode is a 16-page mode, and the *"value*" to be loaded to PAGE register can only be the range from 0 to 15.

MV Rm, Rn (m, n = 0 ~ 3):

The data in Rn register are copied into Rm register and the data in Rn are unchanged. "m" and "n" can be 0 ~ 3, but "m" and "n" cannot be the same.

Increase (INC) Command:

Increase the data in R0 register by one. Note that "INC" instruction can only operate on R0.

END Command:

This command instructs the chip to cease all activity immediately.

Conditional Instruction "Instruction@STS":

Conditional instructions are executed only when the conditions specified in the instructions hold. An extension name "@STS" is added on the end of notation of the conditional instruction. The @STS can be one of the three kinds of conditions as follows,

(a). @LAST: At last time of global repeat.
(b). @TGn_HIGH: High voltage level of the nth trigger pin, where n=1,2, 5 or 6
(c). @TGn_LOW: Low voltage level of the nth trigger pin, where n=1, 2, 5 or 6

PROGRAMMING EXAMPLE

Speech equation

The Speech equation is used to define the combination of playback sound. The following is an example of a play statement format:

```
i:N
H5x+m1*(A_fl+m2*(B_fl+m3*(C_fl+m4*D_fl))+[1FFF0])+...T5x
END
```

(1). " i" is the voice group entry point. It can be a numerous with the range of 0 ~ 255, or symbolic.

(2). "N" represents the number of global repeats with the range of 1 to 16.

(3). “m1", "m2", “m3” and "m4” represent the number of local repeats with the range of 1 to 8.

(4). There is no limit in the number of "( )". However, each pair of "( )" must be written on the same line.

(5). "A", "B", "C", and "D" represent the files containing converted voice data (*.wam)

(6). "*_fl*" is the section control setting, and the parameters "*f*" and "*l*" are defined below:

f : Sampling Frequency definition (default value: *f*=1)

f	3	2	1	0
Frequency	12 KHz	8 KHz	6 KHz	4.8 KHz

l : LED Status definition (default value: *l*=0)

l	1	0
LED Status	On	Off

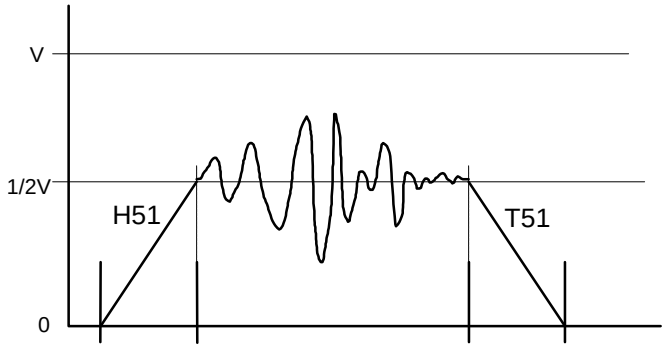
Note 1: If the section control setting is not defined, the default values will be used.

Note 2: If the section control setting is defined, both the "*f*" and "*l*" digits must be defined together. For instance, "H51+A_2+T51" is a wrong speech equation since only one digit (*f=2*) is defined.

(6). [1FFF0] represents a period of silence with the duration “1FFF0” (around 5.4 seconds in the condition of 6 KHz sampling rate). The maximum silence length in one "[ ]" is [FFFFF], that is 1M bits, around 43.7 seconds at 6 KHz sampling rate. Another syntax for silence is to express time duration directly by second or millisecond, like [21.3 sec], [132.5 msec]. Of course the length cannot exceed the maximum silence length. The maximal values in second under different sampling rate are listed below:

Sample Rate	4.8 KHz	6 KHz	8 KHz	12 KHz
Maximal Value	54.61 sec	43.69 sec	32.76 sec	21.84 sec

(7). "H5x" and "T5x", x ranges from 1 to 5, are the Head file and Tail file with the data format for W523Sxx. They are inserted only the voice output type is AUD output. **If PWM output is selected (by Option Control Declaration), H5x and T5x are not needed**. These two files can be used to eliminate the popping sound which may occur when the sound starts and stops. The following is a sample waveform:



Programmable Power-on Initialization (POI)

Whenever the W523Sxx *PowerSpeech™* is powered on, the programs contained in the interrupt vector 32 will be executed immediately. Programs can therefore be written into this interrupt vector to set the initial power-on state. If the user does not wish to execute any programs at power-on, an "END" instruction should be entered in interrupt vector 32.

*PowerSpeech*ä Program Format

The W523Sxx *PowerSpeech*ä has a programming language to define the product functions. An example of the W523Sxx *PowerSpeech*ä program format is shown below. Explanatory notes follow the example.

```
(1) ⇒  W523S60

(2) ⇒  DEFPAGE 8
       NORMAL
       OSC_3MHZ
       VOUT_DAC

(3) ⇒  FREQ1
       LED0

(4) ⇒  LED_ASYN
       LED1_S_OFF
       LED2_S_CTL
       LED_VOL_OFF
       BUSY

(5) ⇒  PAGE0  ◄──── (7)
       32: 5  ◄──── (8)
          H51_SN_31+SN_20+SN_11+T51  ◄──── (9)
(6) ──┘   END
       0:  3
          H51+S1+S2+[0X1FFF0]+T51
          END
       2:  ◄──── (10)
          LD R0, 64
          LS EN0, 0X00    ; DISABLE ALL TRIGGERS
          LD EN1, 0X00
          LD STOP, 0X08    ; STPD HIGH OUTPUT
          END
                    ▲
                    └──── (11)
```

Legend:

(1) **Chip Body**: User must first defines the *PowerSpeech*ä body to be used, or else an error message will appear during compiation. In W523Sxx family, the chip bodies include W523S08, W523S10, W523S12, W523S15, W523S20, W523S25, W523S30, W523S40, W523S50, W523S60, W523S70, W523S80, W523S99 and W523M02.

(2) **Option Control Declaration:** State the option control function in this region. These declarations will decide the corresponding function in the chip and they cannot be changed in user's program.

.

Declaration	Option Control Function	Comment
DEFPAGE 1	1-page mode	default
DEFPAGE 8	8-page mode	
DEFPAGE 16	16-page mode	
DEFPAGE 32	32-page mode	
NORMAL	Normal mode	default
CPU	CPU mode	
OSC_3MHZ	3 MHz system clock	default
OSC_1.5MHZ	1.5 MHz system clock	
VOUT_DAC	DAC type voice output	default
VOUT_PWM	PWM type voice output	

(3) Section Control Declaration: State the section control in this region. The section control can be changed in the SPEECH equation.

Declaration	Section Control Function	Comment
FREQ0	4.8 KHz sample rate	
FREQ1	6 KHz sample rate	default
FREQ2	8 KHz sample rate	
FREQ3	12 KHz sample rate	
LED0	LED Off	default
LED1	LED On	

(4) **Register Control Declaration:** State the register control in this region. The user can use register control declaration or "LD" instruction to get the wanted setting since MODE0 and MODE1 registers are user programmable. The different between these two methods is that once the user use Register Control Declaration to get the wanted setting, he is not able to change the setting by "LD" instruction in the program.

Declaration	Register Control Function
LED_ASYN	LED output in alternate mode
LED_SYN	LED output in synchronous mode
LED1_S_CTL	LED1 section control ON
LED1_S_OFF	LED1 section control OFF
LED2_S_CTL	LED2 section control ON
LED2_STC_CTL	LED2 as STPC control
LED_VOL_OFF	LED volume control OFF
LED_VOL_ON	LED volume control ON
STPA	Set STPA/BUSY pin as STPA output
BUSY	Set STPA/BUSY pin as BUSY output

(5) **Program Block**: Application program and speech operations are written in this area, including the following:
Define voice group entry value with the range of 0 ~ 255.
Determine the number of global repeats.
Describe speech equations.
Define the register values and instructions.

Note 1: The maximum program memory size that W523Sxx can reach is 16M bits.

Note 2: Every GO instruction occupies 32 bits, and every voice group entry value also occupies 32 bits.

Note 3: The GO instruction can include the following contents:
(a). Any instruction listed in INSTRUCTION SETS section.
(b). Any speech data file(*.wmd) for the speech equation.

For example, in the speech equation: "H51+A+B_21+C+T51", there are a total of 5 GO instructions: H51, A, B_21, C, and T51.

(6) **Interrupt Vector/Label**: Define the interrupt vector/label.

Product	Voice group entry value	TG interrupt vector	POI group entry value
W523Sxx	0-255*	0-15	32

* The PAGE register must be used in order to access the interrupt vector/label that exceeds 255.

The voice group entry value can also be expressed by symbolic label. There are several reserved words of page 0 as below:

Voice group entry value	0	1	4	5	32
Symbol	TG1F	TG2F	TG1R	TG2R	POI
Voice group entry value	8	9	12	13	-
Symbol	TG5F	TG6F	TG5R	TG6R	-

(7) **Page Start**: If the page mode configuration is not 1-page mode, the user must insert Page Start (PAGE0, PAGE1, ...) to separate the voice group entries into different pages.

(8) **Global Repeat**: The global repeat number can be the range from 1 to 16. This number must be placed on the same line as the voice group entry.

(9) **Play Statement**: They are used to define the combination of playback sound.

(10) **Blank**: An voice group entry must be followed by one full blank line without any instruction or speech equation except the global repeat.

(11) **Note**: A semicolon (";") is used to distinguish characters that are not part of the program. Characters written to the right of the semicolon are not considered as part of the program.

Some Examples

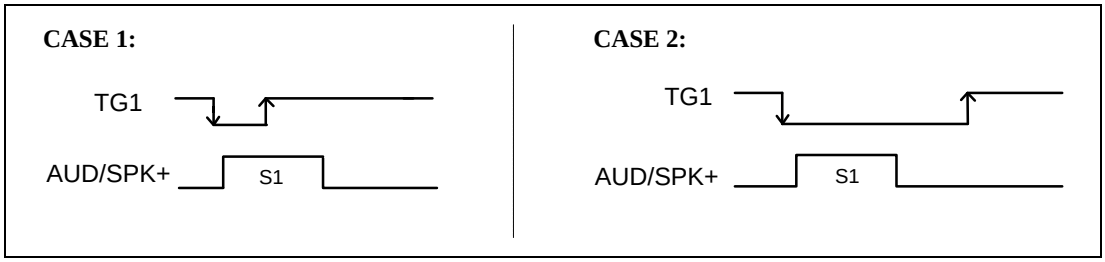
In this section we will present several programming examples for the W523Sxx *PowerSpeech™* chips. The user's programs should be written in ASCII code using a text editor. After being compiled, the sound effects resulting from the programs can be tested by using a Winbond demo board. We choose DAC type voice output in the examples.

Four Playing Modes Setting

A. One-Shot Trigger Mode

```
0:                          ; TG1 falling edge interrupt vector
      LD EN0, 0x01          ; Enable TG1 falling edge input only
      H51+Sound1+T51
      END
```

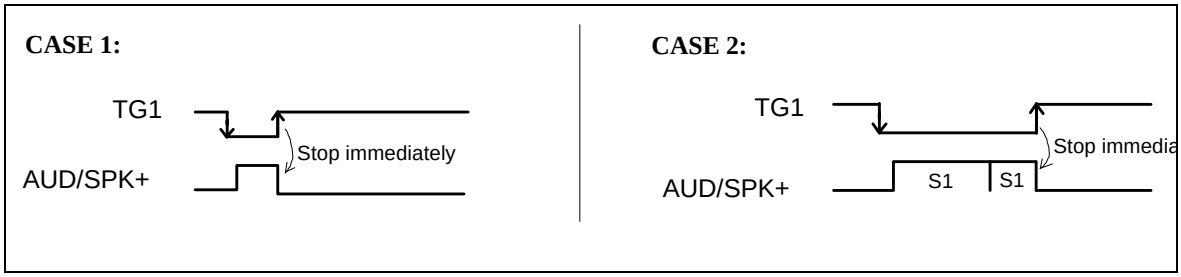
Timing diagram:



B. Level Hold Trigger Mode

```
0:                          ; TG1 falling edge interrupt vector
    LD EN0, 0x11            ; Enable TG1 falling and rising edge input
    H51+Sound1+T51
    JP 0
4:                          ; TG1 rising edge interrupt vector
    END
```

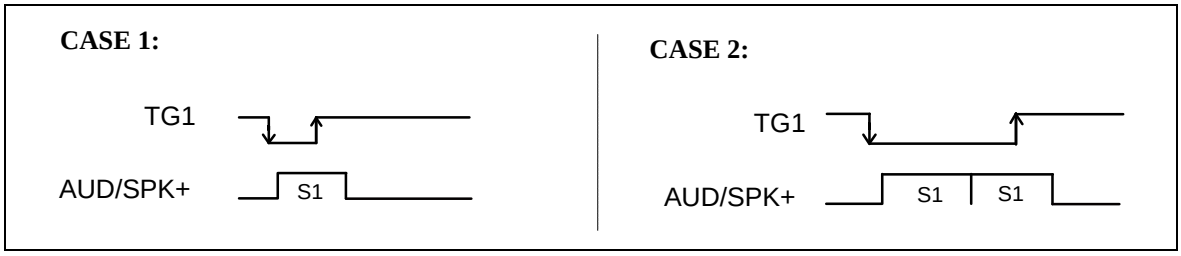
Timing diagram:



C. Completed Cycle Level Hold

```
0:                          ; TG1 falling edge interrupt vector
    LD EN0, 0x01            ; Enable TG1 falling edge input only
    H51+Sound1+T51
    JP 0 @TG1_LOW           ; If TG1 state is low, jump to 0
    END
```

Timing diagram:

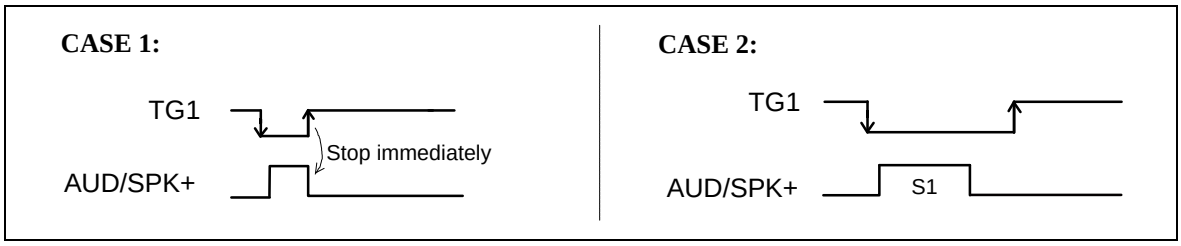


D. Single Cycle Level Hold

```
0:                          ; TG1 falling edge interrupt vector
  LD EN0, 0x11              ; Enable TG1 falling and rising edge input
  H51+Sound1+T51
  END
```

4:
END

Timing diagram:

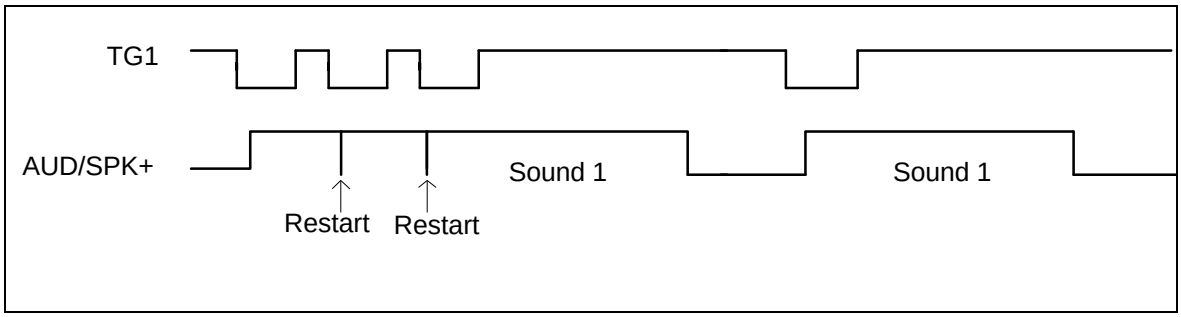


Retriggerable And Non-retriggerable Setting

A. Retriggerable

0:
LD EN0, 0x01
:
:
END

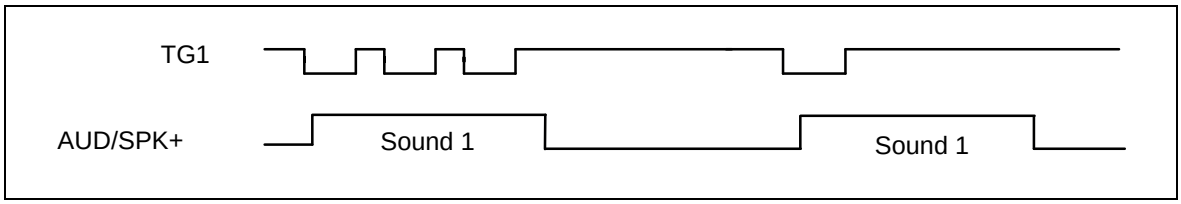
Timing diagram:



B. Non-Retriggerable

0:
LD EN0, 0x00
:
:
LD EN0, 0x11
END

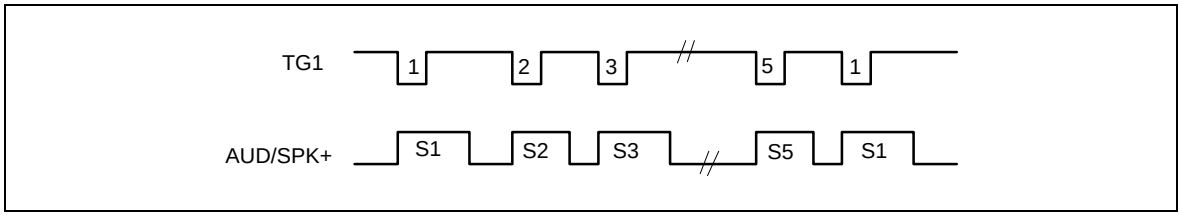
Timing diagram:



Serial Playing Mode (5 Segments)

```
W523S60
32:
    LD R0, 16
    LD EN0, 0x01
    END
0:
    JP R0
16:
    INC
    H51+S1+T51
    END
17:
    INC
    H51+S2+T51
    END
18:
    INC
    H51+S3+T51
    END
19:
    INC
    H51+S4+T51
    END
20:
    LD R0, 16
    H51+S5+T51
    END
```

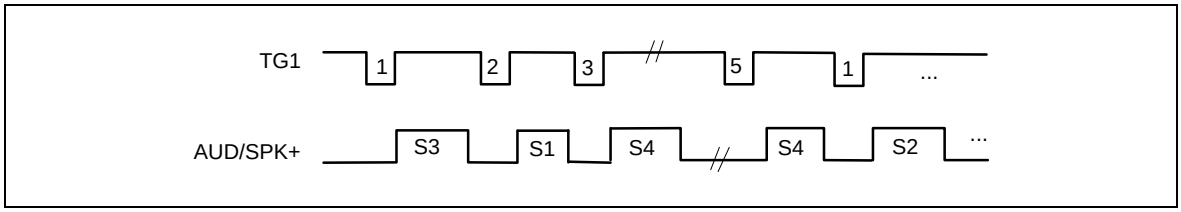
Timing diagram:



S/W Random (1)

```
W523S60
32:
    LD EN0, 0x01
    LD R0, 16
    END
0:
    LD EN0, 0x00
    JP R0
16:
    JP 26 @TG1_HIGH
17:
    JP 27 @TG1_HIGH
18:
    JP 28 @TG1_HIGH
19:
    JP 29 @TG1_HIGH
    JP 16
26:
    H51+S1+T51
    LD R0, 17
    JP 31
27:
    H51+S2+T51
    LD R0, 16
    JP 31
28:
    H51+S3+T51
    LD R0, 19
    JP 31
29:
    H51+S4+T51
    LD R0, 18
31:
    LD EN0, 0x01
    END
```

Timing diagram:

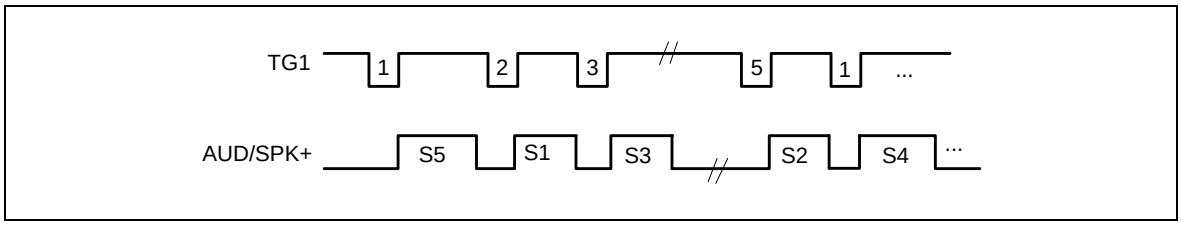


S/W Random (2)

```
W523S60
32:
    LD EN0, 0x11
    END
0:
    LD R0, 16
    [300]
    LD R0, 17
    [300]
    LD R0, 18
    [300]
    LD R0, 19
    [300]
    LD R0, 20
    [300]
    JP 0
4:
    JP R0
```

```
16:
    H51+S4+T51
    END
17:
    H51+S1+T51
    END
18:
    H51+S5+T51
    END
19:
    H51+S3+T51
    END
20:
    H51+S2+T51
    END
```

Timing diagram:



More Than One PAGE

```
W523S60
DEFPAGE 8                   ; select 8-page mode
OSC_1.5MHZ                  ; change oscillator frequency to 1.5 MHz
FREQ2                       ; sample rate 8 KHz

PAGE0                       ; declare page 0 start
21:                         ; label 21 of page 0
     H51+[3D00]+T51
     END
22:
    LD PAGE, 1              ; change page setting
    JP 21                   ; jump to label 21 in page 1 instead of page 0
255:
```

```
…
…
PAGE1                          ; declare page 1 start
21:                            ; label 21 of page 1
      H51+sound_11+T51
      END
19:
…
…
…
PAGE2                          ; declare page 2 start
…
…
```

Matrix Input Application

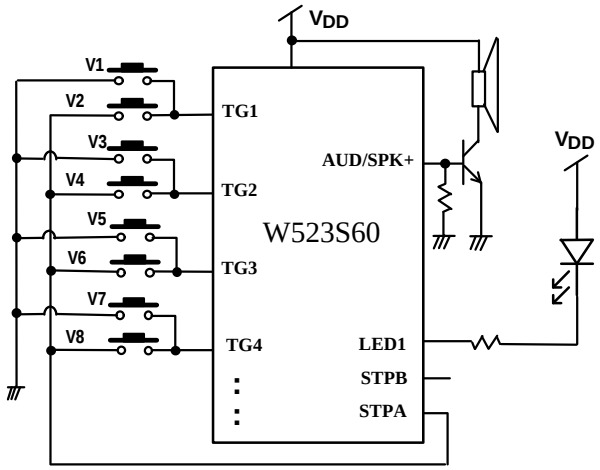
In this application, we use 4 trigger input pins and one output pin to organize the matrix with 8 inputs. User can follow this application to expand to more inputs by using more trigger input pins and output pins.

Program:

```
W583S40
32:
      LD STOP, 0x00            ; STPA set to low level
      LD EN0, 0x0F             ; One Shot play mode
      END
0:
      LD STOP, 0x01            ; STPA set to high level
      JP 18 @TG1_HIGH          ; check high
      H51+V1+T51               ; play V1
      LD STOP, 0x00            ; STPA set to low level
      END
18:                            ; pseudo trigger pin
      H51+V2+T51               ; play V2
      LD STOP, 0x00            ; STPA set to low level
      END
1:
      LD STOP, 0x01            ; STPA set to high level
      JP 19 @TG2_HIGH          ; check high
      H51+V3+T51               ; play V3
      LD STOP, 0x00            ; STPA set to low level
      END
19:                            ; pseudo trigger pin
      H51+V4+T51               ; play V4
      LD STOP, 0x00            ; STPA set to low level
      END
2:
      LD STOP, 0x01            ; STPA set to high level
      JP 20 @TG3_HIGH          ; check high
      H51+V5+T51               ; play V5
      LD STOP, 0x00            ; STPA set to low level
      END
20:                            ; pseudo trigger pin
```

```
        H51+V6+T51              ; play V6
        LD STOP, 0x00           ; STPA set to low level
        END
3:
        LD STOP, 0x01           ; STPA set to high level
        JP 21 @TG4_HIGH         ; check high
        H51+V7+T51              ; play V7
        LD STOP, 0x00           ; STPA set to low level
        END
21:                             ; pseudo trigger pin
        H51+V8+T51              ; play V8
        LD STOP, 0x00           ; STPA set to low level
        END
```

Application Circuit



Delay time: V1~V8: 2ms + debounce time

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	VDD - VSS	-	-0.3 - +7.0	V
Input Voltage	VIN	All Inputs	VSS-0.3 - VDD+0.3	V
Storage Temp.	TSTG	-	-55 - +150	°C
Operating Temp.	TOPR	-	0 - +70	°C

NOTE:
Operating the device under conditions beyond those indicated above may cause permanent damage or affect device reliability.

ELECTRICAL CHARACTERISTICS

(TA=25°C, VSS=0V, VDD=4.5V unless otherwise specified.)

DC PARAMETERS

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		2.4	3	5.5	V
Input Voltage	Vil		VSS-0.3	-	0.3×VDD	V
	Vih		0.7×VDD	-	VDD	
Standby Current	Isb1	VDD=3V, All I/O pins unconnected, No Playing			1	μA
	Isb2	VDD=5V, All I/O pins unconnected, No Playing			1	μA
Operating Current (Ring type)	IOP1	VDD=3V, No Load			500	μA
	IOP2	VDD=5V, No Load			1	mA
Operating Current (Crystal type)	IOP3	VDD=3V, No Load			600	μA
	IOP4	VDD=5V, No Load			1.2	mA
Input Current of TG1-TG8 pins	Iin1	VDD=3V, Vin=0V			-8	μA
Input Current of TEST pin	Iin2	VDD=3V, Vin=3V			50	μA
Input Current of SEL, /RESET and /DISOTP	Iin3	VDD=3V, Vin=0V			-8	μA
SPK (D/A Full Scale)	Idac	VDD=4.5V, Rl=100Ω	-4.0	-5.0	-6.0	mA
Output Current of STPA-STPH	IOL1	VDD=3V, Vout=0.4V	0.8			mA
	IOH1	VDD=3V, Vout=2.7V	-0.8			mA
Output Current of SPK+, SPK-	IOL2	VDD=3V, Rl=8Ω	100			mA
	IOH2		-100			mA
Output Current of WRP, RDP and DATA	IOL3	VDD=3V, Vout=0.4V	0.8			mA
	IOH3	VDD=3V, Vout=2.7V	-0.8			mA

AC PARAMETERS

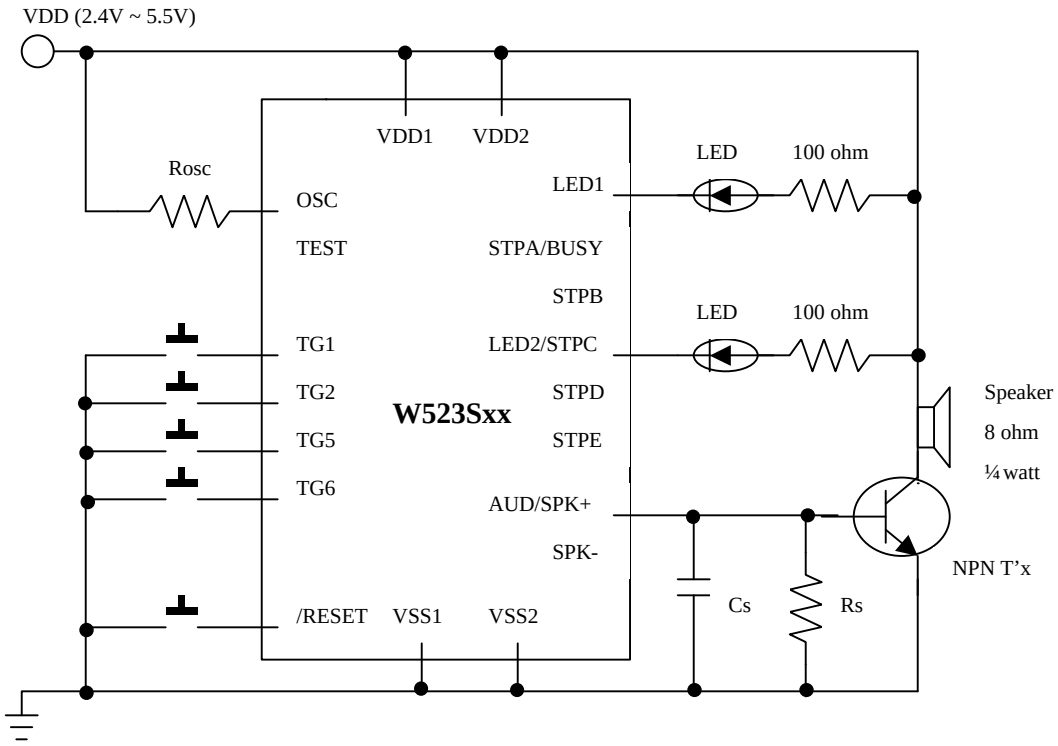
ITEM	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation Frequency (ICE chip W58300)	Fosc1	Ring oscillator, Rosc=270KΩ	2.7	3	3.3	MHz
		Ring oscillator, Rosc=560KΩ	1.3	1.5	1.7	
Oscillation Frequency (Production chip	Fosc2	Ring oscillator, Rosc=750KΩ	2.7	3	3.3	MHz
		Ring oscillator,	1.3	1.5	1.7	

W523Sxx)		Rosc=1.6MΩ				
Oscillation Frequency Deviation by Voltage Drop	ΔFosc / Fosc	F(3V)-F(2.4V) / F(3V)			7.5	%
Instruction Cycle Time	Tins	Fosc = 3 MHz, SR = 6 KHz		1/3		mS
POI Delay Time	TPD			160		mS
Long Debounce Time	TDEBL	Fosc = 3 MHz, SR = 6 KHz	50			mS
Short Debounce Time[1]	TDEBS		400			µS

1. For ring oscillator only.

Typical application circuit

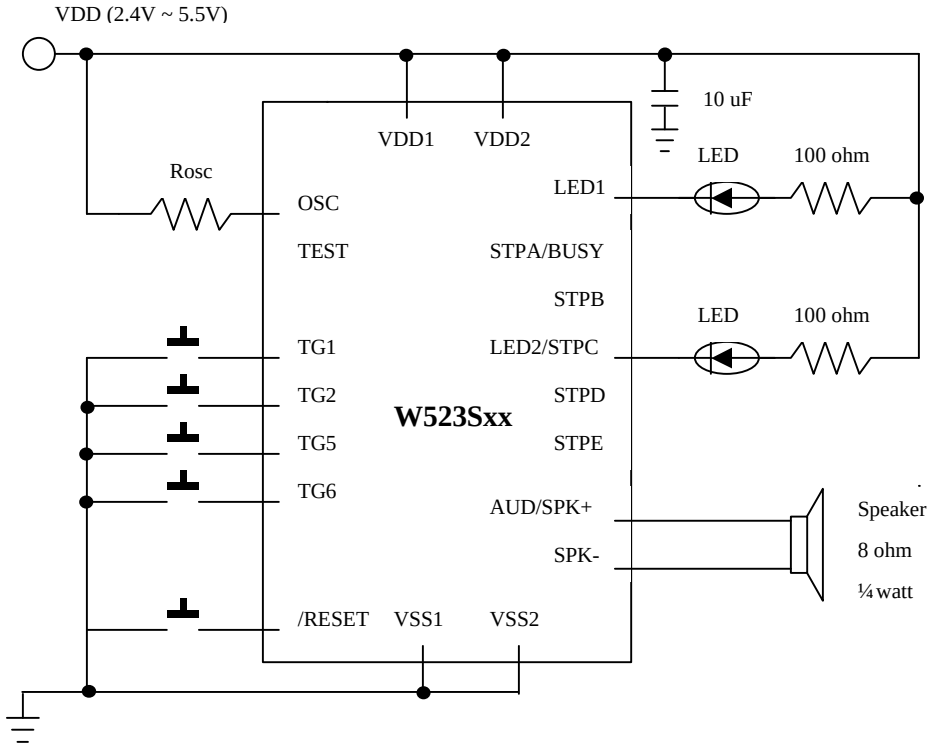
1. DAC output:



Note:
1. In principle, the playing speed determined by Rosc should correspond to the sampling rate during the coding phase. The playing speed may be adjusted by varing Rosc, however.
2. Rs is an optional current-dividing resistor. If Rs is added, the resistance should be between 390 and 820 ohm.
3. The typical Rosc = 1.2 Mohm for 3 MHz Fosc; and Rosc = 2.4 Mohm for 1.5 MHz Fosc.
4. Cs is optional.
5. The DC current gain of the NPN transistor ranges from 120 to 200.
6. All unused trigger pins can be left open because of their internal pull-high resistance.

7. The OSC layout in customer's PCB should be as closed as the OSC pad to avoid noise coupling.
8. The chip's substrate must be wired to Vss.

2. PWM output:



Note:
1. In principle, the playing speed determined by Rosc should correspond to the sampling rate during the coding phase. The playing speed may be adjusted by varing Rosc, however.
2. The typical Rosc = 1.2 Mohm for 3 MHz Fosc; and Rosc = 2.4 Mohm for 1.5 MHz Fosc.
3. All unused trigger pins can be left open because of their internal pull-high resistance.
4. The OSC layout in customer's PCB should be as closed as the OSC pad to avoid noise coupling.
5. The chip's substrate must be wired to Vss.

REFERENCE TABLE OF RESISTOR FOR RING OSCILLATOR

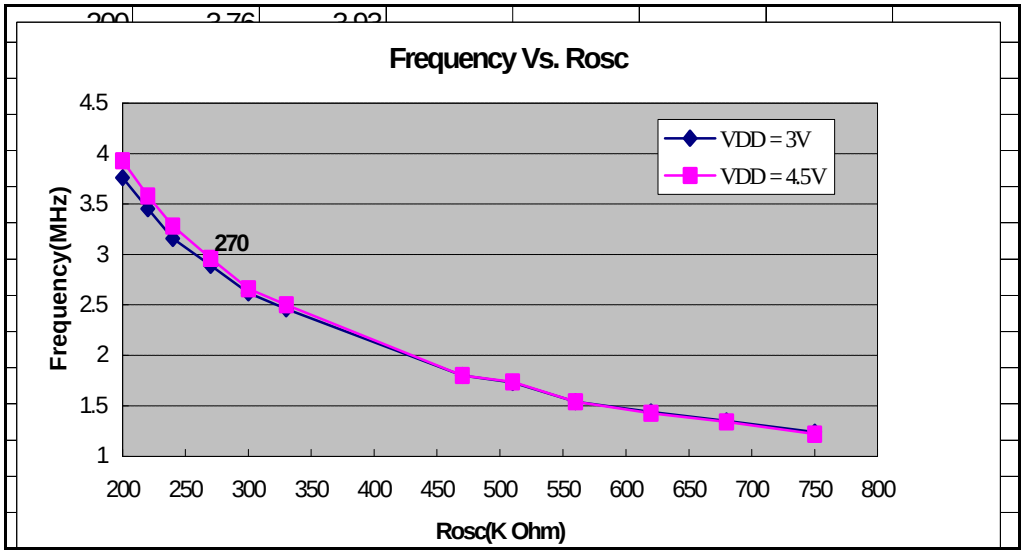
W58300 ICE chip	W523Sxx Production chip	Fosc@4.5V
220 KΩ	620 KΩ	
240 KΩ	680 KΩ	3MHz more
270 KΩ	750 KΩ	typical 3MHz
300 KΩ	820 KΩ	3MHz less
330 KΩ	910 KΩ	
510 KΩ	1.4 MΩ	1.5MHz more
560KΩ	1.6 MΩ	typical 1.5 MHz
620KΩ	1.8 MΩ	1.5MHz less

Oscillation resistor value (Rosc) for W523Sxx Series

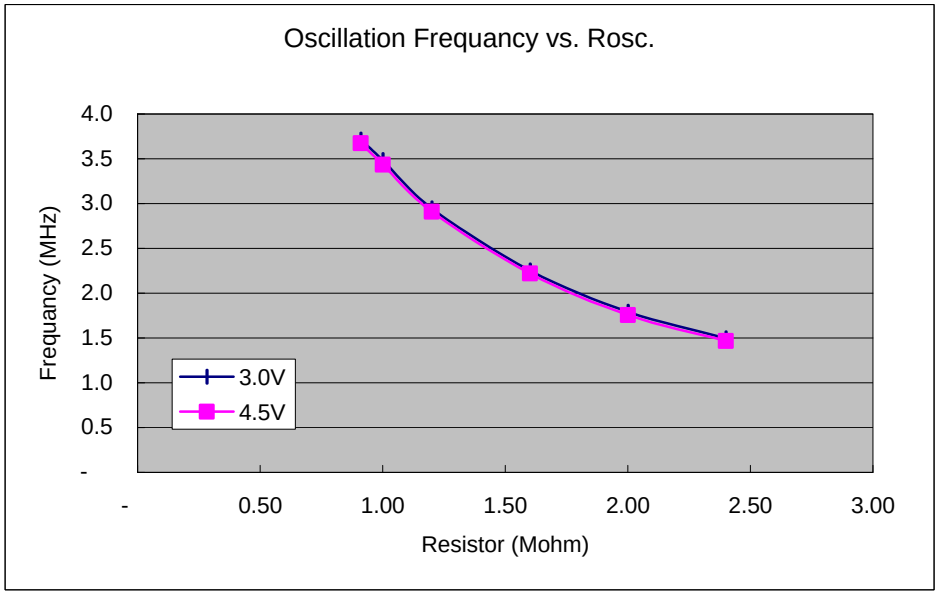
Part No.	Fosc	Supply Voltage	Typical Rosc
W58300 ICE	3MHz	3V or 4.5V	270KΩ
	1.5MHz	3V or 4.5V	560KΩ
W523S10	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S15	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S20	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S25	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S30	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S40	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S50	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S60	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S80	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523S99	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ
W523M02	3MHz	3V or 4.5V	1.2MΩ
	1.5MHz	3V or 4.5V	2.4MΩ

Relationship between Rosc and System Clock at Fixed Supply Voltage

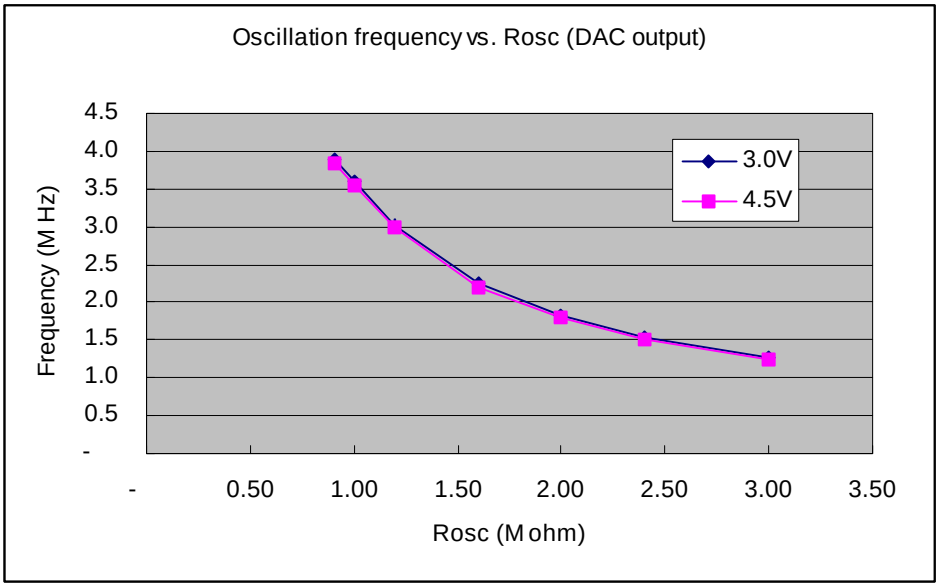
W58300 ICE Chip



W523S08, W523S10

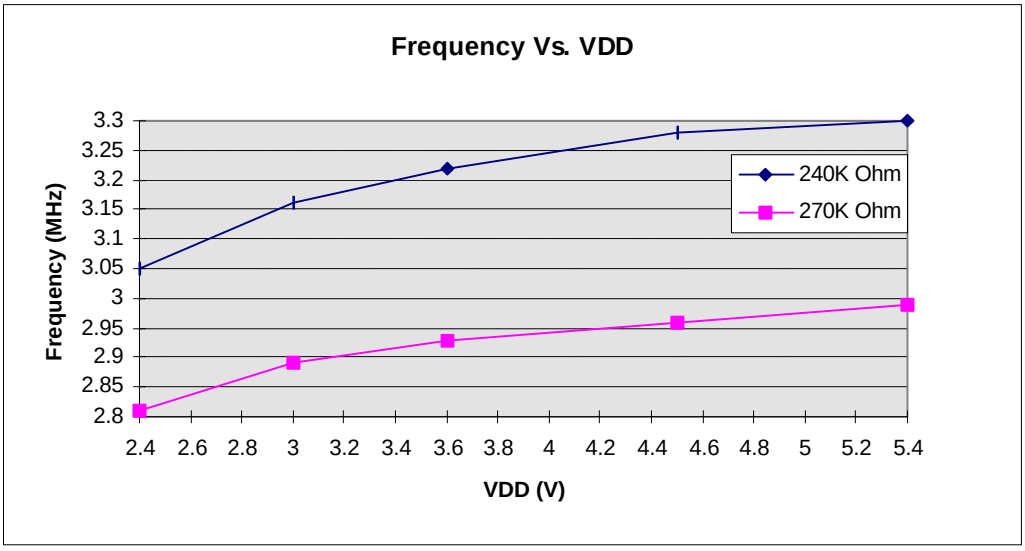


W523S12, W523S15

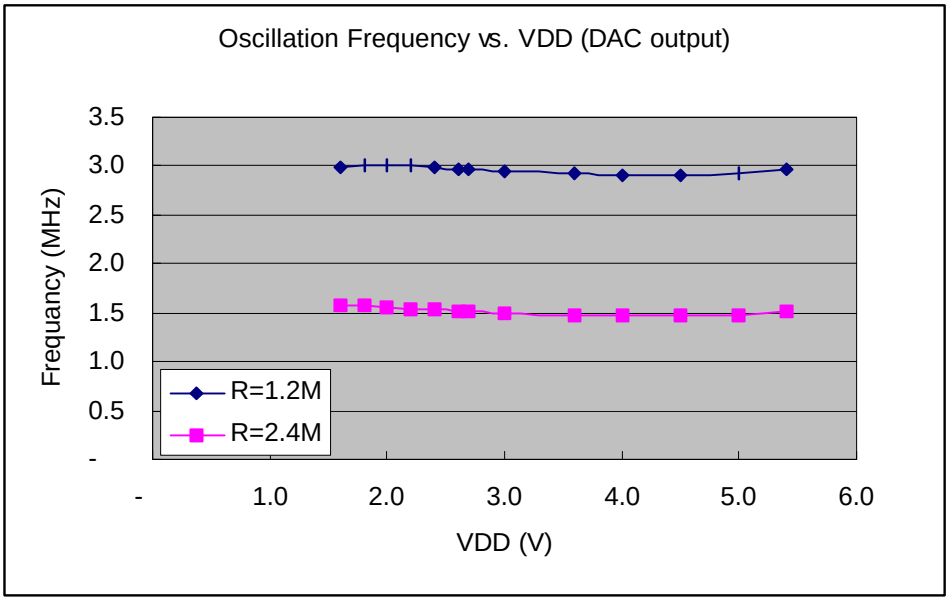


Relationship between Supply Voltage and System Clock at Fixed Rosc

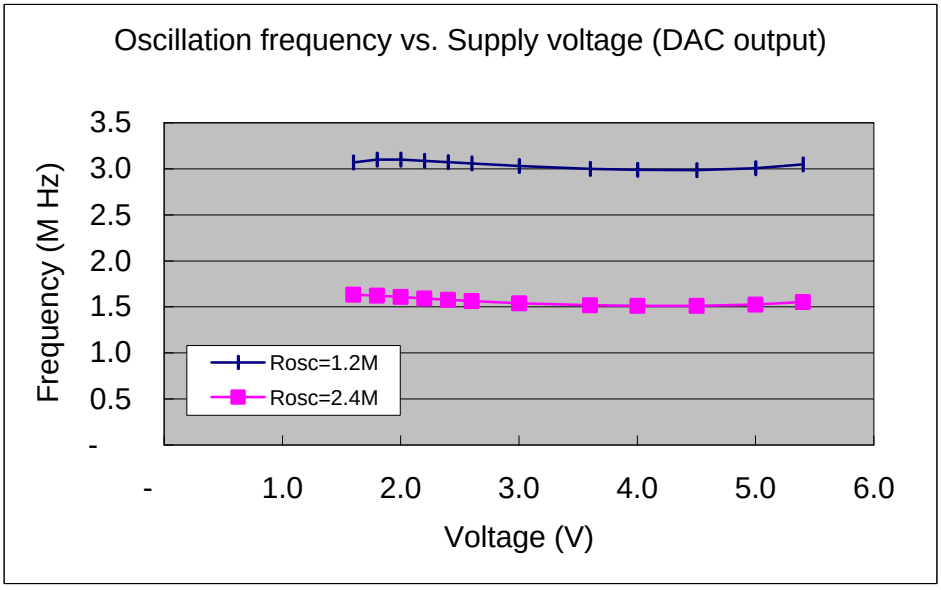
W58300 ICE Chip



W523S08, W523S10



W523S12, W523S15



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