NCP803

Very Low Supply Current 3-Pin Microprocessor Reset Monitor

The NCP803 is a cost–effective system supervisor circuit designed to monitor V_{CC} in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 10 μsec of V_{CC} falling through the reset voltage threshold. Reset is maintained active for a minimum of 140 msec after V_{CC} rises above the reset threshold. The NCP803 has an open drain active–low $\overline{\text{RESET}}$ output. The output of the NCP803 is guaranteed valid down to V_{CC} = 1.0 V and is available in a SOT–23 package.

The NCP803 is optimized to reject fast transient glitches on the V_{CC} line. Low supply current of 1.0 μA (V_{CC} = 3.2 V) make this device suitable for battery powered applications.

Features

- Precision V_{CC} Monitor for 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.6 V to 4.9 V Available in 100 mV Steps
- 140 msec Guaranteed Minimum $\overline{\text{RESET}}$ Output Duration
- $\overline{\text{RESET}}$ Output Guaranteed to V_{CC} = 1.0 V
- Low 1.0 μA Supply Current
- V_{CC} Transient Immunity
- Small SOT–23 Package
- No External Components
- Wide Operating Temperature: –40°C to 105°C

Typical Applications

- Computers
- Embedded Systems
- Battery Powered Equipment
- Critical μP Power Supply Monitoring

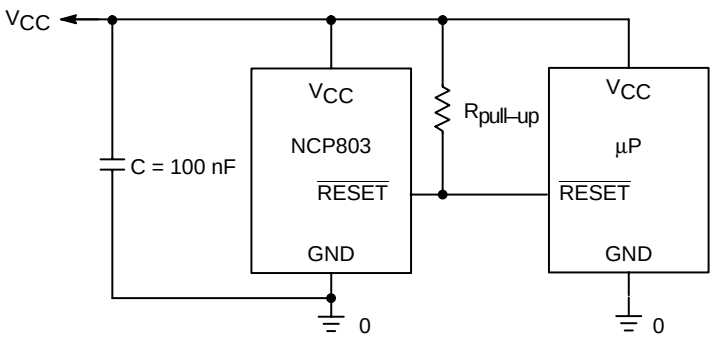
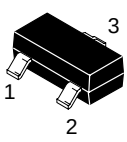


Figure 1. Typical Application Diagram

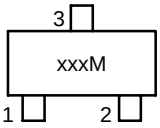
ON Semiconductor™

http://onsemi.com

MARKING DIAGRAM

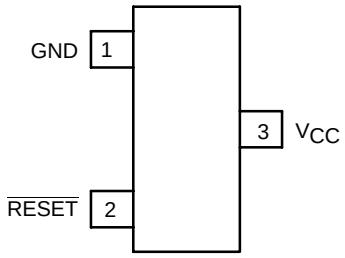


SOT–23 (TO–236) CASE 318



xxx = Specific Device Code
M = Monthly Date Code

PIN CONFIGURATION



SOT–23*
(Top View)

NOTE: *SOT–23 is equivalent to JEDEC (TO–236)

ORDERING INFORMATION

Device	Package	Shipping
NCP803SNxxxT1	SOT–23	3000/Tape & Reel

NOTE: The "xxx" denotes a suffix for V_{CC} voltage threshold options – see page 6 for more details.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

ABSOLUTE MAXIMUM RATINGS* (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to GND)	V_{CC}	6.0	V
$\overline{RESET}$		–0.3 to (V_{CC} + 0.3)	V
Input Current, V_{CC}		20	mA
Output Current, $\overline{RESET}$		20	mA
dV/dt (V_{CC})		100	V/μsec
Thermal Resistance, Junction to Air	$R_{\theta JA}$	491	°C/W
Operating Temperature Range	T_A	–40 to +105	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{sol}	+260	°C
Latch–up performance: Negative	$I_{Latch–up}$	150	mA

*Maximum Ratings are those values beyond which damage to the device may occur.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per MIL–STD–883, Method 3015.
   Machine Model Method 400 V.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150°C$$

ELECTRICAL CHARACTERISTICS T_A = –40°C to +105°C unless otherwise noted. Typical values are at T_A = +25°C. (Note 3)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Range					V
T_A = 0°C to +70°C		1.0	–	5.5	
T_A = –40°C to +105°C		1.2	–	5.5	
Supply Current	I_{CC}				μA
V_{CC} = 3.3 V					
T_A = –40°C to +85°C		–	0.5	1.2	
T_A = 85°C to +105°C		–	–	2.0	
V_{CC} = 5.5 V					
T_A = –40°C to +85°C		–	0.8	1.8	
T_A = 85°C to +105°C		–	–	2.5	
Reset Threshold (Note 4)	V_{TH}				V
NCP803SN308					
T_A = +25°C		3.04	3.08	3.11	
T_A = –40°C to +85°C		3.00	–	3.15	
T_A = +85°C to +105°C		2.92	–	3.23	
NCP803SN293					
T_A = +25°C		2.89	2.93	2.96	
T_A = –40°C to +85°C		2.85	–	3.00	
T_A = +85°C to +105°C		2.78	–	3.08	
NCP803SN263					
T_A = +25°C		2.59	2.63	2.66	
T_A = –40°C to +85°C		2.55	–	2.70	
T_A = +85°C to +105°C		2.50	–	2.76	

3. Production testing done at T_A = 25°C, over temperature limits guaranteed by design.
4. Contact your ON Semiconductor sales representative for other threshold voltage options.

ELECTRICAL CHARACTERISTICS (continued) T_A = –40°C to +105°C unless otherwise noted. Typical values are at T_A = +25°C. (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
Reset Temperature Coefficient		–	30	–	ppm/°C
V_{CC} to Reset Delay V_{CC} = V_{TH} to (V_{TH} – 100 mV)		–	10	–	μsec
Reset Active Timeout Period		140	240	460	msec
$\overline{\text{RESET}}$ Output Voltage Low V_{CC} = V_{TH} – 0.2 V 1.6 V ≤ V_{TH} ≤ 2.0 V, I_{SINK} = 0.5 mA 2.1 V ≤ V_{TH} ≤ 4.0 V, I_{SINK} = 1.2 mA 4.1 V ≤ V_{TH} ≤ 4.9 V, I_{SINK} = 3.2 mA	V_{OL}	–	–	0.3	V
$\overline{\text{RESET}}$ Leakage Current V_{CC} > V_{TH}, $\overline{\text{RESET}}$ De–asserted	I_{LEAK}	–	–	1	μA

5. Production testing done at T_A = 25°C, over temperature limits guaranteed by design.

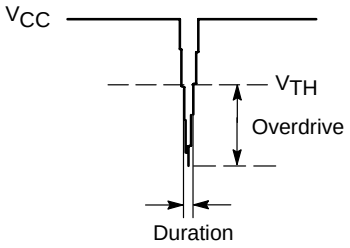
PIN DESCRIPTION

Pin No.	Symbol	Description
1	GND	Ground
2	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ output remains low while V_{CC} is below the reset voltage threshold, and for 240 msec (typ.) after V_{CC} rises above reset threshold.
3	V_{CC}	Supply Voltage: C = 100 nF is recommended as a bypass capacitor between V_{CC} and GND.

APPLICATIONS INFORMATION

V_{CC} Transient Rejection

The NCP803 provides accurate V_{CC} monitoring and reset timing during power–up, power–down, and brownout/sag conditions, and rejects negative–going transients (glitches) on the power supply line. Figure 2 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. Any combination of duration and overdrive which lies **under** the curve will **not** generate a reset signal. Combinations above the curve are detected as a brownout or power–down. Typically, transient that goes 100 mV below the reset threshold and lasts 5 μs or less will not cause a reset pulse. Transient immunity can be improved by adding a capacitor in close proximity to the V_{CC} pin.



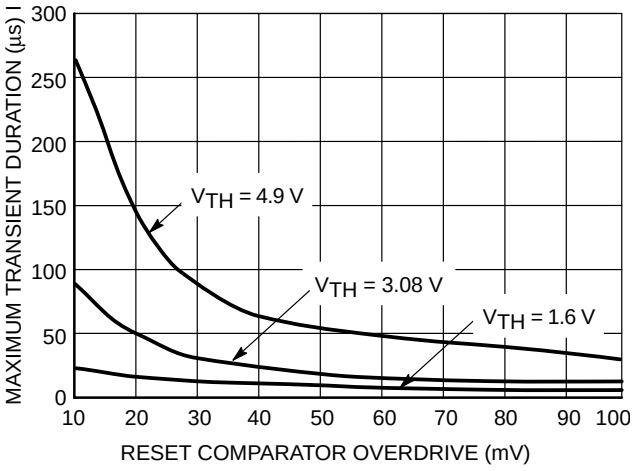


Figure 2. Maximum Transient Duration vs. Overdrive for Glitch Rejection at 25°C

Processors With Bidirectional I/O Pins

Some μP's (such as Motorola 68HC11) have bi–directional reset pins which interface easily with the Open Drain $\overline{\text{RESET}}$ output of the NCP803. As shown in Figure 3, one can connect directly to the $\overline{\text{RESET}}$ output of the NCP803 to the $\overline{\text{RESET}}$ pin of the μP. The pull–up resistor avoids an undetermined voltage of the $\overline{\text{RESET}}$ pin.

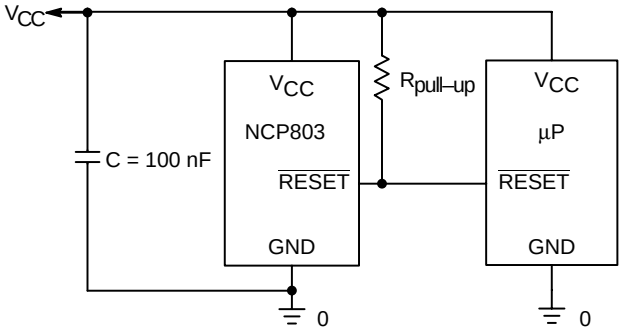


Figure 3. Interfacing to Bidirectional Reset I/O

NCP803 $\overline{\text{RESET}}$ Output Allows Use With Two Power Supplies

In numerous applications the pull–up resistor placed on the $\overline{\text{RESET}}$ output is connected to the supply voltage monitored by the IC. Nevertheless, a different supply voltage can also power this output and so level–shift from the monitored supply to reset the μP. However, if the NCP803's supply goes below 1 V, the $\overline{\text{RESET}}$ output ability to sink current will decrease and the result is a high state on the pin even though the supply's IC is under the threshold level. This occurs at a V_{CC} level that depends on the $R_{pull–up}$ value and the voltage to which it is connected.

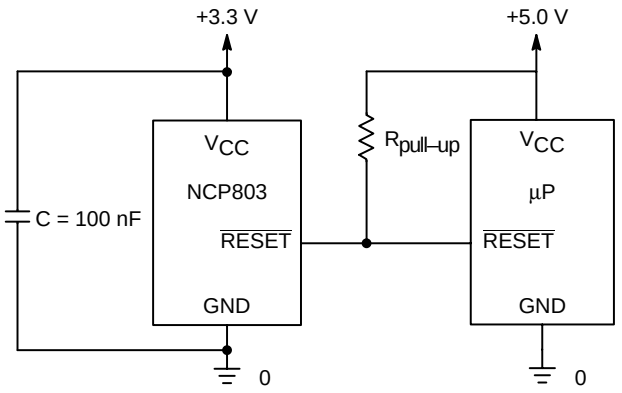


Figure 4. $\overline{\text{RESET}}$ Output with Two Power Supplies

TYPICAL CHARACTERISTICS

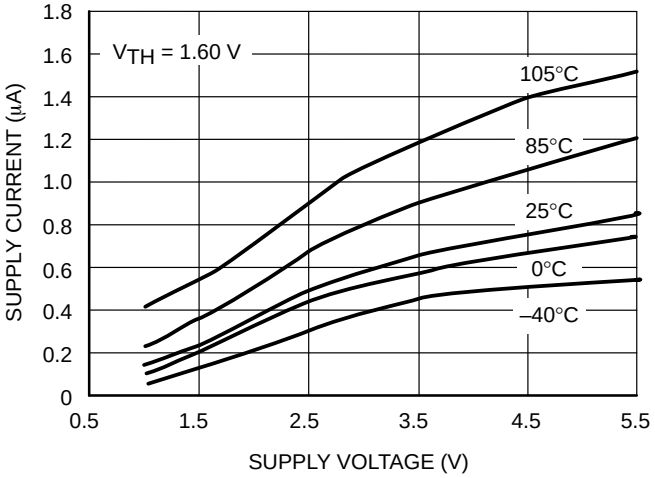


Figure 5. Supply Current vs. Supply Voltage

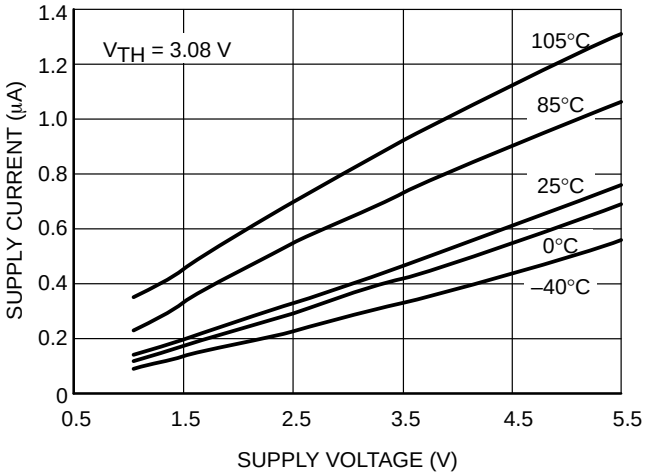


Figure 6. Supply Current vs. Supply Voltage

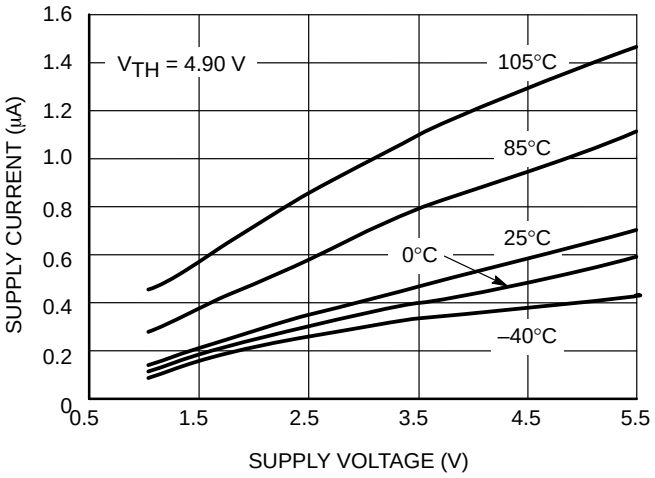


Figure 7. Supply Current vs. Supply Voltage

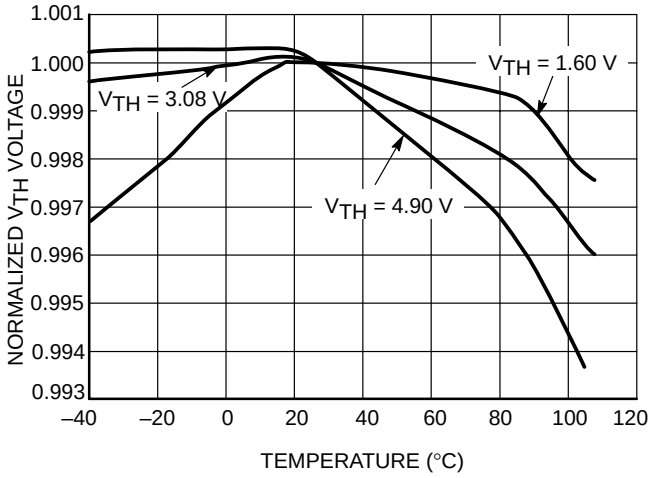


Figure 8. Normalized Reset Threshold Voltage vs. Temperature

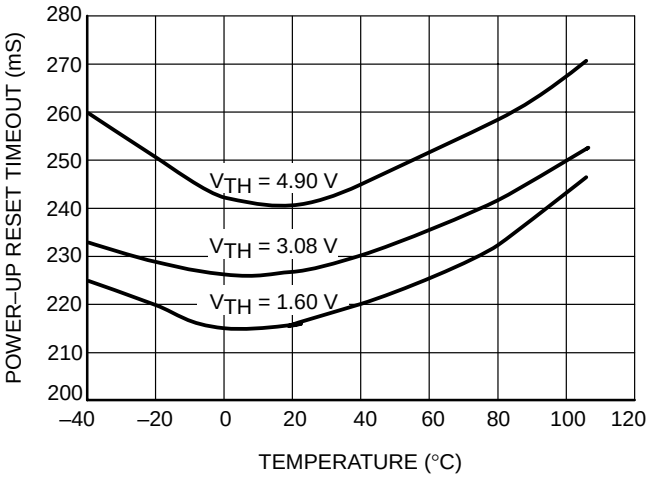


Figure 9. Power–up Reset Timeout vs. Temperature

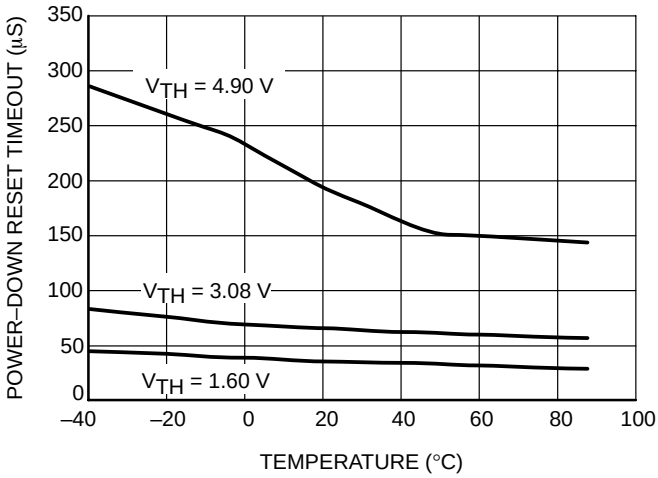
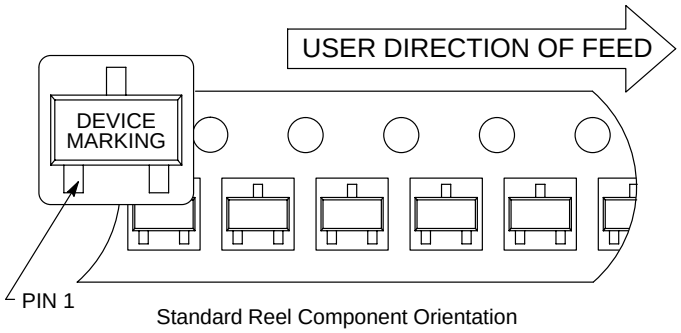


Figure 10. Power–down Reset Timeout vs. Temperature (Overdrive = 20 mV)

TAPING FORM

Component Taping Orientation for 3L SOT−23 (JEDEC−236) Devices



Standard Reel Component Orientation
(Mark Right Side Up)

Tape & Reel Specifications Table

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SOT−23	8 mm	4 mm	3000	7 inches

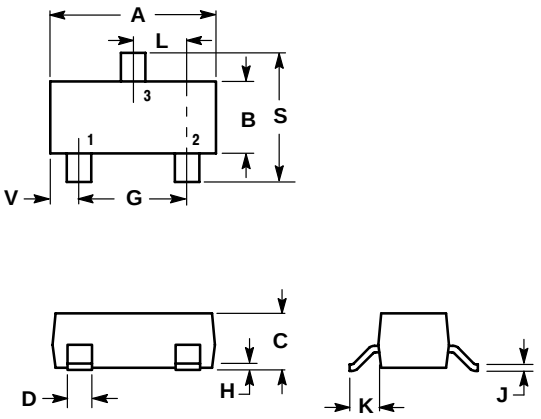
MARKING AND THRESHOLD INFORMATION

ON Semiconductor Part #	V_{TH}*	Marking (Note 6)
NCP803SN263T1	2.63	SQCM
NCP803SN293T1	2.93	SQDM
NCP803SN308T1	3.08	SQEM

*Contact your ON Semiconductor sales representative for other threshold voltage options.
6. M = Monthly Date Code

PACKAGE DIMENSIONS

SOT–23
PLASTIC PACKAGE (TO–236)
CASE 318–08
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318–03 AND –07 OBSOLETE, NEW STANDARD 318–08.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
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Phone: 81–3–5740–2700
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ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.