

SED1330

CMOS GRAPHIC LCD CONTROLLER

This part is replaced by SED1335. Some pin differences between SED1330 and SED1335 exist. Please check SED1335 data sheet. S-MOS Systems, Inc., will continue to support existing designs which use SED1330.

■ DESCRIPTION

The SED1330 is a CMOS low-power dot matrix liquid crystal graphic display controller. The device stores in external RAM display data sent by an 8-bit microcomputer, and generates all the signals required by the LCD drivers. The LSI incorporates an internal character generator ROM which supports user-defined characters (also an external CGROM can be supported).

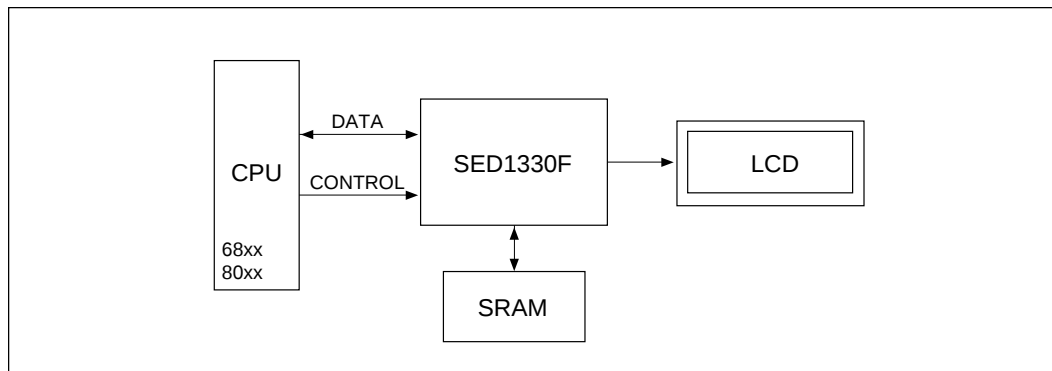
The SED1330 can be interfaced to high-speed microprocessors such as the Intel family or Motorola family. The controller supports a set of rich commands that will allow the user to create a layered display of characters and graphics.

Also, the controller functions as a pipeline buffer between the MPU and display memory so that low-cost, medium-speed SRAM can be used.

■ FEATURES

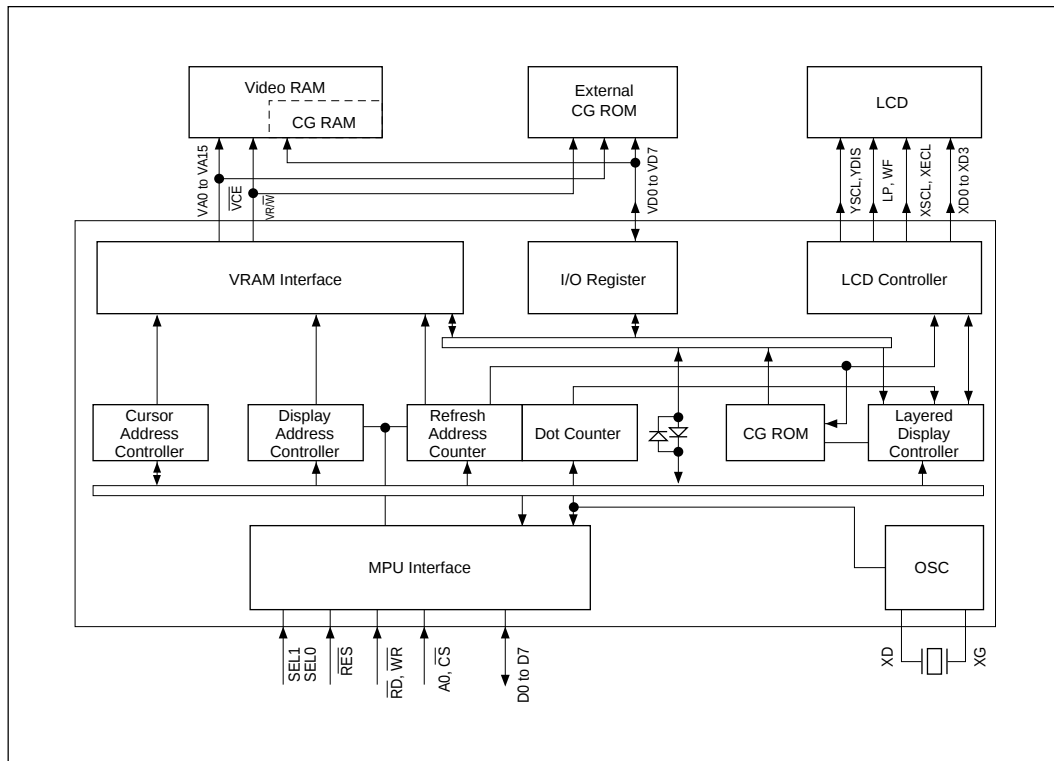
- CMOS low-power graphic and character display controller
- Selectable MPU interface is compatible with both the Intel family and the Motorola family
- Smooth scrolling support:
Horizontal and vertical scroll
Scrolling of selected areas of the display
- Multimode display:
2 layers of overlapping character and graphics
3 layers of overlapping graphics
- Selectable display synthesis:
Inverse video
Flashing display, cursor on/off/blink
Under and bar cursor, block cursor
Simple animation
- Programmable cursor
- Internal character generator ROM
- Supports external character generator ROM:
8 × 8 or 8 × 16 pixel characters
Allows mixing of ROM and RAM character sets
- Supports 64K bytes of memory:
2 of 32K × 8 100ns SRAM
or 8 of 8K × 8 100ns SRAM
- Display duty 1/2 to 1/256
- Low power dissipation 5mA (typical)
0.05μA (typical), standby
- Logic power supply 4.5 to 5.5V
- Package Plastic QFP5-60 pin (FBA)
Plastic QFP6-60 pin (FBB)

■ SYSTEM BLOCK DIAGRAM

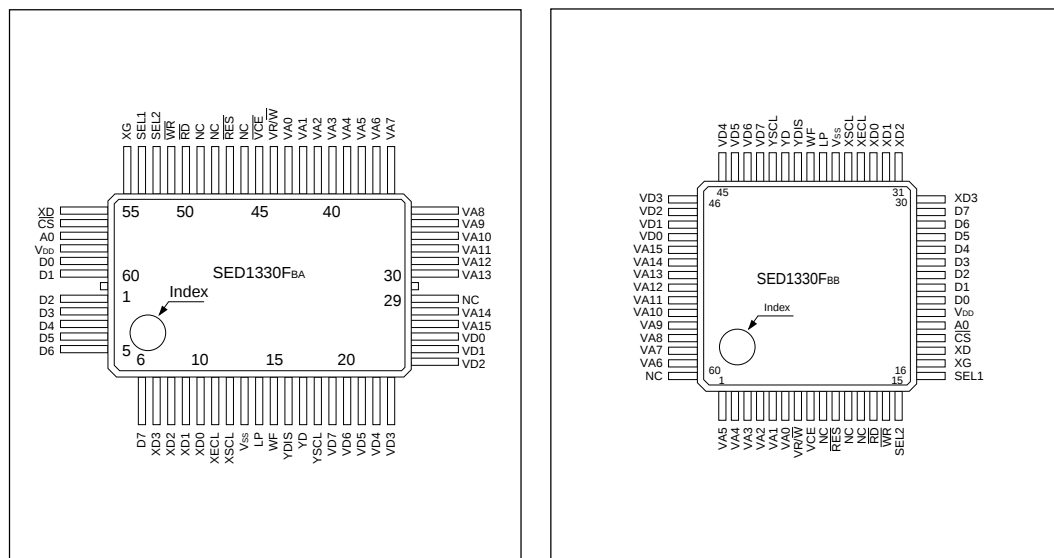


SED1330

■ BLOCK DIAGRAM



■ PINOUT



■ PIN DESCRIPTIONS

Pin Name	Pin No.		I/O	Functions
	SED1330FBA	SED1330FBB		
XG	54	17	I	Oscillator terminal
XD	55	18	O	Oscillator terminal
V _{DD}	58	21	+5V	Power supply
V _{SS}	13	36	GND (0V)	Power supply
SEL1, 2	53 • 52	16 • 15	I	MPU interface format selection
D0 to D7	59 to 60 1 to 6	22 to 29	I/O	Data bus
A0	57	20	I	Data type selection
$\overline{\text{RD}}$	50	13	I	80 series Read strobe signal 68 series "E" clock
$\overline{\text{WR}}$	51	14	I	80 series Write strobe signal 68 series R/W signal
$\overline{\text{CS}}$	56	19	I	Chip select
$\overline{\text{RES}}$	47	10	I	Reset
VA0 to VA15	43 to 30 28 to 27	6 to 1 59 to 50	O	VRAM address bus
VD0 to VD7	26 to 19	49 to 42	I/O	VRAM data bus
$\overline{\text{VRW}}$	44	7	O	VRAM R/W signal
$\overline{\text{VCE}}$	45	8	O	Memory control signal
XD0 to XD3	10 to 7	33 to 30	O	Dot data output bus to X driver
XSCL	12	35	O	Dot data shift clock for X driver
XECL	11	34	O	Chip enable shift clock for Y driver
LP	14	37	O	Dot data latch pulse
WF	15	38	O	Frame signal
YSCL	18	41	O	Scan data shift clock for Y driver
YD	17	40	O	Scan data output
YDIS	16	39	O	Power down signal when display OFF

NC: No Connection

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	−0.3 to 7.0	V
Input voltage	V _I	−0.5 to V _{DD} +0.5	V
Power dissipation	P _D	300	mW
Operating temperature	T _{opr}	−20 to 75	°C
Storage temperature	T _{stg}	−60 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s (at lead)	—

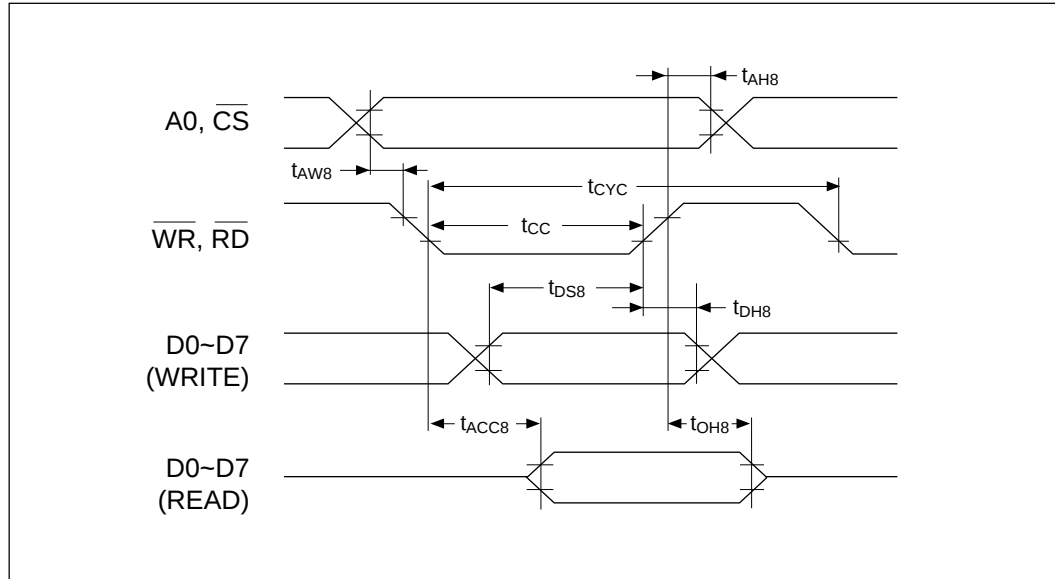
● DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V±10%, V_{SS} = 0V, T_a = -20 to 75°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Operating voltage		V _{DD}		4.5	5.0	5.5	V
Register data retention voltage		V _{OH}		2.0	—	6.0	V
T T L	High level input voltage	V _{IHT}	D0 to D7, A0, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$,	2.2	—	V _{DD} +0.3	V
	Low level input voltage	V _{ILT}	VD0 to VD7, I _{OH} = -5.0mA,	-0.3	—	0.8	V
	High level output voltage	V _{OHT}	I _{OL} = 5.0mA, $\overline{\text{VR}}/\overline{\text{W}}$, $\overline{\text{VCE}}$,	2.4	—	—	V
	Low level output voltage	V _{OLT}	$\overline{\text{REF}}$	—	—	0.4	V
C M O S	High level input voltage	V _{IHC}	I _{OH} = 1.6mA, I _{OL} = -1.6mA,	0.8V _{DD}	—	—	V
	Low level input voltage	V _{ILC}	SEL1, 2, SYNC, YD, XD0 to	—	—	0.2V _{DD}	V
	High level output voltage	V _{OHC}	XD3, XSCL, XECL, LP, FR,	V _{DD} -0.4	—	—	V
	Low level output voltage	V _{OLC}	YSCL, YDIS, OSC1, OSC2	—	—	0.4	V
SCHMITT	Positive trigger threshold voltage	V _{T+}	$\overline{\text{RES}}$ *	0.5V _{DD}	0.7V _{DD}	0.8V _{DD}	V
	Negative trigger threshold voltage	V _{T-}		0.2V _{DD}	0.3V _{DD}	0.5V _{DD}	V
Input leakage current		I _{LI}	V _I = V _{DD} or V _{SS}	—	0.05	2.0	μA
Output leakage current		I _{LO}		—	0.10	5.0	μA
Average operating current		I _{DDA}	f _{osc} = 10MHz, No load (No external V-RAM)	—	8	12	mA
Standby current		I _{DDS}	XG = $\overline{\text{CS}}$ = V _{DD}	—	0.05	20	μA
Oscillation frequency		f _{OSC}	AT X'tal XG, XD	1.0	—	10.0	MHz
External clock frequency		f _{CLK}		—	—	10.0	MHz
Feed back resistance		R _f		0.5	1.0	5.0	MΩ

* $\overline{\text{RES}}$ input pulse should be longer than 1.0ms.VL5 should be OFF when $\overline{\text{RES}}$ is "L".

- AC CHARACTERISTICS
 - System Bus READ/WRITE Timing I (8080)

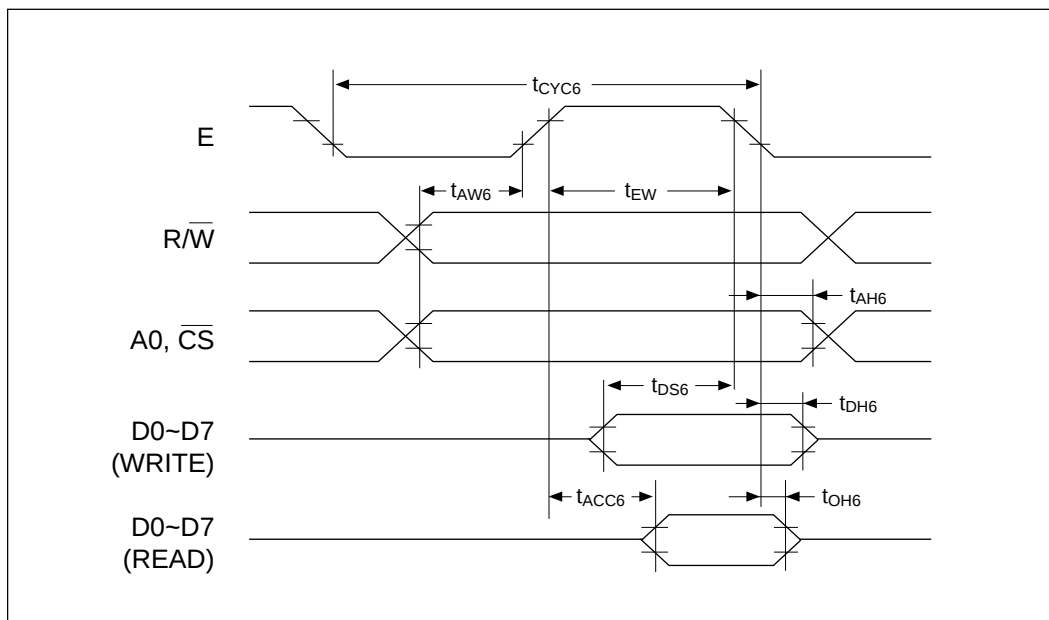


Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
A0, $\overline{CS}$	Address hold time	tAH8	10	—	ns	CL = 100 pF + 1TTL
	Address setup time	tAW8	30	—	ns	
$\overline{WR}$, $\overline{RD}$	System cycle time	tCYC	*1	—	ns	
	Control pulse width	tCC	220	—	ns	
D0 to D7	Data setup time	tDS8	120	—	ns	
	Data hold time	tDH8	10	—	ns	
	$\overline{RD}$ access time	tACC8	—	120	ns	
	Output disable time	tOH8	10	50	ns	

*1. tCYC = 2t_b + tCC + tCEA + 75 > tACV + 245 Memory control/movement control commands.

= 4t_b + tCC + 30 All other commands.

○ System Bus READ/WRITE Timing II (6800)



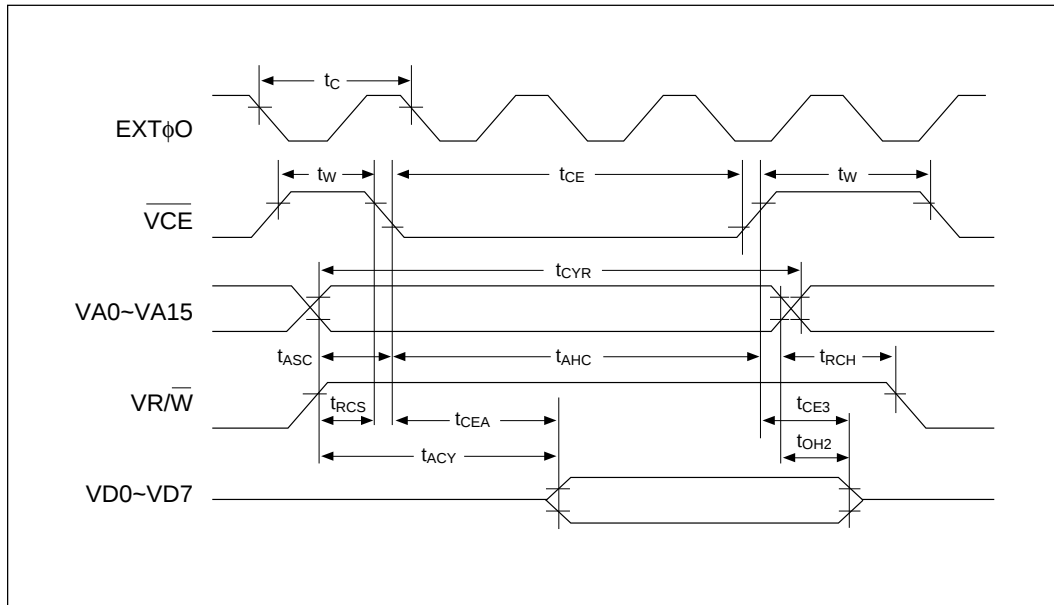
Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
A0, $\overline{CS}$, R/W	System cycle time	t_{CYC6}^{*1}	*2	—	ns	CL = 100 pF + 1 TTL
	Address setup time	t_{AW6}	30	—	ns	
	Address hold time	t_{AH6}	10	—	ns	
D0 to D7	Data setup time	t_{DS6}	120	—	ns	
	Data hold time	t_{DH6}	10	—	ns	
	Output disable time	t_{OH6}	10	50	ns	
	Access time	t_{ACC6}	—	120	ns	
E	Enable pulse width	t_{EW}	220	—	ns	

*1. t_{CYC6} means a cycle of ($\overline{CS.E}$) not E alone.

*2. $t_{CYC6} = 2t_c + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$ Memory control/movement control commands.

= $4t_c + t_{EW} + 30$ All other commands.

◦ Display Memory READ Timing



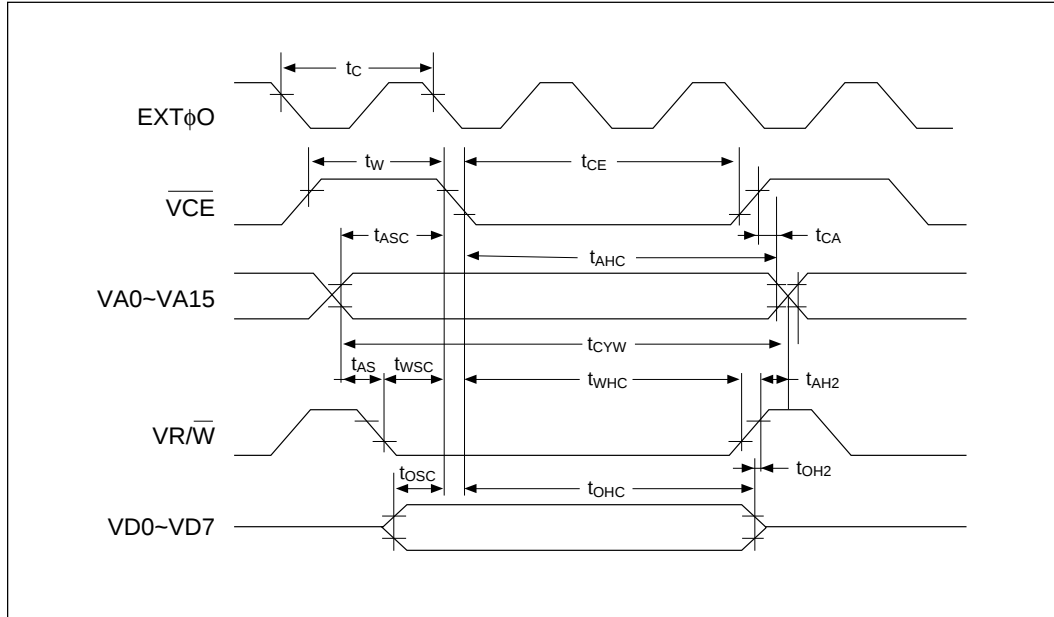
Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT φ0	Clock cycle	t_c	100	—	ns	CL = 100 pF + 1TTL
$\overline{VCE}$	$\overline{VCE}$ high-level pulse width	t_w	$t_c - 40$	—	ns	
	$\overline{VCE}$ low-level pulse width	t_{CE}	$2t_c - 40$	—	ns	
VA0 to VA15	Read cycle time	t_{CYR}	*1	—	ns	
	$\overline{VCE}$ address setup time (fall)	t_{ASC}	$t_c - 45$	—	ns	
	$\overline{VCE}$ address hold time (fall)	t_{AHC}	$2t_c - 40$	—	ns	
$VR/\overline{W}$	$\overline{VCE}$ read cycle setup time (fall)	t_{RCS}	$t_c - 45$	—	ns	
	$\overline{VCE}$ read cycle hold time (fall)	t_{RCH}	$t_c/2 - 35$	—	ns	
VD0 to VD7	Address access time	t_{ACV}	—	*2	ns	
	$\overline{VCE}$ access time	t_{CEA}	—	*3	ns	
	Output data hold time	t_{OH2}	0	—	ns	
	$\overline{VCE}$ data off time	t_{CE3}	0	—	ns	

*1. $t_{CYR} = 3t_c$

*2. $t_{ACV} = 3t_c - 120$

*3. $t_{CEA} = 2t_c - 120$

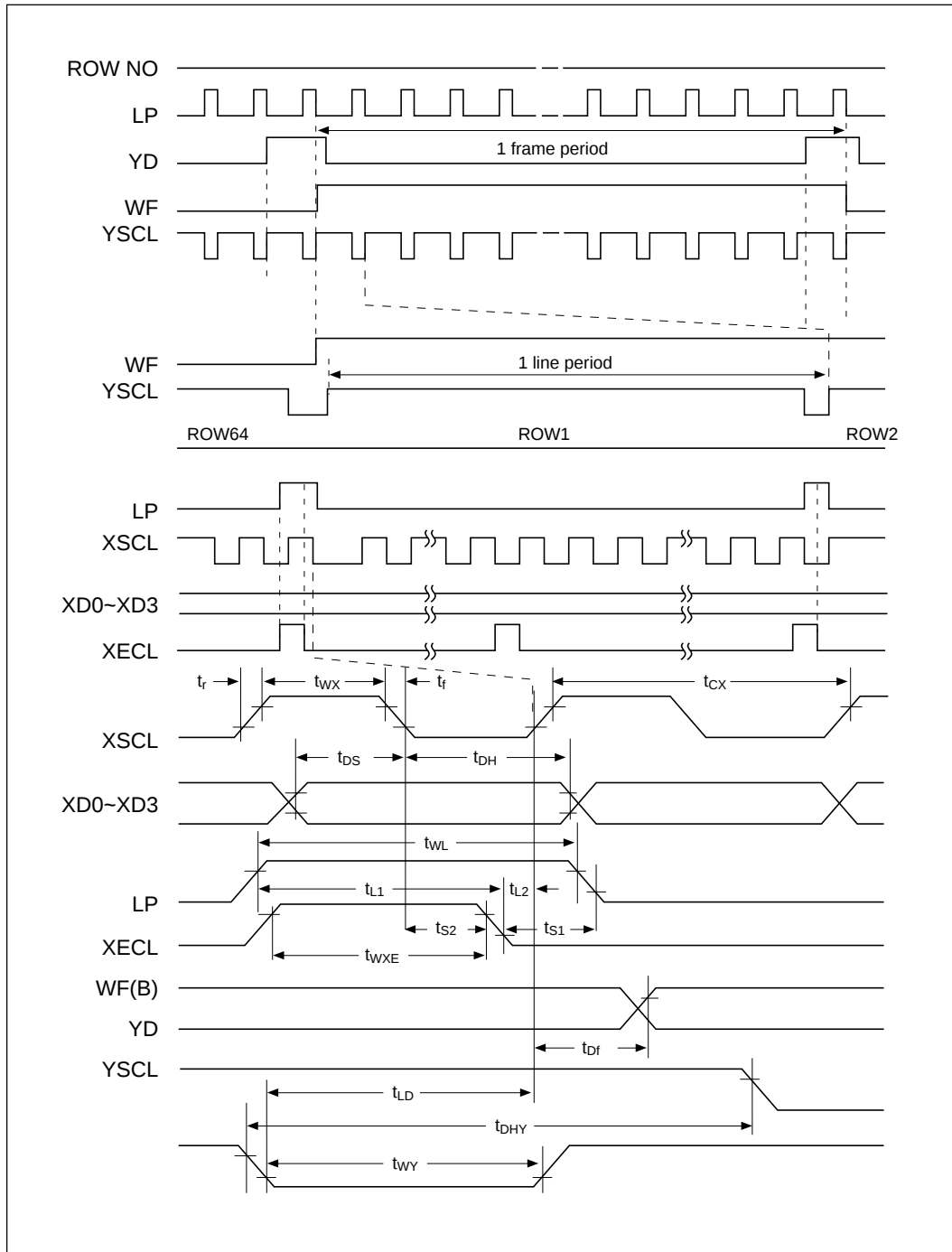
◦ Display Memory WRITE Timing



Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT φ0	Clock cycle	tc	100	—	ns	CL = 100 pF + 1TTL
VCE	VCE HIGH-level pulse width	tw	tc – 40	—	ns	
	VCE LOW-level pulse width	tCE	2tc – 40	—	ns	
VA0 to VA15	Write cycle time	tcyw	3tc	—	ns	
	VCE address hold time (fall)	tAHC	2tc – 40	—	ns	
	VCE address setup time (fall)	tASC	tc – 55	—	ns	
	VCE address hold time (rise)	tCA	5	—	ns	
	VR/W address setup time (fall)	tAS	0	—	ns	
	VR/W address hold time (rise)	tAH2	15	—	ns	
	VR/W address hold time (fall)	tOSC	—	—	ns	
VR/W	VCE write setup time (fall)	twsc	tc – 55	—	ns	
	VCE write hold time (fall)	twhc	2tc – 40	—	ns	
VD0 to VD7	VCE data input setup time (fall)	tdsc	twsc – 10	—	ns	
	VCE data input hold time (fall)	tdhc	2tc – 30	—	ns	
	VR/W data hold time (rise)	tdh2	10*	50	ns	

* Lines VD0 to VD7 are latched.

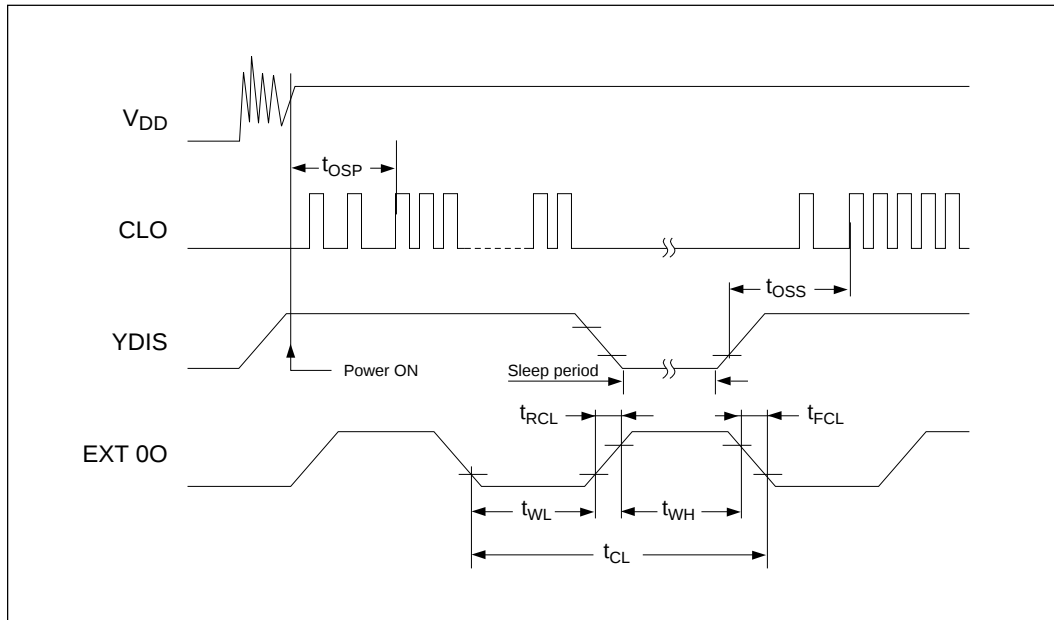
◦ LCD Control Timing



SED1330

Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
EXT $\phi 0$	Clock cycle	tc	100	—	ns	V _{DD} = 5.0V $\pm$ 10% CL = 150F
	Rising time	tr	—	35	ns	
	Falling time	tr	—	35	ns	
XSCL	Shift clock cycle time	tcx	4tc	—	ns	
	XSCL clock pulse width	twx	tcx2 – 80	—	ns	
XD0 to XD3	X-data hold time	t _{DH}	tcx2 – 100	—	ns	
	X-data setup time	t _{DS}	tcx2 – 100	—	ns	
LP	Latch data setup time	t _{LS}	tcx2 – 100	—	ns	
	LP signal pulse width	twL	tcx4 – 80	—	ns	
XECL	XECL setup time	t _{L1}	tcx3 – 100	—	ns	
	XECL data hold time	t _{L2}	tc – 30	—	ns	
	Enable setup time	t _{S1}	tc – 30	—	ns	
	Enable delay time	t _{S1}	tc – 30	—	ns	
	XECL clock pulse width	tw _{XE}	tcx3 – 80	—	ns	
WF	Time allowance of WF delay	t _{DF}	—	100	ns	
YSCL	LP delay time against YSCL	t _{LD}	tcx4 – 100	—	ns	
	YSCL clock pulse width	tw _Y	tcx4 – 80	—	ns	
YD	Y-data hold time	t _{DHY}	tcx6 – 100	—	ns	

○ Oscillator Timing

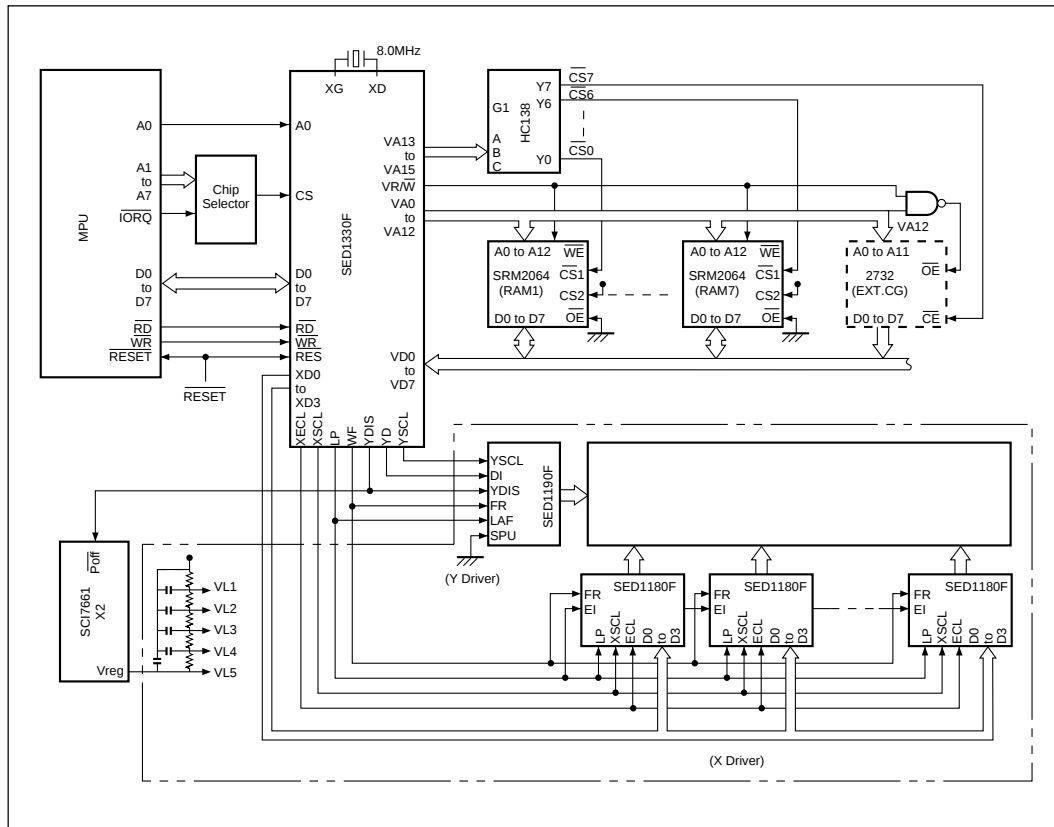


Signal	Parameter	Symbol	Rating		Unit	Remark
			Min	Max		
CLO	Time to stable CLO output after power-ON	t_{OSP}	—	3	ms	$\overline{RES} = H$ 20 pF
	Time to stable CLO after sleep OFF	t_{OSS}	—	1	ms	
EXT $\phi 0$	External clock rise time	t_{RCL}	—	15	ns	
	External clock fall time	t_{FCL}	—	15	ns	
	External clock high-pulse width	t_{WH}	*1	*2	ns	
	External clock low-pulse width	t_{WL}	*1	*2	ns	
	External clock cycle	t_{CL}	100	—	ns	

*1. $(t_{CL} - t_{RCL} - t_{FCL}) \times 475/1000 < t_{WH}, t_{WL}$

*2. $(t_{CL} - t_{RCL} - t_{FCL}) \times 525/1000 > t_{WH}, t_{WL}$

■ EXAMPLE OF APPLICATION



■ CHARACTER CODE TABLE (BUILT-IN CHARACTER GENERATOR)

		Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)	2		!	"	#	\$	%	&	'	(	)	*	+	,	-	.	/
	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
	6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
	7	p	q	r	s	t	u	v	w	x	y	z	{		}	~	
	A		あ	い	う	え	お	か	き	く	け	こ	さ	し	す	せ	そ
	B	ー	ア	イ	ウ	エ	オ	カ	キ	ク	ケ	コ	サ	シ	ス	セ	ソ
	C	タ	チ	ツ	テ	ト	ナ	ニ	ノ	ハ	ヒ	フ	ヘ	ホ	マ	ミ	ム
	D	メ	ム	ヤ	ユ	ヨ	ラ	リ	ル	レ	ロ	ワ	ヰ	ヱ	ヰ	ヱ	ヰ
	1																

Note:  means all dots of 6 × 8 matrix are on.

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