CS5351

108 dB, 192 kHz, Multi-Bit Audio A/D Converter

Features

- Advanced Multi-bit Delta-Sigma Architecture
- 24-Bit Conversion
- 108 dB Dynamic Range
- -98 dB THD+N
- System Sampling Rates up to 192 kHz
- Single-Ended Analog Inputs
- Less than 150 mW Power Consumption
- High Pass Filter or DC Offset Calibration
- Supports Logic Levels Between 5 and 1.8V
- Linear Phase Digital Anti-Alias Filtering
- Functionally Compatible with the CS5361

General Description

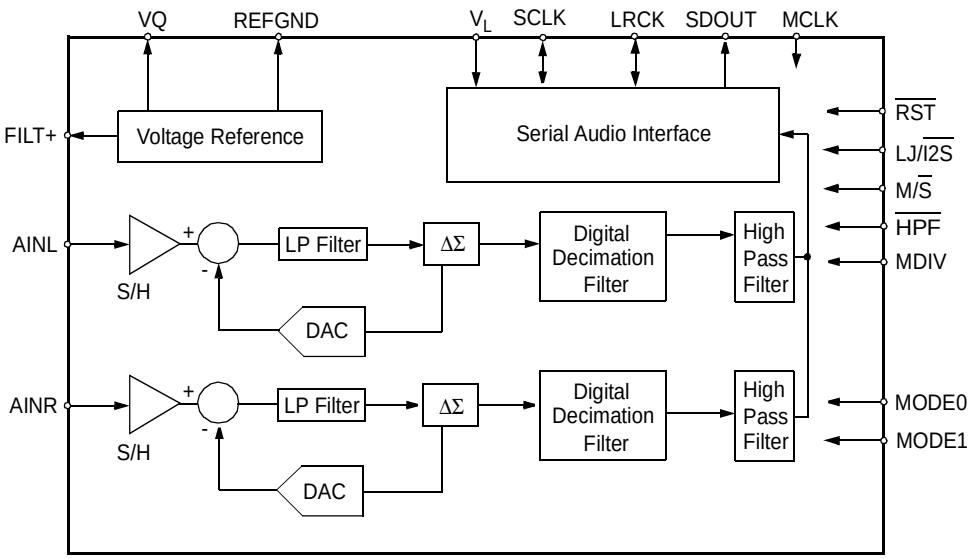
The CS5351 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 192 kHz per channel.

The CS5351 uses a 5th-order, multi-bit delta-sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5351 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD-R, CD-R, digital mixing consoles, and effects processors.

ORDERING INFORMATION

CS5351-KS	-10° to 70° C	24-pin SOIC
CS5351-BS	-40° to 85° C	24-pin SOIC
CDB5351	Evaluation Board	



Advance Product Information

This document contains information for a new product.
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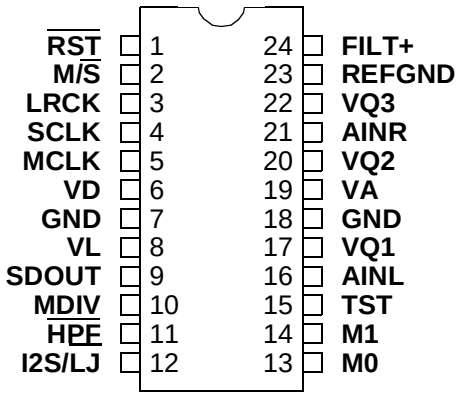
1 PIN DESCRIPTIONS



Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - The device enters system reset when enabled.
M/S	2	**Master / Slave Select** (*Input*) - Selects operation as either clock master or slave.
LRCK	3	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	4	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	6	**Digital Power** (*Input*) **-** Positive power for the digital section.
GND	7,18	**Ground** (*Input*) - Ground reference.
VL	8	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDOUT	9	**Serial Audio Data** (*Output*) - Output for two's complement serial audio data.
MDIV	10	**Master Clock Divide** (*Input*) - Enables a master clock divide by two function.
HPF	11	**High-Pass Filter Enable** (*Input*) - Enables the Digital High-Pass Filter.
I2S/LJ	12	**Serial Audio Interface Format Select** (*Input*) - Selects either the left-justified or I^2S format for the SAI.
M0 **M1**	13, 14	**Mode Selection** (*Input*) - Determines the operational mode of the device.
TST	15	**Test** (*Input*) - Intended for testing only.
AINR **AINL**	16, 21	**Analog Input** (*Input*) - The full scale analog input level is specified in the Analog Characteristics specification table.
VQ1 **VQ2** **VQ3**	17, 20, 22	**Quiescent Voltage** (*Input/Output*) **-** Filter connection for internal quiescent reference voltage.
VA	19	**Analog Power** (*Input*) **-** Positive power for the analog section.
REFGND	23	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
FILT+	24	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.

2 TYPICAL CONNECTION DIAGRAM

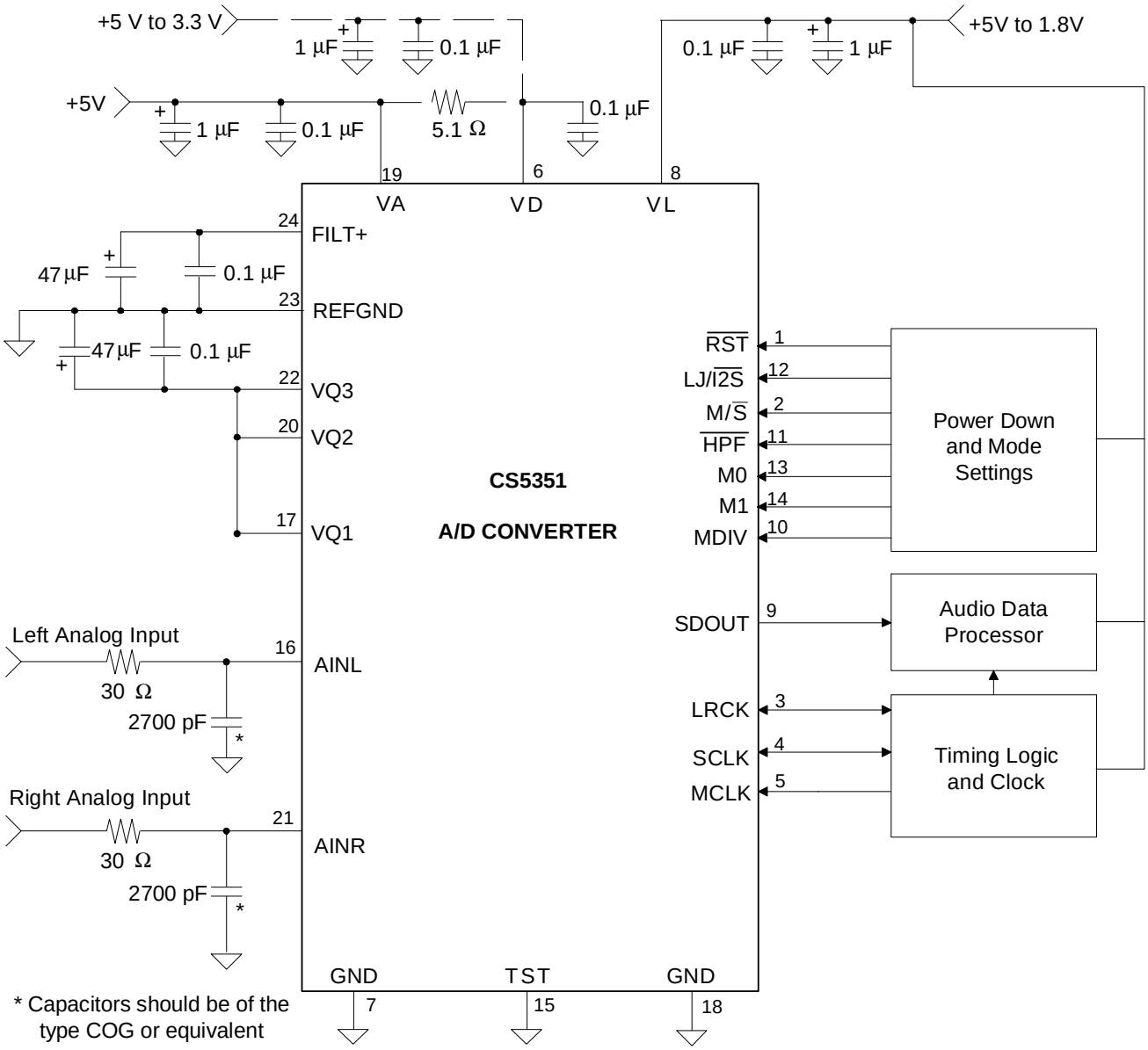


Figure 1. Typical Connection Diagram

3 APPLICATIONS

3.1 Operational Mode/Sample Rate Range Select

The output sample rate, Fs, can be adjusted from 2kHz to 192kHz. The CS5351 must be set to the proper speed mode via the mode pins, M1 and M0. Refer to Table 1.

Mode 1	Mode 0	MODE	Output Sample Rate (Fs)
0	0	Single Speed Mode	2kHz - 50kHz
0	1	Double Speed Mode	50kHz - 100kHz
1	0	Quad Speed Mode	100kHz - 192kHz
1	1	Reserved	

Table 1. CS5351 Mode Control

3.2 System Clocking

The device supports operation in either Master Mode, where the left/right and serial clocks are synchronously generated on-chip, or Slave mode, which requires external generation of the left/right and serial clocks. The device also includes a master clock divide mode where the master clock will be internally divided prior to any other internal circuitry when MDIV is enabled, set to logic 1.

3.2.1 Master Mode

In Master mode, LRCK and SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 2. Refer to Table 2 for common master clock frequencies

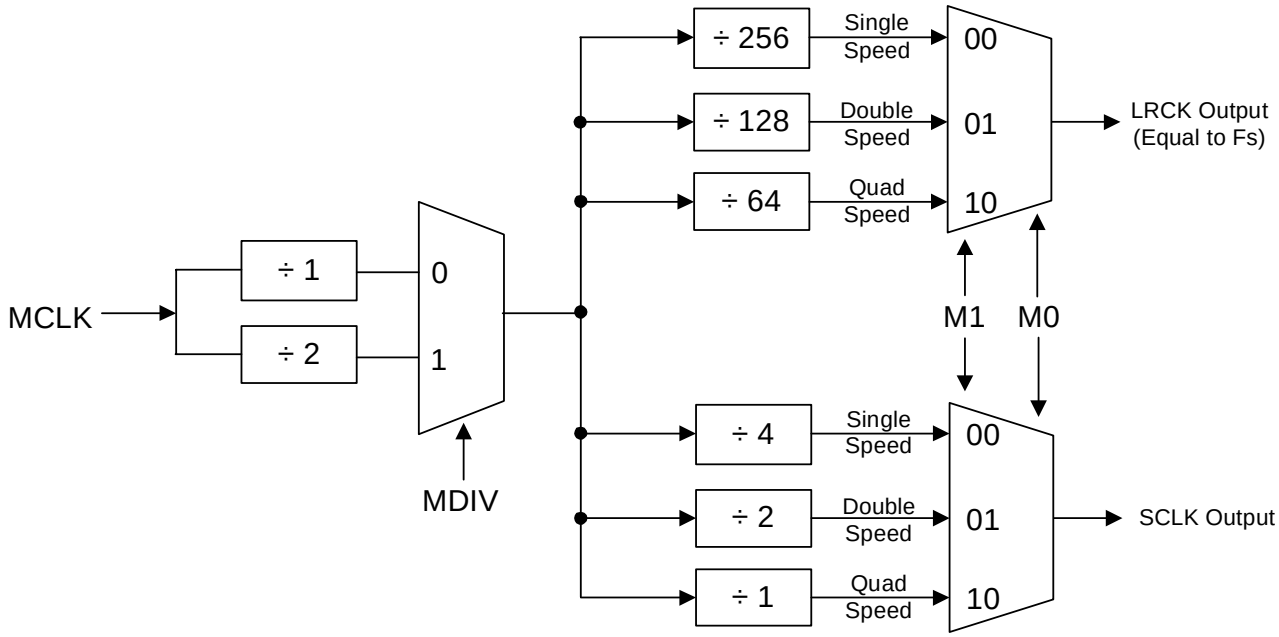


Figure 2. CS5351 Master Mode Clocking

SAMPLE RATE (kHz)	DIV = 0 MCLK (MHz)	DIV = 1 MCLK (MHz)
32	8.192	16.384
44.1	11.2896	22.5792
48	12.288	24.576
64	8.192	16.384
88.2	11.2896	22.5792
96	12.288	24.576
176.4	11.2896	22.5792
192	12.288	24.576

Table 2. CS5351 Common Master Clock Frequencies

3.2.2 Slave Mode

LRCK and SCLK operate as inputs in Slave mode. The left/right clock must be synchronously derived from the master clock and be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and be equal to 64x Fs to maximize system performance. Refer to Table 3 for required clock ratios.

	Mode 0 (SSM)	Mode 1 (DSM)	Mode 2 (QSM)
MCLK/LRCK Ratio	256x (512x)*	128x (256x)*	128x (256x)*
SCLK/LRCK Ratio	32x, 64x, 128x	32x, 64x	64x

*Available when MDIV = 1

Table 3. CS5351 Slave Mode Clock Ratios

3.3 Power-up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

The internal reference voltage must be stable for the device to produce valid data. Therefore, there is a delay between the release of reset and the generation of valid output, due to the finite output impedance of FILT+ and the presence of the external capacitance.

3.4 Analog Connections

The analog modulator samples the input at 6.144 MHz (MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are ($n \times 6.144$ MHz) the digital passband frequency, where n=0,1,2,...Refer to the Typical Connection Diagram which shows the suggested filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the analog input pins.

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3.5 High Pass Filter and DC Offset Calibration

The operational amplifiers in the input circuitry driving the CS5351 may generate a small DC offset into the A/D converter. The CS5351 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the $\overline{\text{HPF}}$ pin is taken high during normal operation, the current value of the DC offset register is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1) Running the CS5351 with the high pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.

2) Disabling the high pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5351.

3.6 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5351 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and REFGND. The CDB5351 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

3.7 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS5351's in the system. If only one master clock source is needed, one solution is to place one CS5351 in Master mode, and slave all of the other CS5351's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5351 reset with the inactive edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

4 CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (CS5351-KS)

(T_A = 25° C; Logic "0" = GND = 0 V; Logic "1" = VL = 5V; VA = 5V, VD = 3.3V, MCLK = 12.288 MHz, SCLK = 64 Fs, Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 1 kHz sine wave.)

Parameter		Symbol	Min	Typ	Max	Unit
Single Speed Mode Fs = 48kHz						
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
Double Speed Mode Fs = 96kHz						
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
	40kHz bandwidth unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
	40kHz bandwidth -1dB		-	-95	-	dB
Quad Speed Mode Fs = 192kHz						
Dynamic Range	A-weighted		102	108	-	dB
	unweighted		99	105	-	dB
	40kHz bandwidth unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-98	-92	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
	40kHz bandwidth -1dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	95	-	dB
Interchannel Phase Deviation			-	0.0001	-	Degree
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage			0.95	1.0	1.05	Vrms
Input Impedance			18	-	-	kΩ

Note: 1. Referred to the typical full-scale input voltage

ANALOG CHARACTERISTICS (CS5351-BS) (T_A = 25° C; Logic "0" = GND = 0 V; Logic "1" = VL = 5V; VA = 5V, VD = 3.3V, MCLK = 12.288 MHz, SCLK = 64 Fs, Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 1 kHz sine wave.)

Parameter		Symbol	Min	Typ	Max	Unit
Single Speed Mode Fs = 48kHz						
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
Double Speed Mode Fs = 96kHz						
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
	40kHz bandwidth unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
	40kHz bandwidth -1dB		-	-95	-	dB
Quad Speed Mode Fs = 192kHz						
Dynamic Range	A-weighted		101	108	-	dB
	unweighted		98	105	-	dB
	40kHz bandwidth unweighted		-	102	-	dB
Total Harmonic Distortion + Noise	(Note 1)	THD+N				
	-1 dB		-	-98	-91	dB
	-20 dB		-	-85	-	dB
	-60 dB		-	-45	-	dB
	40kHz bandwidth -1dB		-	-95	-	dB
Dynamic Performance for All Modes						
Interchannel Isolation			-	95	-	dB
Interchannel Phase Deviation			-	0.0001	-	Degree
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Error				-	±5	%
Gain Drift			-	±100	-	ppm/°C
Offset Error	HPF enabled		-	0	-	LSB
	HPF disabled		-	100	-	LSB
Analog Input Characteristics						
Full-scale Input Voltage			0.9	1.0	1.1	Vrms
Input Impedance			18	-	-	kΩ

DIGITAL DECIMATION FILTER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Single Speed Mode (2kHz to 50kHz sample rates)					
Passband (-0.1 dB) (Note 3)		0	-	0.469	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 3)		0.579	-	-	Fs
Stopband Attenuation		-95	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
Double Speed Mode (50kHz to 100kHz sample rates)					
Passband (-0.1 dB) (Note 3)		0	-	0.45	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 3)		0.670	-	-	Fs
Stopband Attenuation		-92	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
Quad Speed Mode (100kHz to 192kHz sample rates)					
Passband (-0.1 dB) (Note 3)		0	-	0.245	Fs
Passband Ripple		-	-	±0.035	dB
Stopband (Note 3)		0.775	-	-	Fs
Stopband Attenuation		-97	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.0	µs
High Pass Filter Characteristics					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 2)			20	-	Hz
Phase Deviation @ 20Hz (Note 2)		-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time			10^4/Fs		s

Notes: 2. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

3. The filter frequency response scales precisely with Fs.

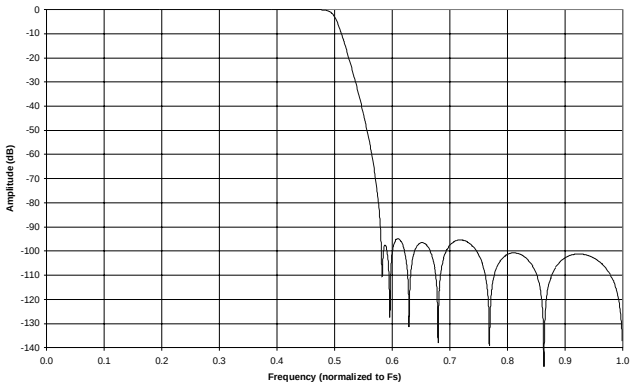


Figure 3. Single Speed Mode Stopband Rejection

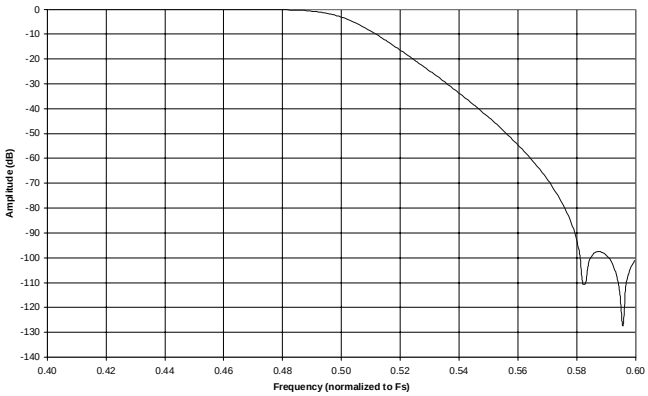


Figure 4. Single Speed Mode Transition Band

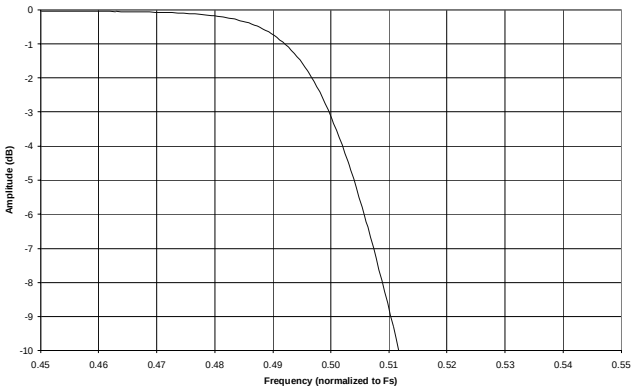


Figure 5. Single Speed Mode Transition Band (Detail)

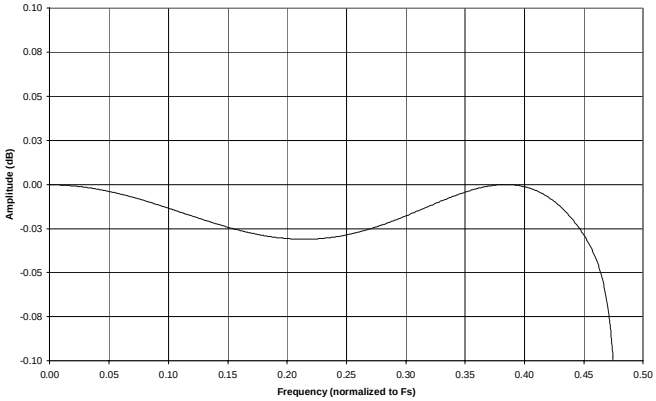


Figure 6. Single Speed Mode Passband Ripple

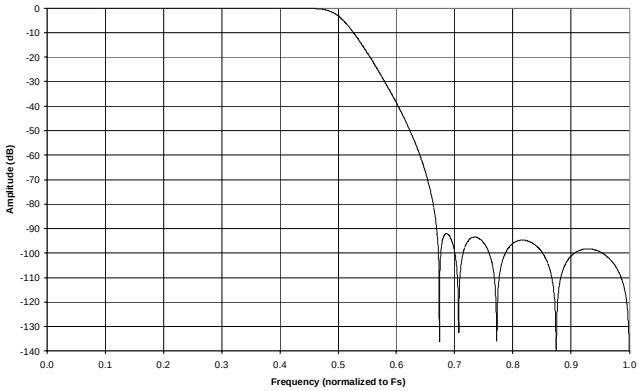


Figure 7. Double Speed Mode Stopband Rejection

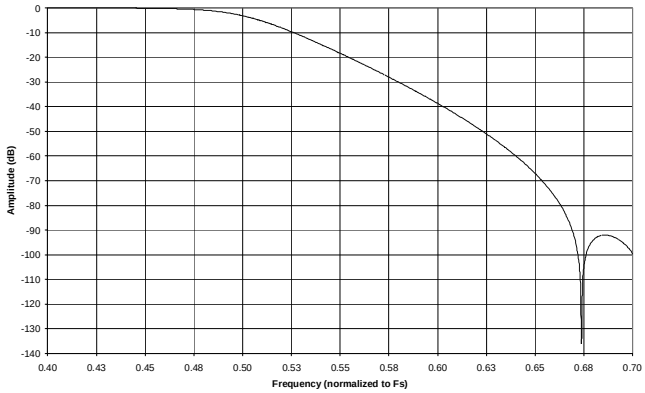


Figure 8. Double Speed Mode Transition Band

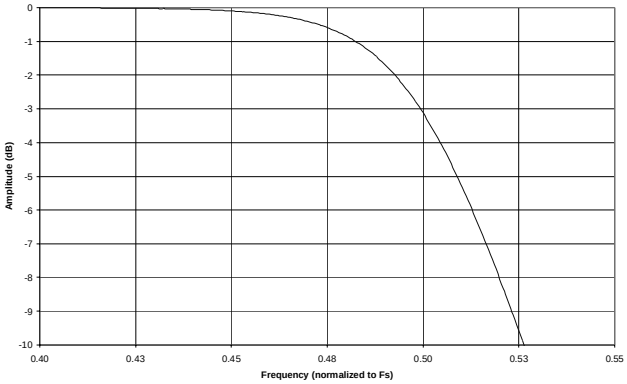


Figure 9. Double Speed Mode Transition Band (Detail)

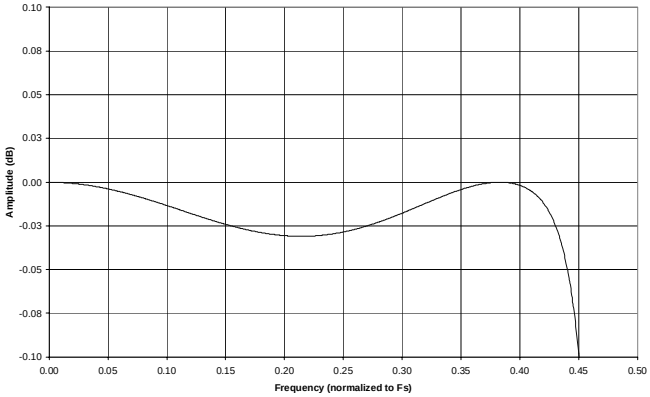


Figure 10. Double Speed Mode Passband Ripple

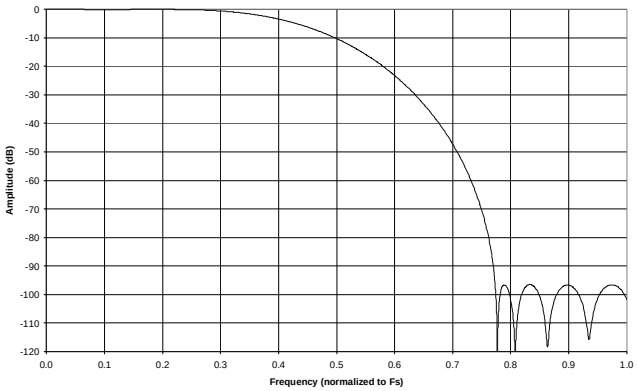


Figure 11. Quad Speed Mode Stopband Rejection

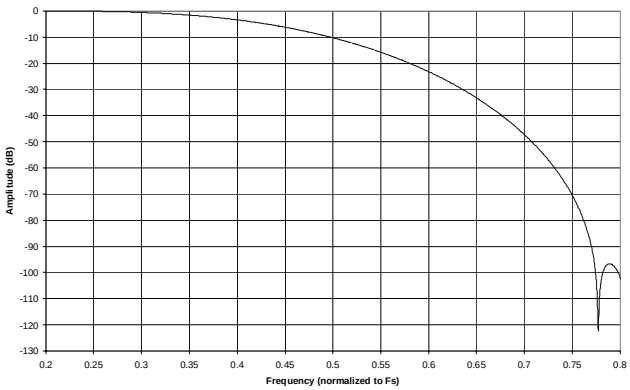


Figure 12. Quad Speed Mode Transition Band

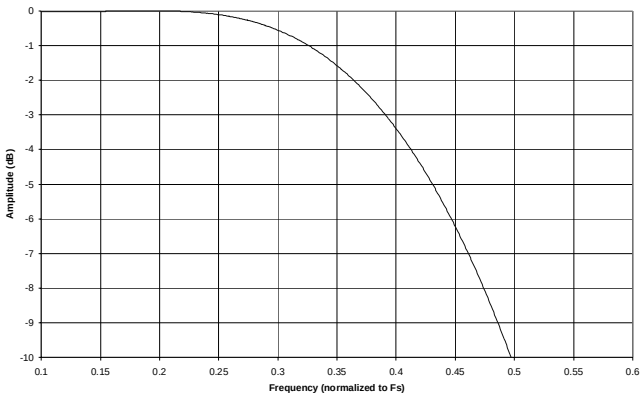


Figure 13. Quad Speed Mode Transition Band (Detail)

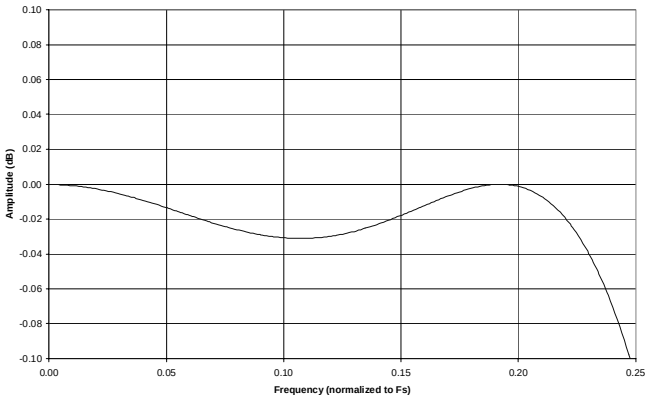


Figure 14. Quad Speed Mode Passband Ripple

DC ELECTRICAL CHARACTERISTICS (GND = 0V, all voltages with respect to ground. T_A = 25 °C; MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies:	Positive Analog	VA	4.75	5.0	5.25	V
	Positive Digital	VD	3.1	-	5.25	V
	Positive Logic	VL	1.7	-	5.25	V
Power Supply Current	VA	I_A	-	17.5	21	mA
(Normal Operation)	VL,VD = 5 V	I_D	-	22	26	mA
	VL,VD = 3.3V	I_D	-	14.5	17	mA
Power Supply Current	VA	I_A	-	2	-	mA
(Power-Down Mode)(Note 4)	VL,VD=5V	I_D	-	2	-	mA
Power Consumption						
(Normal Operation)	VL, VD=5V	-	-	198	235	mW
	VL, VD = 3.3V	-	-	135	161	mW
	(Power-Down Mode)	-	-	20	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 5)	PSRR	-	65	-	dB
V_Q Nominal Voltage			-	2.5	-	V
Output Impedance			-	50	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	5	-	V
Output Impedance			-	35	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

Notes: 4. Power Down Mode is defined as $\overline{RST}$ = Low with all clocks and data lines held static.

5. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS (T_A = 25 °C)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VL)	V_{IL}	-	-	30%	V
High-Level Output Voltage at I_o = 2 mA		V_{OH}	VL - 1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature			-	-	135	°C
Junction to Ambient Thermal Impedance		θ_{JA}	-	70	-	°C/W
Ambient Operating Temperature (Power Applied)	-KS	T_A	-10	-	+70	°C
	-BS	T_A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS (GND = 0V, All voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Logic	VL	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
Input Current	(Note 6)	I_{in}	-	-	±10	mA
Analog Input Voltage	(Note 7)	V_{IN}	GND-0.7	-	VA+0.7	V
Digital Input Voltage	(Note 7)	V_{IND}	-0.7	-	VL+0.7	V
Ambient Operating Temperature (Power Applied)	-KS	T_A	-20	-	+85	°C
	-BS	T_A	-50	-	+95	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 6. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.

7. The maximum over/under voltage is limited by the input current.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (T_A = 25° C; Logic "0" = GND = 0 V; Logic "1" = VL = VA = 5 V, VD = 3.3V, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Period	t_{clkw}	40	-	1953	ns
MCLK Pulse Width High	tclkh	15	-	-	ns
MCLK Pulse Width Low	tclkl	15	-	-	ns
Master Mode					
SCLK falling to LRCK	t_{mslr}	-20	-	20	ns
SCLK falling to SDOUT valid	t_{sdo}	0	-	40	ns
SCLK Duty Cycle		-	50	-	%
LRCK Duty Cycle		-	50	-	%
Slave Mode					
Single Speed					
Output Sample Rate	Fs	2	-	50	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	163	-	-	ns
SCLK High/Low	t_{sclkhl}	20	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	40	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
Double Speed					
Output Sample Rate	Fs	50	-	100	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	163	-	-	ns
SCLK High/Low	t_{sclkhl}	20	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	40	ns
SCLK falling to LRCK edge	t_{slrd}	-20	-	20	ns
Quad Speed					
Output Sample Rate	Fs	100	-	192	kHz
LRCK Duty Cycle		40	50	60	%
SCLK Period	t_{sclkw}	81	-	-	ns
SCLK High/Low	t_{sclkhl}	20	-	-	ns
SCLK falling to SDOUT valid	t_{dss}	-	-	20	ns
SCLK falling to LRCK edge	t_{slrd}	-10	-	10	ns

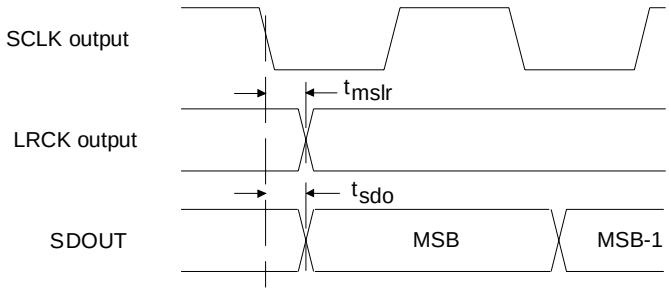


Figure 15. Master Mode, Left Justified Serial Audio Interface

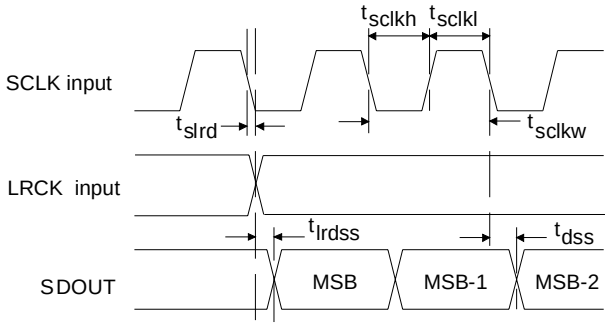


Figure 16. Slave Mode, Left Justified Serial Audio Interface

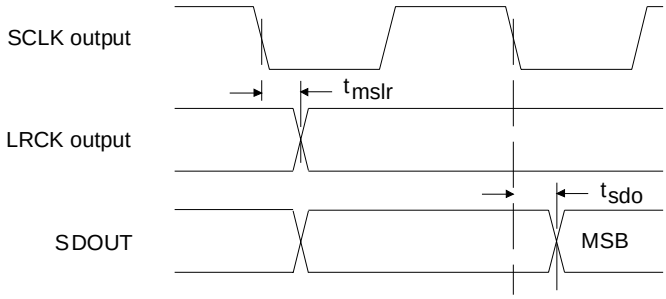


Figure 17. Master Mode, I²S Serial Audio Interface

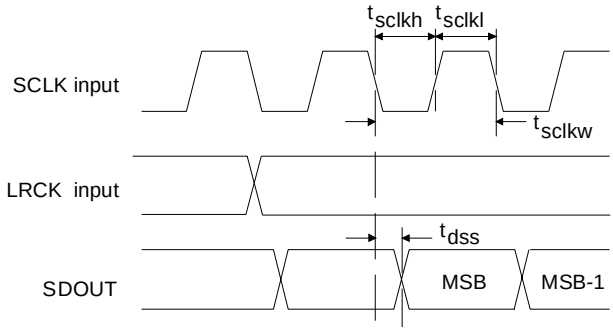


Figure 18. Slave Mode, I²S Serial Audio Interface

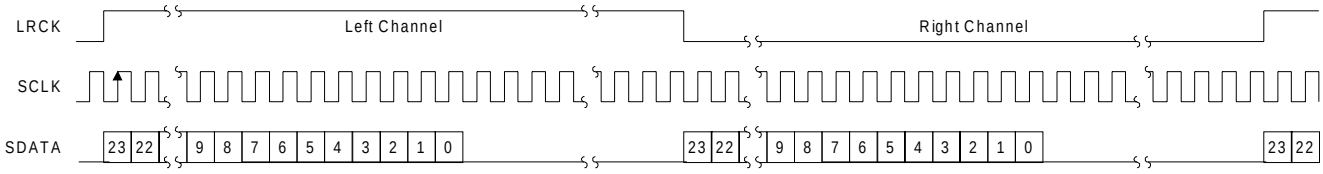


Figure 19. Left-Justified Serial Audio Interface

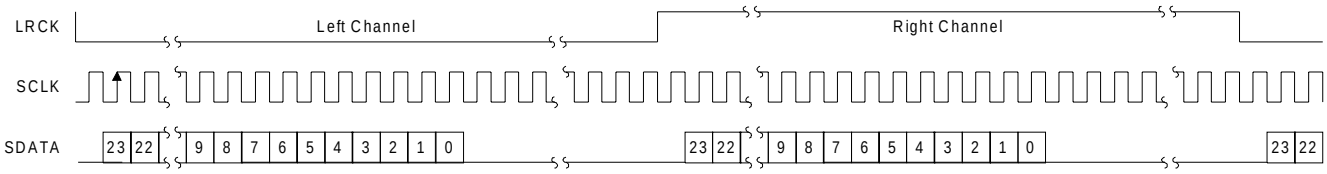


Figure 20. I^2S Serial Audio Interface

5 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

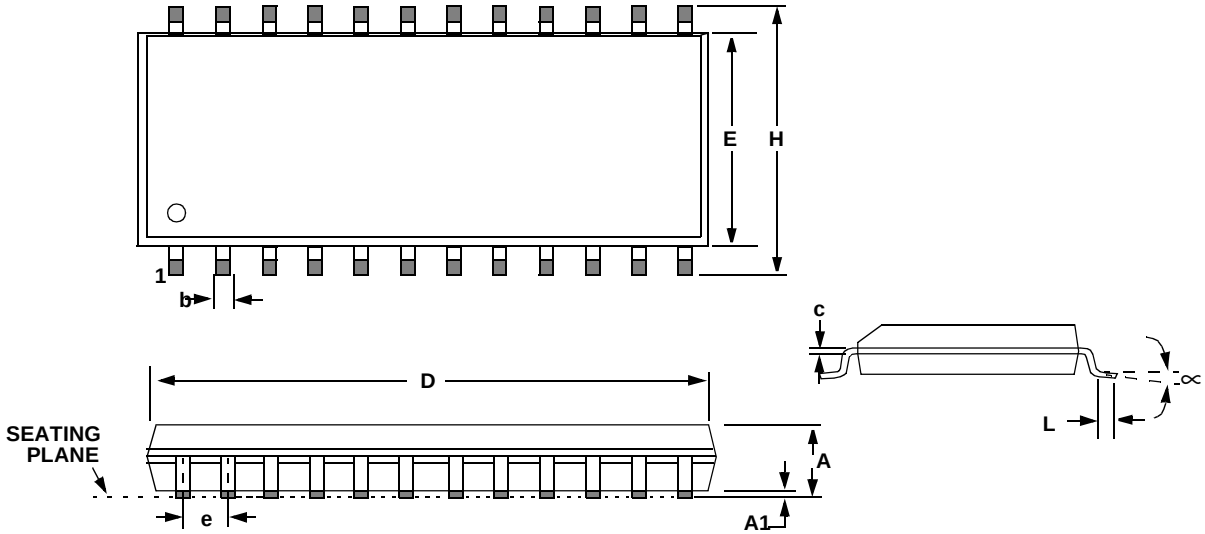
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

6 PACKAGE DIMENSIONS

24L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

• Notes •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