

## Fixed Function Multi-Effects Audio Processor

### Features

- DSP for embedded reverb/effects applications
  - 24-bit Audio Processing Engine
  - No External RAM required
  - Two 24-bit  $\Delta\Sigma$  ADCs with 100 dB Dyn. Range
  - Two 24-bit  $\Delta\Sigma$  DACs with 100 dB Dyn. Range
- Mono Guitar or Mixer Effects firmware included
- Real time parameter control via messaging protocol
- Serial Control Port for microcontroller interface
- Single +5V supply operation
- 100-pin Metric Quad Flat Package (MQFP)

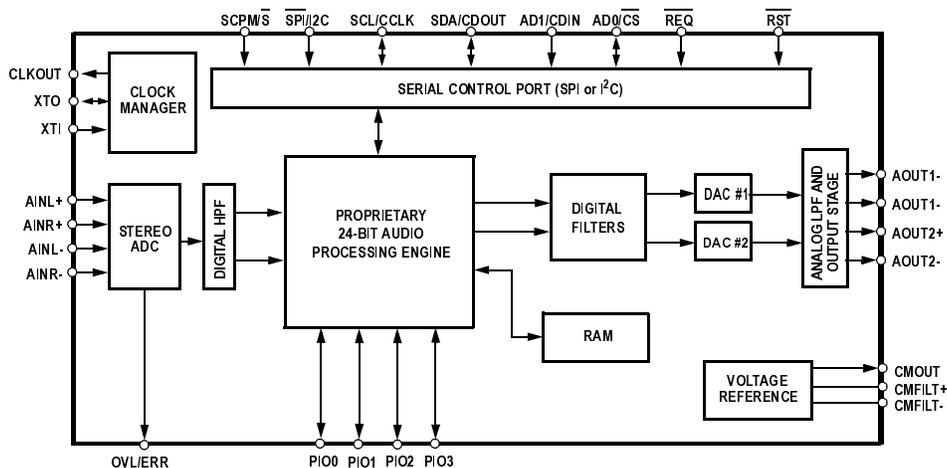
### Description

The CS4812 is a complete audio effects processing system on a chip. This device includes a proprietary 24-bit audio processing engine with considerable on-chip RAM, two ADCs and two DACs. A full-featured serial control port allows interfacing to an external host microcontroller. Other features such as single +5V operation simplify system design.

The CS4812, combined with Crystal effects firmware, is the ideal solution for a variety of effects processing applications where user parameter control is desired. The Crystal effects firmware provides a messaging protocol for the serial control port that allows an external microcontroller to have real-time parameter control over the audio effects. The complete processor and effects solution may be evaluated with the CDB4812 demonstration board. The CDB4812 demonstrates a host of mono electric guitar effects including a digital spring reverb, delay, chorus, flange and tremolo with parameter adjustment capability. Please refer to AN195 for more information on application firmware for the CS4812.

### ORDERING INFO

CS4812-KM	-10 to +70°C	100-pin MQFP
CDB4812	Electric Guitar Effects w/ Parameter Controls.	



### Advance Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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## 1. CHARACTERISTICS AND SPECIFICATIONS

**ADC CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ;  $V_A, V_D = +5\text{V}$ ; -1 dB Full Scale Input Sine wave, 997 Hz;  $F_s = 48\text{ kHz}$ ;  $XTI = 12.288\text{ MHz}$  (PLL disabled). Measurement Bandwidth is 20 Hz to 20 kHz.)

Parameters	Symbol	Min	Typ	Max	Units		
<b>Analog Input Characteristics</b>							
ADC Conversion Stereo Audio channels		16	-	24	Bits		
Dynamic Range	(A weighted, Note 5)	93	100	-	dB		
	(unweighted, Note 5)	90	97	-	dB		
Total Harmonic Distortion + Noise (PLL enabled)	(Note 1,5)	-	-92	-87	dB		
	(Note 1,2,5)	-	-92	-	dB		
Interchannel Isolation		-	90	-	dB		
Interchannel Gain Mismatch		-	0.1	-	dB		
Offset Error (with high pass filter enabled)	(Note 6)	-	-	0	LSB		
Full Scale Input Voltage (Differential)		1.9	2.0	2.1	$V_{\text{rms}}$		
Gain Drift	(Note 2)	-	100	-	ppm/ $^\circ\text{C}$		
Input Resistance		10	-	-	k $\Omega$		
Input Capacitance		-	-	15	pF		
CMOUT Output Voltage		-	2.3	-	V		
Common Mode Rejection Ratio	(Note 2)		CMRR	60	dB		
Group Delay ( $F_s = \text{Output Sample Rate}$ )	(Note 4)		$t_{\text{gd}}$	-	15/ $F_s$	s	
Group Delay Variation vs. Frequency			$\Delta t_{\text{gd}}$	-	-	0	$\mu\text{s}$
<b>High Pass Filter Characteristics</b>							
Frequency Response	-3dB (Note 3)	-	3.7	-	Hz		
	-0.14dB (Note 3)	-	20	-	Hz		
Phase Deviation	@ 20 Hz (Note 3)	-	10	-	Degree		
Passband Ripple		-	-	0	dB		

- Notes:
1. Referenced to typical full-scale differential input voltage ( $2 V_{\text{rms}}$ ).
  2. Bench tested only.
  3. Filter characteristics scale with output sample rate.
  4. Group delay for  $F_s = 48\text{ kHz}$ ,  $t_{\text{gd}} = 15/48\text{ kHz} = 313\ \mu\text{s}$ .
  5. Measured using differential analog input circuit, see Figure 10.
  6. Filter Response is not tested but guaranteed by design.

**DAC CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ;  $V_A, V_D = +5\text{V}$ ; -1 dB Full Scale Output Sine wave, 997 Hz;  $F_s = 48\text{ kHz}$ ;  $XTI = 12.288\text{ MHz}$  (PLL disabled). Measurement Bandwidth is 20 Hz to 20 kHz.)

Parameters	Symbol	Min	Typ	Max	Units
<b>Analog Output Characteristics - Minimum Attenuation, 10 k<math>\Omega</math>, 100 pF load; unless otherwise specified.</b>					
DAC Resolution		16	-	24	Bits
Dynamic Range (DAC not muted, A weighted)		95	100	-	dB
Total Harmonic Distortion + Noise	THD+N	-	-90	-85	dB
Interchannel Isolation		-	90	-	dB
Interchannel Gain Mismatch		-	0.1	-	dB
Offset Voltage (differential) (Note 7)		-	-20 $\pm$ 5	-	mV
Offset Voltage ( $V_+/V_-$ relative to CMOUT) (Note 7)		-	-45/-25	-	mV
Full Scale Output Voltage (Differential)		1.9	2.0	2.1	$V_{\text{rms}}$
Gain Drift (Note 2)		-	100	-	ppm/ $^\circ\text{C}$
Out of Band Energy ( $F_s/2$ to $2F_s$ , Note 2)		-	-60	-	dBFS
Analog Output Load Resistance		10	-	-	k $\Omega$
Capacitance		-	-	100	pF
Group Delay ( $F_s = \text{Input Sample Rate}$ )	$t_{\text{gd}}$	-	16/ $F_s$	-	s
<b>Analog Loopback Performance</b>					
Signal-to-Noise Ratio (CCIR-2K weighted, -20 dB input)	CCIR-2K	-	74	-	dB
<b>Power Supply</b>					
Power Supply Current Operating		-	200	-	mA
Power Down (Note 8)		-	1	-	mA
Power Supply Rejection (1 kHz, 10 mV $_{\text{rms}}$ , Note 2)		-	50	-	dB

Notes: 7. Measured with DAC calibration disabled.

8. Measured with XTI clock disabled.

**SWITCHING CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ ;  $V_A, V_D = +5\text{V}$ ,  $C_L = 30\text{ pF}$ )

Parameters	Symbol	Min	Typ	Max	Units
Audio ADC's & DAC's Sample Rate	Fs	30	-	50	kHz
XTI Frequency XTI = 128Fs, 256Fs, 512Fs		3.84	-	25.6	MHz
XTI Duty Cycle XTI = 128Fs, 256Fs, 512Fs (Note 9)		40	-	60	%
XTI Jitter Tolerance		-	500	-	ps
$\overline{\text{RST}}$ Low Time (Note 10)		500	-	-	ns

Notes: 9. Guaranteed by characterization but not tested.

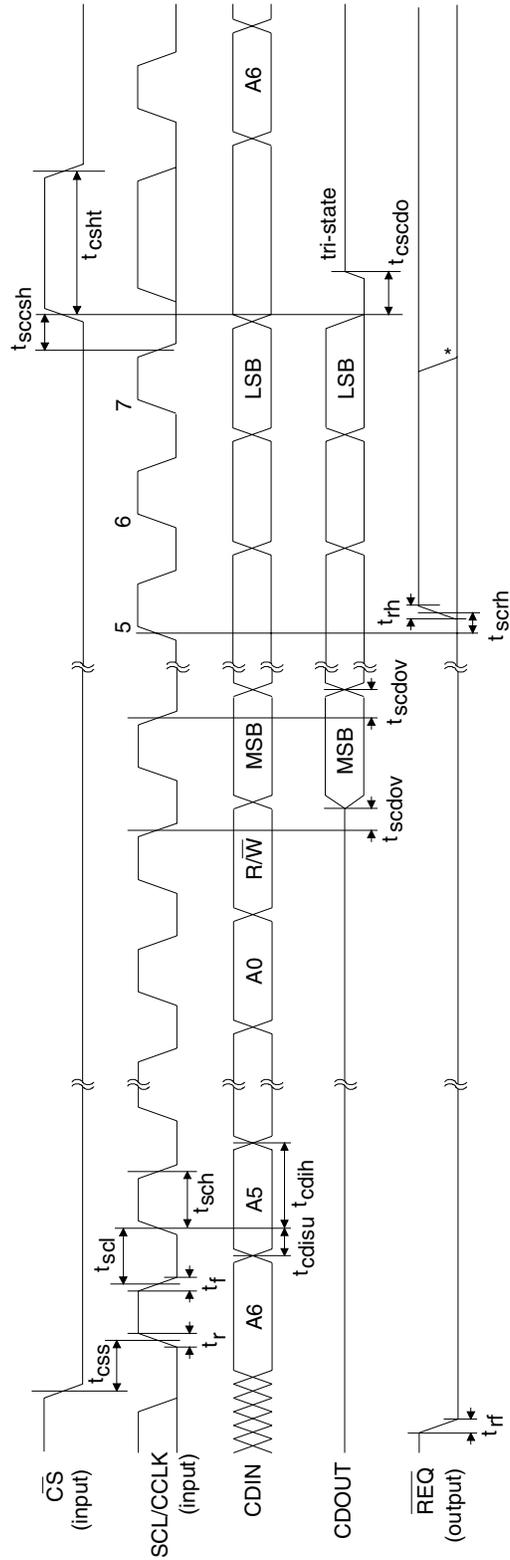
10. On power-up, the CS4812  $\overline{\text{RST}}$  pin should be asserted until the power supplies have reached steady state.

## SWITCHING CHARACTERISTICS - CONTROL PORT - SPI SLAVE

( $T_A = 25\text{ }^\circ\text{C}$ ;  $V_A, V_D = 5\text{ V}$ ; Inputs: Logic 0 = DGND, Logic 1 = VD,  $C_L = 30\text{ pF}$ )

Parameter	Symbol	Min	Max	Unit
<b>SPI Slave Mode</b> ( $\overline{\text{SPI/I2C}} = 0, \overline{\text{SCPM/S}} = 0$ , Note 14)				
CCLK Clock Frequency	$f_{\text{sck}}$	-	6	MHz
CCLK Low Time	$t_{\text{scl}}$	66	-	ns
CCLK High Time	$t_{\text{sch}}$	66	-	ns
Rise Time of Both CDIN and CCLK Lines	$t_r$	-	100	ns
Fall Time of Both CDIN and CCLK Lines	$t_f$	-	100	ns
Setup Time CDIN to CCLK Rising	$t_{\text{cdisu}}$	40	-	ns
Hold Time CCLK Rising to CDIN (Note 11)	$t_{\text{cdih}}$	15	-	ns
Time from CCLK edge to CDOUT Valid (Note 12)	$t_{\text{scdov}}$	-	45	ns
Rise Time for CDOUT	$t_{\text{cdor}}$	-	25	ns
Fall Time for CDOUT	$t_{\text{cdof}}$	-	25	ns
$\overline{\text{CS}}$ Falling to CCLK Rising	$t_{\text{css}}$	20	-	ns
Time from CCLK Falling to $\overline{\text{CS}}$ Rising	$t_{\text{sccsh}}$	0	-	ns
High Time Between Active $\overline{\text{CS}}$	$t_{\text{csht}}$	1	-	$\mu\text{s}$
Time from CCLK Rising to $\overline{\text{REQ}}$ Rising (Note 13)	$t_{\text{scrh}}$	-	$2 \cdot \text{DSPCLK} + 10$	ns
Rise Time for $\overline{\text{REQ}}$	$t_{\text{rr}}$	-	100	ns
Fall Time for $\overline{\text{REQ}}$	$t_{\text{rf}}$	-	100	ns

- Notes:
11. Data must be held for sufficient time to bridge 100 ns transition time of CCLK.
  12. CDOUT should NOT be sampled during this time period.
  13. DSPCLK frequency is twice the DSP instruction rate.
  14. Timing is guaranteed by characterization. Production test guarantees functionality.



\* See section 3.5.1.2 for a detailed explanation of  $\overline{REQ}$  behavior

**Figure 1. SPI Control Port Slave Mode Timing**

## SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MASTER

(TA = 25°C, VA, VD = 5V; Inputs: logic 0 = DGND, logic 1 = VD, CL = 30 pF)

Parameter	Symbol	Min	Typ	Max	Units
<b>SPI Master (AutoBoot) Mode</b> (SPI/I2C = 0, SCPM/S = 1, Note 14)					
CCLK Clock Frequency (Note 15)	$f_{sck}$	-	Fs	-	kHz
CCLK Low Time	$t_{scl}$	-	$1/(2*Fs)$	-	ns
CCLK High Time	$t_{sch}$	-	$1/(2*Fs)$	-	ns
CCLK Rise Time (Note 16)	$t_{r2}$	-	12	-	ns
CCLK Fall Time (Note 16)	$t_{f2}$	-	12	-	ns
RST rising to CS falling	$t_{srs}$	-	42	-	μs
CS High Time Between Transmissions	$t_{csh}$	37	-	-	μs
CS Falling to CCLK Edge	$t_{css}$	5	-	-	μs
CS Falling to CDOUT valid	$t_{dv}$	-	-	50	ns
CCLK Falling to CDOUT valid	$t_{pd}$	-	-	100	ns
CDIN to CCLK Rising Setup Time	$t_{dsu}$	80	-	-	ns
CCLK Rising to DATA Hold Time	$t_{dh}$	80	-	-	ns
CCLK Falling to CS rising	$t_{clcs}$	40	-	-	ns

Notes: 15. Depending on the input clock configuration, CCLK may be up to 2\*Fs temporarily during AutoBoot after RST is de-asserted and before the control port registers have been initialized.

16. Measured with a 2.2 kΩ pull-up resistor to VD.

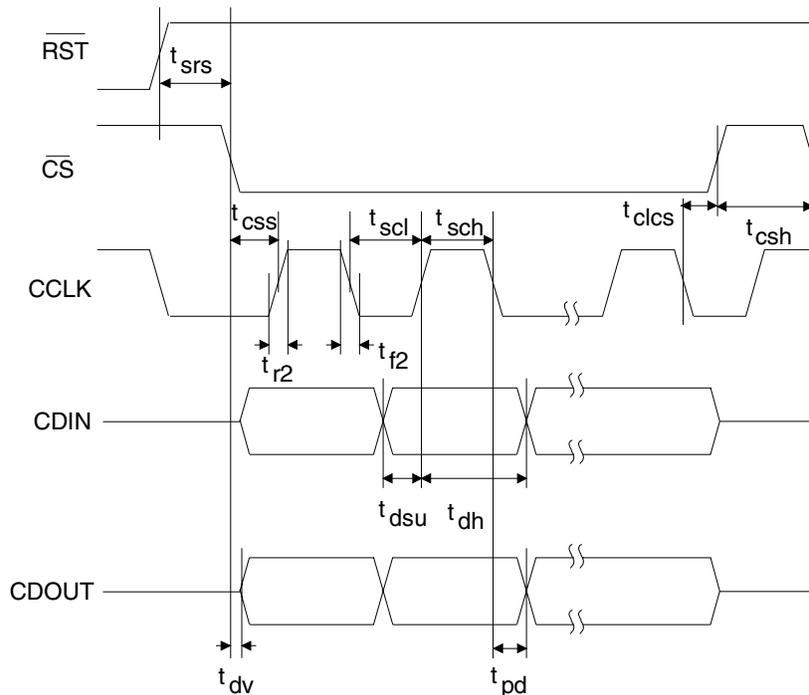


Figure 2. SPI Control Port Master Mode (AutoBoot) Timing

## SWITCHING CHARACTERISTICS - CONTROL PORT - I<sup>2</sup>C<sup>®</sup> SLAVE

(T<sub>A</sub> = 25 °C; V<sub>A</sub>, V<sub>D</sub> = 5 V; Inputs: Logic 0 = DGND, Logic 1 = V<sub>D</sub>, C<sub>L</sub> = 30 pF)

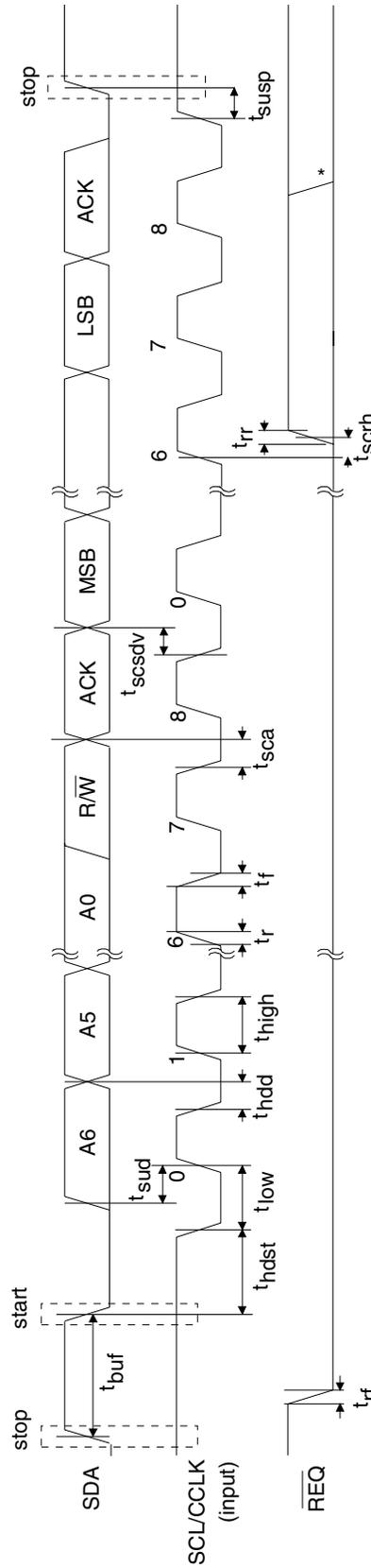
Parameter	Symbol	Min	Max	Units
<b>I<sup>2</sup>C<sup>®</sup> Slave Mode</b> ( $\overline{\text{SPI/I2C}} = 1, \overline{\text{SCPM/S}} = 0$ ) (Note 17)				
SCL Clock Frequency	f <sub>scl</sub>	-	100	kHz
Bus Free Time Between Transmissions	t <sub>buf</sub>	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t <sub>hdst</sub>	4.0	-	μs
SCL Low Time	t <sub>low</sub>	4.7	-	μs
SCL High Time	t <sub>high</sub>	4.0	-	μs
RST rising to start condition (Note18)	t <sub>srs</sub>	1	-	ms
SDA Hold Time from SCL Falling (Note 19)	t <sub>hdd</sub>	0	-	μs
Rise Time of Both SDA and SCL	t <sub>r</sub>	-	1	μs
Fall Time of Both SDA and SCL	t <sub>f</sub>	-	300	ns
SCL Falling to CS4812 ACK	t <sub>sca</sub>	-	1.3	μs
SCL Falling to SDA Valid During READ	t <sub>scsdv</sub>	-	1.5	μs
Time from SCL Rising to $\overline{\text{REQ}}$ Rising (Note 20)	t <sub>scrh</sub>	-	2*DSPCLK+10	ns
Rise Time for $\overline{\text{REQ}}$	t <sub>rr</sub>	-	100	ns
Fall Time for $\overline{\text{REQ}}$	t <sub>rf</sub>	-	100	ns
Setup Time for Stop Condition	t <sub>susp</sub>	4.7	-	μs
Setup Time for Repeated Start	t <sub>sust</sub>	4.7	-	μs

Notes: 17. Use of the I<sup>2</sup>C bus interface requires a license from Philips. I<sup>2</sup>C is a registered trademark of Philips Semiconductors.

18. Not tested.

19. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

20. DSPCLK frequency is twice the DSP instruction rate.



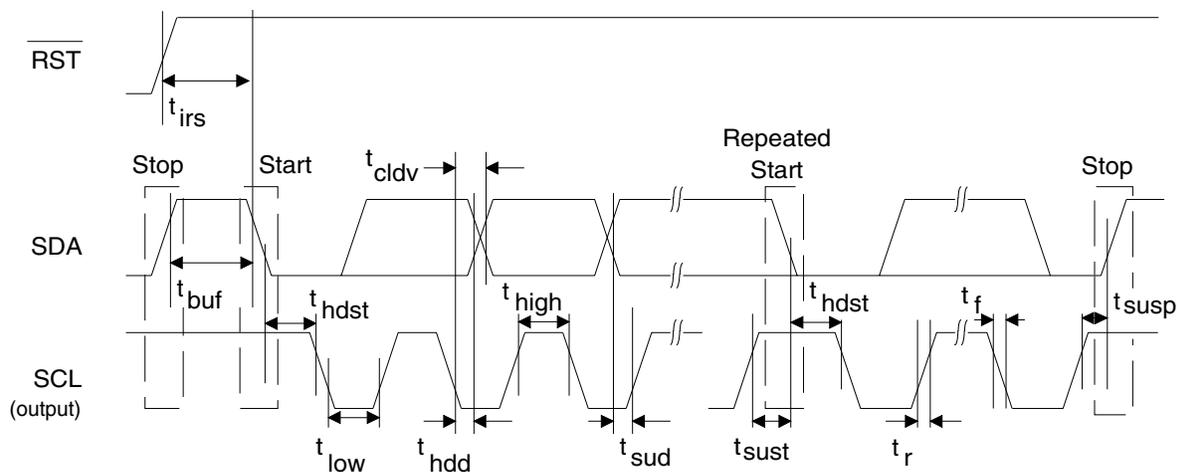
\* See section 3.5.2.2 for a detailed explanation of  $\overline{REQ}$  behavior

**Figure 3. I<sup>2</sup>C<sup>®</sup> Control Port Slave Mode Timing**

## SWITCHING CHARACTERISTICS - CONTROL PORT - I<sup>2</sup>C<sup>®</sup> MASTER (T<sub>A</sub> = 25°C; VA, VD = 5V; Inputs: logic 0 = DGND, logic 1 = VD, C<sub>L</sub> = 30 pF)

Parameter	Symbol	Min	Typ	Max	Units
<b>I<sup>2</sup>C<sup>®</sup> Master (AutoBoot) Mode</b> ( $\overline{\text{SPI}}/\text{I}2\text{C} = 1$ , $\text{SCPM}/\overline{\text{S}} = 1$ ) (Note 21)					
SCL Clock Frequency (Note 22)	f <sub>scl</sub>	-	Fs	-	kHz
Clock Low Time	t <sub>low</sub>	-	1/(2*Fs)	-	μs
Clock High Time	t <sub>high</sub>	-	1/(2*Fs)	-	μs
Bus Free Time Between Transmissions	t <sub>buf</sub>	4.7	-	-	μs
RST rising to start condition	t <sub>irs</sub>	-	22	-	μs
Start Condition Hold Time	t <sub>hdst</sub>	4.0	-	-	μs
Setup Time for Repeated Start Condition	t <sub>sust</sub>	13.5	-	-	μs
SDA Setup Time to SCL Rising	t <sub>sud</sub>	250	-	-	ns
SDA Hold Time from SCL Falling (Note 23)	t <sub>hdd</sub>	0	-	-	μs
SCL falling to SDA Output Valid	t <sub>cldv</sub>	-	-	1.5	μs
SCL and SDA Rise Time (Note 24)	t <sub>r</sub>	-	-	1	μs
SCL and SDA Fall Time (Note 24)	t <sub>f</sub>	-	-	300	ns
Setup Time for Stop Condition	t <sub>susp</sub>	4.7	-	-	μs

- Notes: 21. Use of the I<sup>2</sup>C bus interface requires a license from Philips. I<sup>2</sup>C is a registered trademark of Philips Semiconductors.
22. Depending on the input clock configuration, CCLK may be up to 2\*Fs temporarily during AutoBoot after RST has been de-asserted and before the control port registers have been initialized.
23. Data must be held for sufficient time to bridge the worst case fall time of 300 ns for CCLK/SCL.
24. For both SDA transmitting and receiving.



**Figure 4. I<sup>2</sup>C<sup>®</sup> Control Port Master Mode (AutoBoot) Timing**

**ABSOLUTE MAXIMUM RATINGS** (All voltages with respect to AGND = DGND = 0V.)

Parameters	Symbol	Min	Typ	Max	Units	
Power Supplies	Digital Analog	VD VA	-0.3 -0.3	- -	6.0 6.0	V V
Input Current	(Note 25)	-	-	±10.0	mA	
Analog Input Voltage	(Note 26)	-0.7	-	(VA)+0.7	V	
Digital Input Voltage	(Note 26)	-0.7	-	(VD)+0.7	V	
Ambient Temperature	(Power Applied)	-55	-	+125	°C	
Storage Temperature		-65	-	+150	°C	

Notes: 25. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

26. The maximum over or under voltage is limited by the input current.

Warning: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**

(All voltages with respect to AGND = DGND = 0V.)

Parameters	Symbol	Min	Typ	Max	Units	
Power Supplies	Digital	VD	4.75	5.0	5.25	V
I <sub>VA</sub> - V <sub>DI</sub> < 0.4V	Analog	VA	4.75	5.0	5.25	V
Operating Ambient Temperature	T <sub>A</sub>	-10	25	70	°C	

**DIGITAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C; V<sub>A</sub>, V<sub>D</sub> = 5V)

Parameters	Symbol	Min	Typ	Max	Units
High-level Input Voltage (except XTI)	V <sub>IH</sub>	2.8	-	(VD)+0.3	V
Low-level Input Voltage (except XTI)	V <sub>IL</sub>	-0.3	-	0.8	V
High-level Output Voltage at I <sub>O</sub> = -2.0 mA (except XTO)	V <sub>OH</sub>	(VD)-1.0	-	-	V
Low-level Output Voltage at I <sub>O</sub> = 2.0 mA (except XTO)	V <sub>OL</sub>	-	-	0.4	V
High-level Input Voltage (XTI)	V <sub>IH</sub>	2.8	-	-	V
Low-level Input Voltage (XTI)	V <sub>IL</sub>	-	-	2.3	V
Input Leakage Current (Digital Inputs)		-	-	10	µA
Output Leakage Current (High-Z Digital Outputs)		-	-	10	µA

**SWITCHING CHARACTERISTICS - PROGRAMMABLE I/O**

(T<sub>A</sub> = 25 °C; V<sub>A</sub>, V<sub>D</sub> = 5V ±5%; Inputs: logic 0 = DGND, logic 1 = V<sub>D</sub>, C<sub>L</sub> = 30 pF)

Parameters	Symbol	Min	Typ	Max	Units
Output Rise Time	t <sub>rpo</sub>	-	200	-	ns
Output Fall Time	t <sub>fpo</sub>	-	200	-	ns

## 2. TYPICAL CONNECTION DIAGRAMS

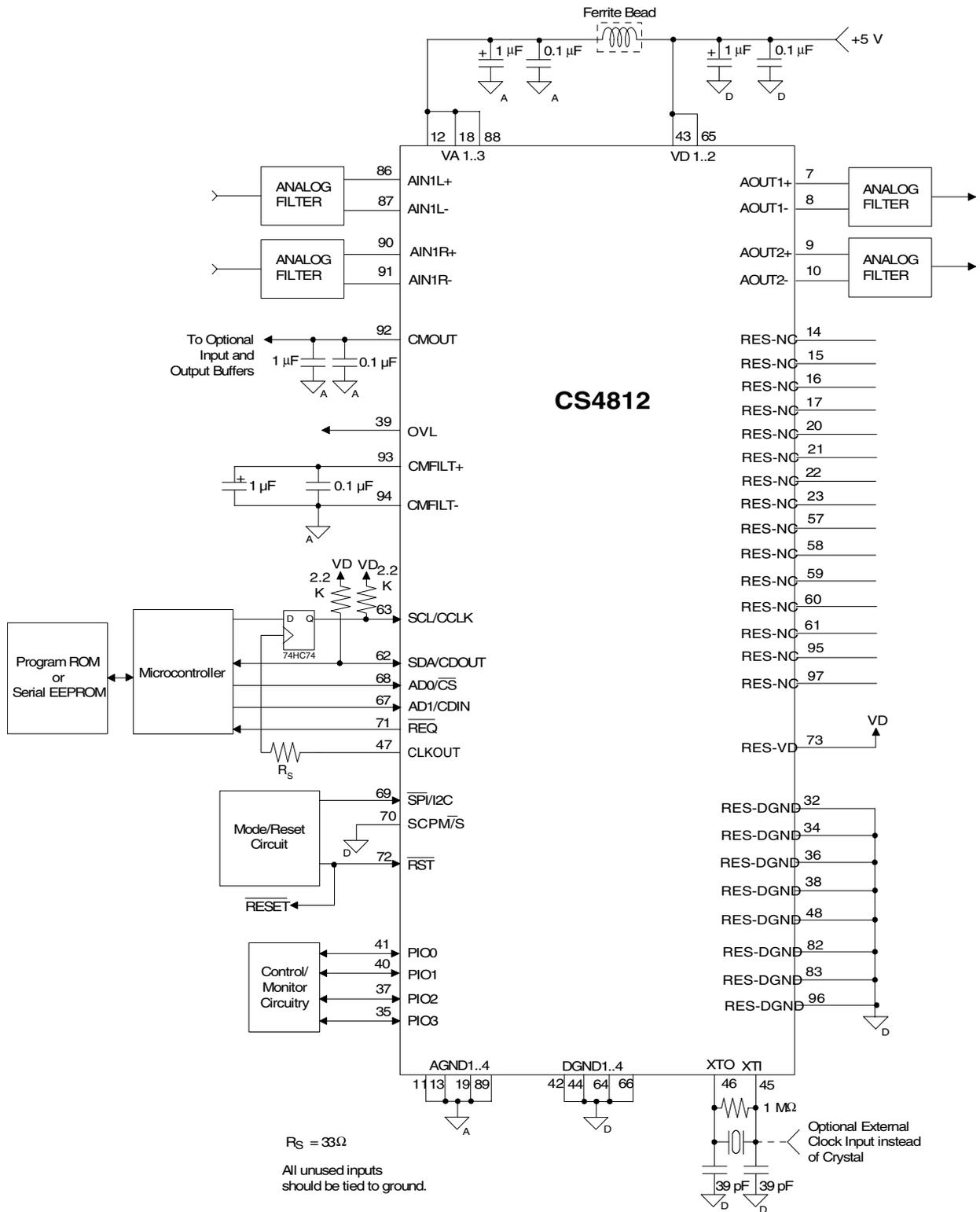
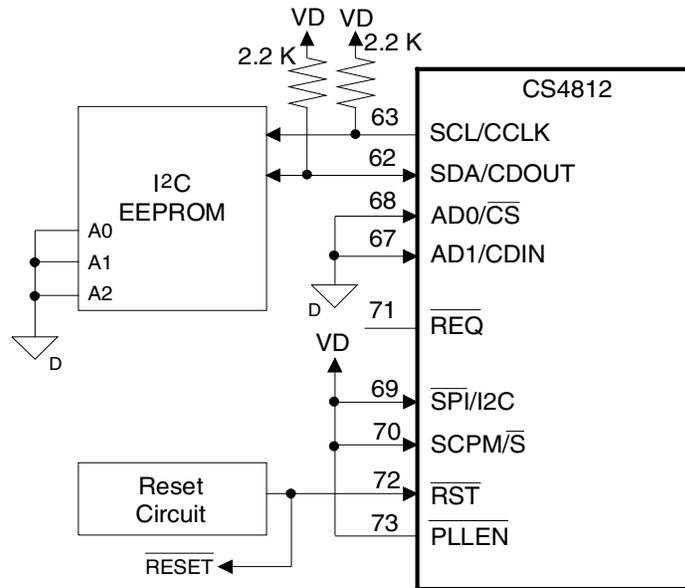
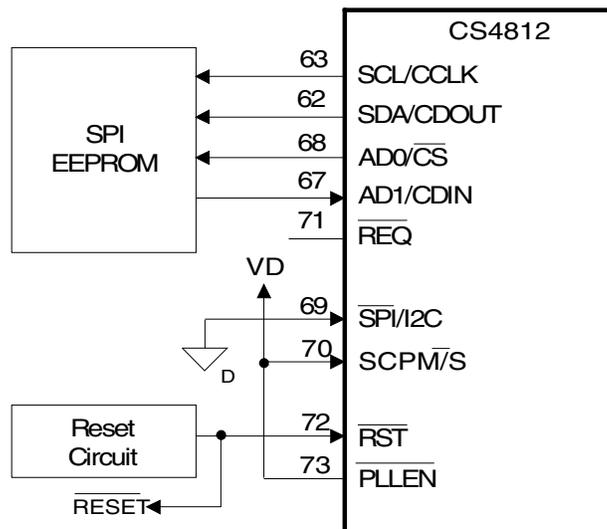


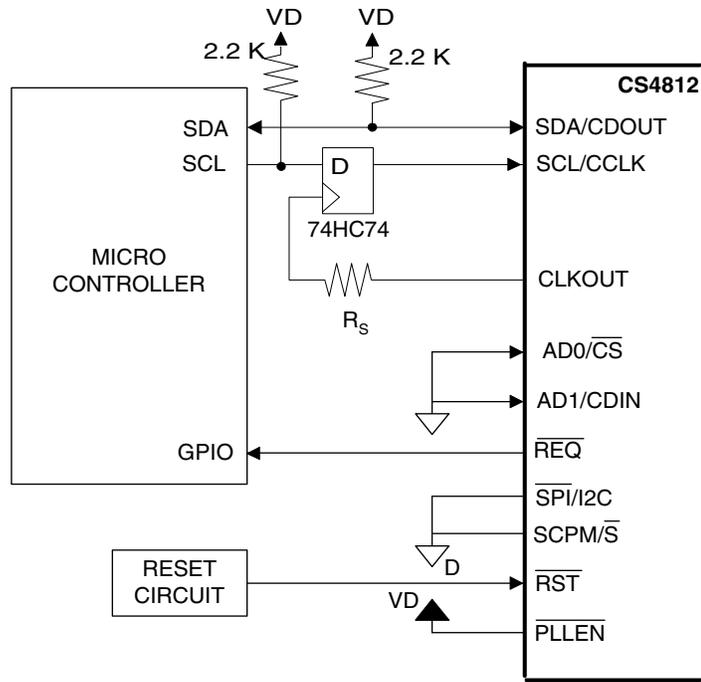
Figure 5. Typical Connection Diagram, Control Port Slave Mode



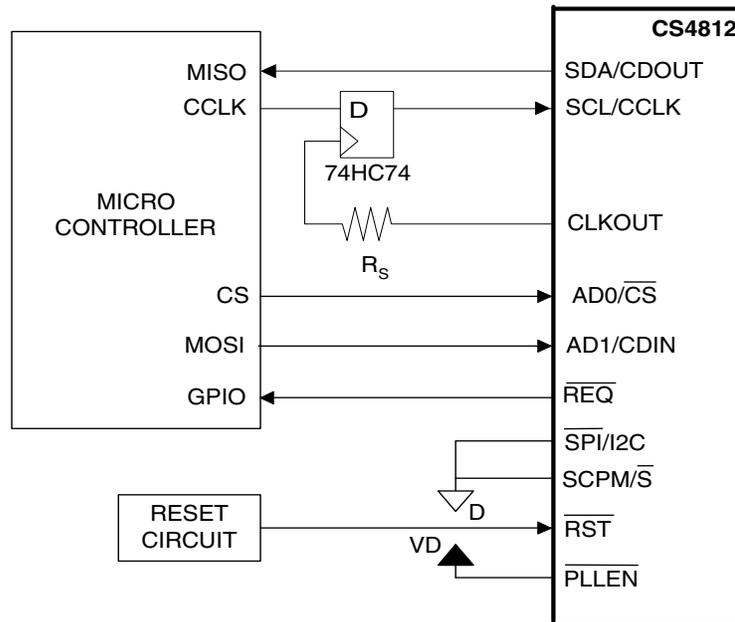
**Figure 6. Typical Connection Diagram, Control Port I<sup>2</sup>C Master Mode**



**Figure 7. Typical Connection Diagram, Control Port SPI Master Mode**



**Figure 8. Typical Connection Diagram, Control Port I<sup>2</sup>C Slave Mode**



**Figure 9. Typical Connection Diagram, Control Port SPI Slave Mode**

### 3. FUNCTIONAL DESCRIPTION

#### 3.1 Overview

The CS4812 is a complete audio subsystem on a chip, integrating an DSP with on-chip RAM, two 24-bit ADCs, two 24-bit DACs, and a serial control port.

The sigma-delta ADCs include linear phase digital anti-aliasing filters and only require a single-pole external passive filter.

The sigma-delta DACs include analog switched-capacitor anti-image filters and require an external second or third order active filter that can be easily integrated into an output differential-to-single-ended converter circuit.

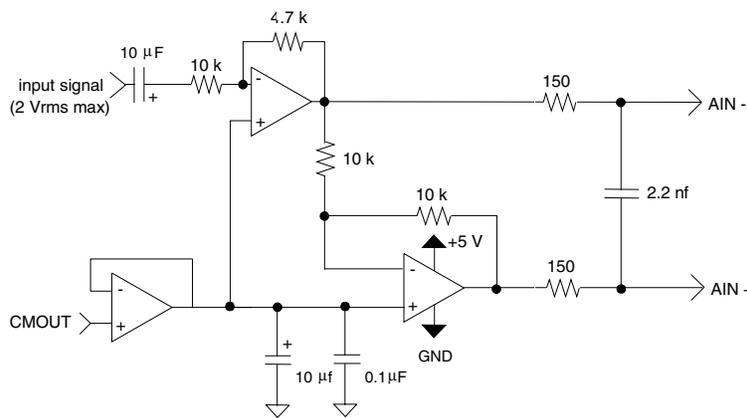
The serial control port is designed to accommodate I<sup>2</sup>C<sup>®</sup> or SPI interfaces and can operate in master or slave mode. It allows interfacing to external non-volatile memory for stand-alone operation or to a host-controller for real-time control. All communications between the DSP and an external EEPROM or host-controller are handled through the serial control port.

#### 3.2 Analog Inputs

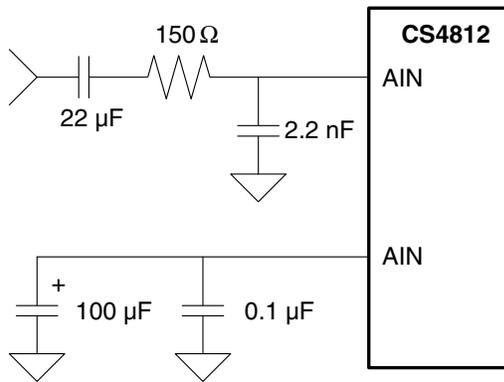
##### 3.2.1 Line Level Inputs

AINR+, AINR-, AINL+, and AINL- are the line level analog inputs (See Figure 5). These pins are internally biased to the CMOUT voltage of 2.3 V. A DC blocking capacitor placed in series with the input pins allows signals centered around 0 V to be input to the CS4812. Figure 5 shows operation with a single-ended input source. This source may be supplied to either the positive or negative input as long as the unused input is connected to ground through capacitors as shown. When operated with single-ended inputs, distortion will increase at input levels higher than -1 dBFS. If better performance is required, a single-ended-to-differential converter, shown in Figure 10, may be used. It provides unity gain, DC blocking and anti-alias filtering.

Inputs may be externally AC or DC coupled. This permits use of the ADCs for input of audio signals or for measurement of DC control voltages. By default, an internal high pass filter removes any DC offsets from both of the ADC inputs. If measurement of DC is required on either of the ADC inputs, then the on-chip high pass filter must be disabled. Analog audio input signals that are DC coupled must be biased at 2.3 V to maintain proper input



**Figure 10. Recommended Line Input Buffer**



**Figure 11. Single Ended Input**

signal swing. DC control input voltages may range from ground to Vcc.

ADC output data is in twos-complement binary format. For inputs above full scale, the ADC digital output saturates. The OVL output pin asserts when the analog input is out-of-range.

### 3.2.2 Digital High Pass Filter

In DC coupled systems, a small DC offset may exist between the input circuitry and the A/D converters. The CS4812 includes a defeatable high pass filter after the decimator to remove these DC components. The high pass filter response is given in “High Pass Filter Characteristics” on page 4 and scales linearly with sample rate. In applications where DC level measurement is required, as would occur when one of the ADC inputs is used for measurement of DC control voltages, the high pass filter may be disabled via a control port register. Note: The high pass filter defeat operates on both ADC inputs simultaneously therefore external DC blocking must be provided in the design of the analog audio input circuit.

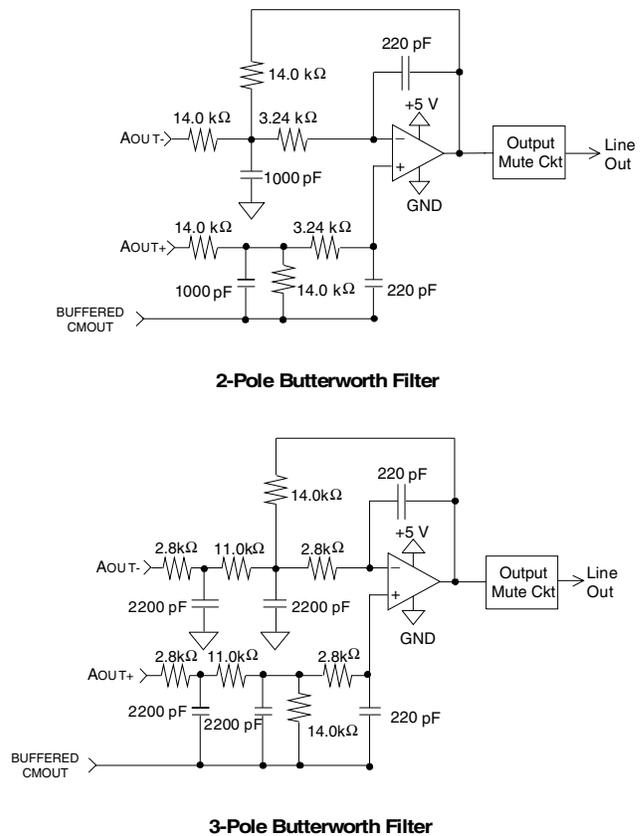
## 3.3 Analog Outputs

### 3.3.1 Line Level Outputs

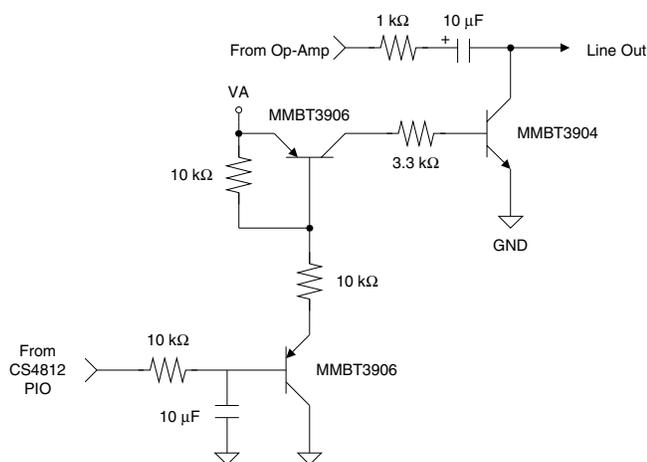
The CS4812 contains on-chip differential buffer amplifiers that produce line level outputs capable

of driving 10 kΩ loads to full scale. These amplifiers internally biased to the CMOUT voltage of 2.3 V.

The recommended off-chip analog filter is a second order Butterworth with a 3 dB corner at Fs. A third order Butterworth filter with a -3 dB corner at 0.75 Fs can be used if greater out of band noise filtering is desired. These filters can be easily integrated into a differential-to-single-ended converter circuit as shown in the 2-pole and 3-pole Butterworth filters of Figure 12. The hardware mute circuit referenced in Figure 12 is shown in Figure 13. Hardware muting is recommended on power-up and power-down.



**Figure 12. Butterworth Output Filters**



**Figure 13. Output Mute Circuit**

### 3.4 Clock Generation

The CS4812 master clock may be generated by using the on-chip oscillator with an external crystal or may be derived from an external clock source.

#### 3.4.1 Clock Source

The CS4812 requires a 256 Fs master clock to run the internal logic. The two possible clock sources are the on-chip crystal oscillator or an external clock input to the XTI pin.

When using the on-chip crystal oscillator, external loading capacitors are required. (see Figure 5) High frequency crystals (>8 MHz) should be parallel resonant, fundamental mode and designed for 20 pF loading. (equivalent to 40 pF to ground on each leg)

### 3.5 Serial Control Port

The serial control port contains all of the main control logic for the chip. It controls power-on sequencing, hardware configuration and DSP operation. In AutoBoot mode, the serial control port manages the entire boot process including initialization of its own hardware configuration registers from EEPROM, code download from the EEPROM to the DSP and initialization of the CODEC. In host-controlled mode, the host-device ini-

tializes the hardware configuration registers and downloads the application code to the DSP via 2 dedicated control port registers. Application messaging between the host and the DSP is also done via these control port registers. The operation of the control port may be completely asynchronous to the audio sample rate. However, it is recommended that the control port pins remain static when not in use.

The required control port register settings are contained in the Crystal effects firmware application code EEPROM image.

The control port supports the SPI bus and the I<sup>2</sup>C<sup>®</sup> bus in both master and slave modes. The bus interface is selected via the  $\overline{\text{SPI/I}^2\text{C}}$  pin and the master/slave mode is selected via the  $\text{SCPM}/\overline{\text{S}}$  pin. These pins are sampled during de-assertion of the  $\overline{\text{RST}}$  pin.

Master mode is selected for stand-alone operation when AutoBooting from an external serial EEPROM. Slave mode is selected when the CS4812 is connected to an external host controller.

#### 3.5.1 SPI Bus

The SPI bus interface consists of 5 digital signals, CCLK, CDIN, CDOUT,  $\overline{\text{CS}}$  and  $\overline{\text{REQ}}$ . CCLK, the control port bit clock, is used to clock individual data bits. CDIN, the control data input, is the serial data input line to the CS4812. CDOUT, the control data output, is the output data line from the CS4812. It is open-drain and requires a 2.2 kΩ pull-up resistor.  $\overline{\text{CS}}$ , the chip select signal, is asserted low to enable the SPI port.  $\overline{\text{REQ}}$ , the request pin, is used by the DSP to request a read by a host controller when operating in control port slave mode. Data is clocked into the chip on the rising edge of CCLK and out on the falling edge. When in slave mode, the CLK signal must be synchronous with the internal DSP clock. An external D flip flop off of CLKOUT as shown in Figure 9 can be used to retime the CLK signal. There is limited drive capability on CLKOUT so

a buffer may be required to minimize the capacitive loading on CLKOUT.

CCLK and  $\overline{CS}$  may be inputs or outputs with respect to the CS4812. If the serial control port of the CS4812 is defined as the master, then CCLK and  $\overline{CS}$  are outputs and CCLK requires a 2.2 k $\Omega$  pull-up resistor. If the CS4812 is defined as the slave, then CCLK and  $\overline{CS}$  are inputs and no pull-up resistor is required on CCLK.

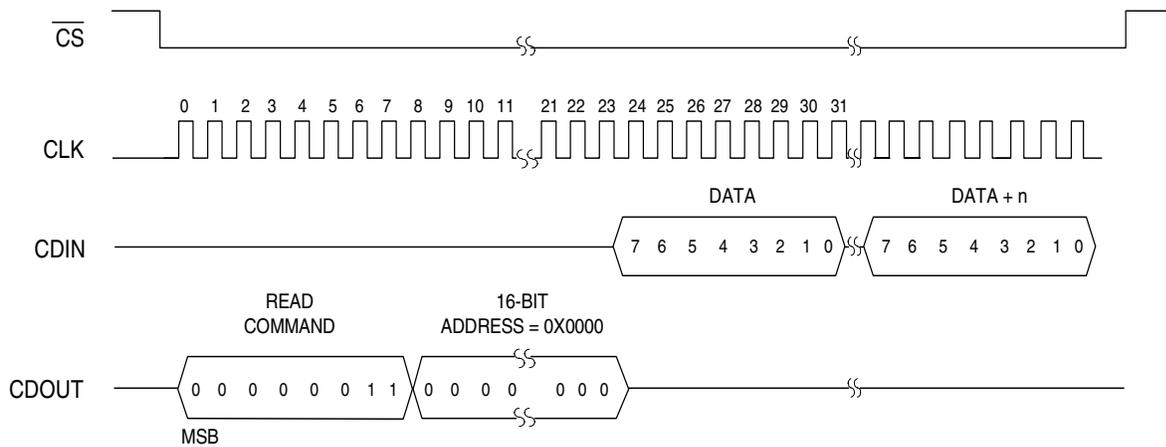
**3.5.1.1 SPI Master Mode**

The SPI master mode is designed for read-only operation during AutoBooting from a serial EEPROM. A typical AutoBoot sequence with a Xicor X25650 serial EEPROM, or equivalent, is shown in Figure 14. On exit from reset, the CS4812 asserts  $\overline{CS}$ .

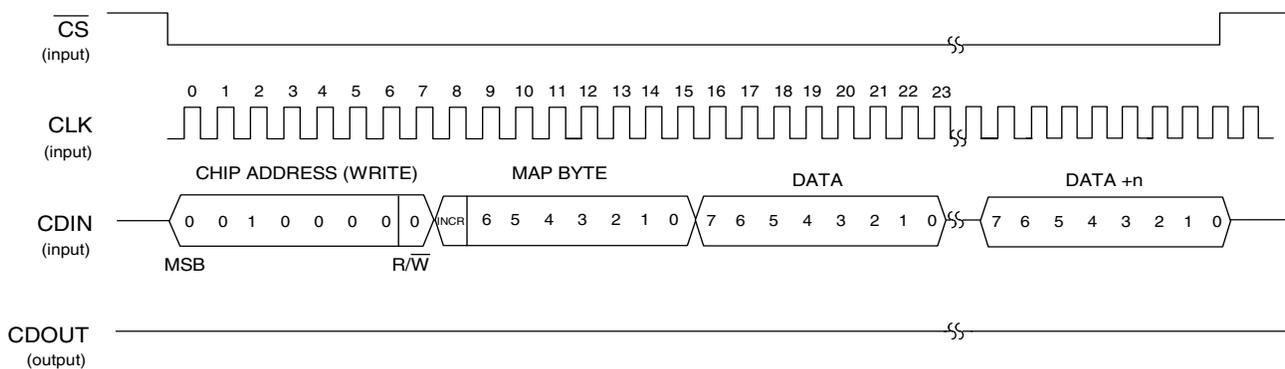
The 8-bit read instruction (00000011) is sent to the EEPROM followed by a pre-defined 16-bit start address. The CS4812 then automatically clocks out sequential bytes from the EEPROM until the last byte has been received. After the last byte is received, the CS4812 deasserts  $\overline{CS}$  and begins program execution. At this point, the serial control port becomes inactive until the next reset.

**3.5.1.2 SPI Slave Mode**

In SPI slave mode, a write sequence from an external host controller is shown in Figure 15. The host controller asserts  $\overline{CS}$  and sends a 16-bit write preamble to the CS4812. This preamble consists of a 7-bit chip address (must be 0010000) followed by a one-bit R/W (Read/Write) bit (set to 0 for write)

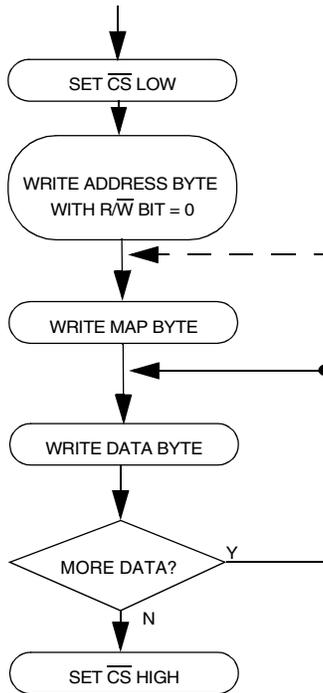


**Figure 14. Control Port Timing, SPI Master Mode AutoBoot**



**Figure 15. Control Port Timing, SPI Slave Mode Write**

and a memory address pointer (MAP) byte. The MAP byte contains the address of the control port register to be accessed. Following the preamble, the host controller sends the actual data byte to be written to the register designated by the MAP. The host controller then de-asserts  $\overline{CS}$ . Figure 16 shows the SPI slave mode write flow diagram.

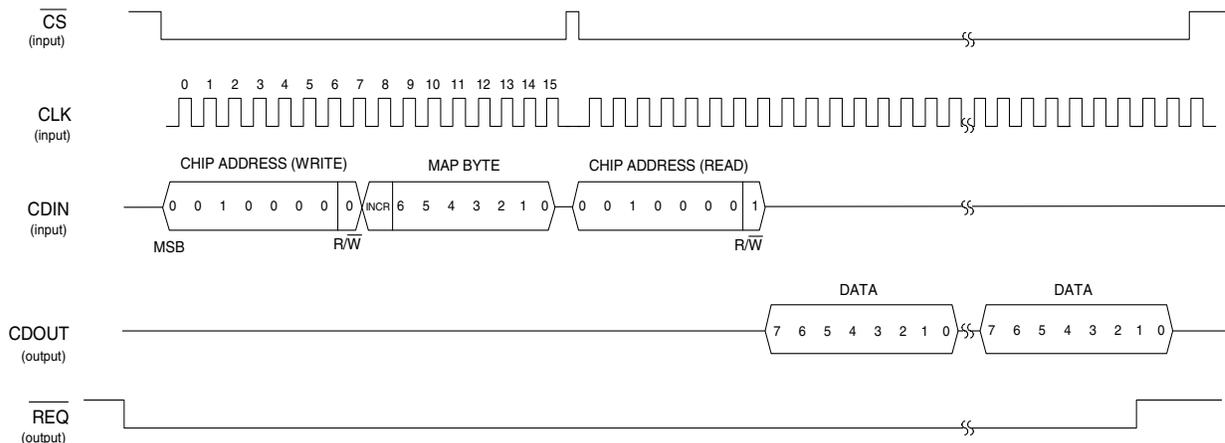


**Figure 16. SPI Slave Write Flow Diagram**

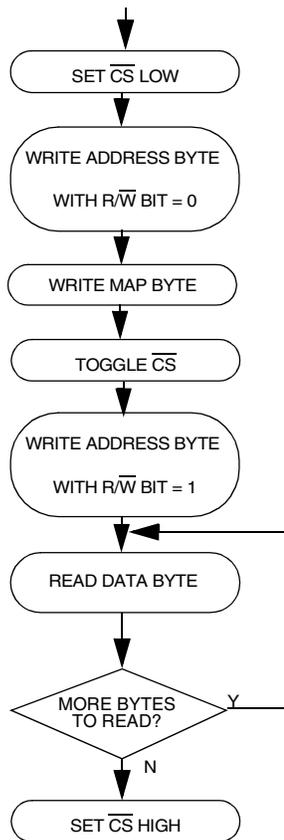
In SPI slave mode, a read sequence from an external controller is shown in Figure 17. The host controller executes a partial write-cycle by sending a 16-bit write preamble to the CS4812 with the MAP byte set to the address of the control port byte register to be read. The host controller then de-asserts  $\overline{CS}$ , re-asserts  $\overline{CS}$ , and sends the 7-bit chip address followed by the R/W bit set to 1. The host controller then clocks out the control port register designated by the MAP byte. The host controller then de-asserts  $\overline{CS}$ . Figure 18 shows the SPI mode slave read flow diagram initiated by the host microcontroller. Figure 19 shows the SPI slave mode read flow diagram incorporating the DSP  $\overline{REQ}$  signal.  $\overline{REQ}$  is used to notify the host controller that a data byte from the DSP is waiting to be read.

The behavior of the  $\overline{REQ}$  signal is dependent on when data is written to the serial control port output register in relation to CCLK and bit 2 of the current byte being transferred. There are three cases of  $\overline{REQ}$  behavior:

1. The  $\overline{REQ}$  line will be de-asserted immediately following the rising edge of CCLK on the D2 bit of the current byte being transferred if there is no data in the serial control port output register. The  $\overline{REQ}$  line remains de-asserted and a stop condition



**Figure 17. Control Port Timing, SPI Slave Mode Read**

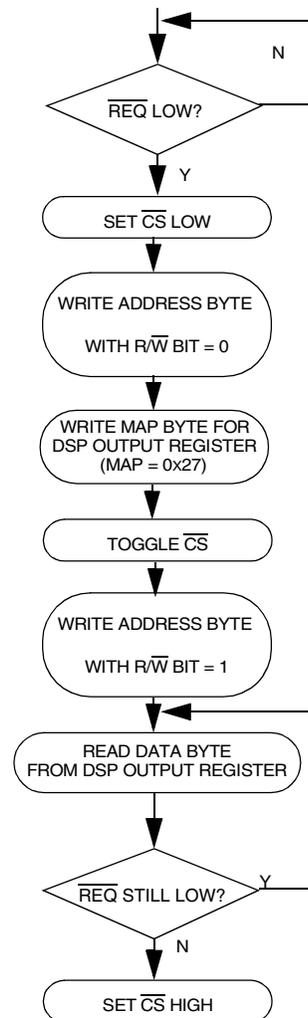


**Figure 18. SPI Slave Mode Read Flow Diagram**

should be issued by the bus master, thus completing the transfer.

2. If data is written to the serial control port output register prior to the rising edge of CCLK for the D2 data bit,  $\overline{REQ}$  will remain asserted. The bus master should continue to shift out this new byte.

3. If data is placed in the SCP output register by the DSP after the rising edge of CCLK for the D2 bit,  $\overline{REQ}$  will be immediately re-asserted, thus creating a pulse on  $\overline{REQ}$ . The byte in the SCP out register may be read by the bus master as part of the current transaction or may be read later as part of a new read transaction.



**Figure 19. SPI Slave Mode Read from DSP Core Flow Diagram using DSP REQ**

The CS4812 has a MAP auto increment capability which allows block reads or writes of successive control port registers. This feature is enabled by setting the INCR bit in the MAP byte.

During a write sequence, multiple bytes may be written by continuing to send data bytes to the CS4812 after the first data byte and before de-asserting  $\overline{CS}$ . If auto increment is disabled, the last data byte sent will appear in the register designated by the MAP. If auto increment is enabled, data bytes sent following the first data byte will be written to successive registers following that designated in the MAP.

During a read sequence, multiple bytes may be read by continuing to clock out data bytes to the CS4812 after the first data byte and before de-asserting  $\overline{CS}$ . If auto increment is disabled, the last data byte read will be the register designated by the MAP. If auto increment is enabled, data bytes read following the first data byte will be read from successive registers following that designated in the MAP.

### 3.5.2 I<sup>2</sup>C Bus

The I<sup>2</sup>C bus interface implemented on the CS4812 consists of 3 digital signals, SCL, SDA and  $\overline{REQ}$ . SCL, or serial clock, is used to clock individual data bits. SDA, or serial data, is a bidirectional data line.  $\overline{REQ}$ , the request pin, is used by the DSP to request a host read when operating in control port slave mode. Two additional pins, AD1 and AD0, are inputs which determine the 2 lowest order bits of the 7-bit I<sup>2</sup>C device address.

SCL may be defined as an input or an output with respect to the CS4812. If the serial control port of the CS4812 is defined as the master, then SCL is an open-drain output and requires a pull-up resistor as shown in Figure 5. Conversely, if the serial control port of the CS4812 is defined as the slave, then SCL is an input.

SDA carries time-multiplexed bidirectional serial data. It is open-drain and requires a pull-up resistor as shown in Figure 5.

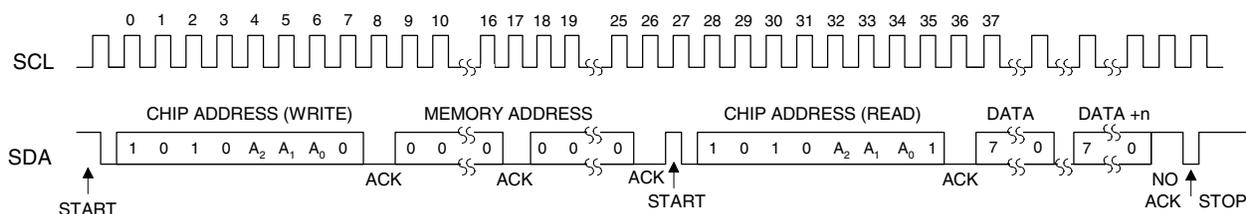
AD1 and AD0, the inputs which determine the 2 lowest order bits of the 8-bit I<sup>2</sup>C device address, are meaningful only when the CS4812 is operating as

a slave device and may be tied to ground when the CS4812 is configured for master mode.

When operating in control port slave mode, the  $\overline{REQ}$  output pin is used by the CS4812 DSP to request communication with the master.

#### 3.5.2.1 I<sup>2</sup>C Master Mode

The I<sup>2</sup>C master mode is designed for read-only operation during AutoBooting from a serial EEPROM. A typical AutoBoot sequence with a Microchip X24256 serial EEPROM, or equivalent, is shown in Figure 20. On exit from reset, the CS4812 sends an initial write preamble to the EEPROM which consists of a I<sup>2</sup>C start condition and the slave address byte. The slave address consists of the 4 most significant bits set to 1010, the following 3 bits corresponding to the device select bits, A<sub>2</sub>, A<sub>1</sub> and A<sub>0</sub> set to 000 and the last bit (R/W) set to 0. Following this, a 2-byte EEPROM starting address of 0x0000 is sent to the EEPROM. The 2-byte EEPROM starting address uses only the lowest 13 bits and sets the highest 3 bits to zero. To begin reading from the EEPROM, the CS4812 sends another start condition followed by a read preamble. The read preamble is identical to the write preamble except for the state of the R/W bit. The CS4812 then automatically clocks out sequential bytes from the EEPROM until the last byte has been received. These bytes include initial values for all control port registers as well as the DSP application code. After the last byte, the CS4812 initiates a stop condition and begins program execution. At this point, the serial control port becomes inactive until the next reset. Actual EE-



**Figure 20. Control Port Timing, I<sup>2</sup>C Master Mode AutoBoot**

PROM memory mapping is handled automatically by the development tools and is transparent to the designer.

3.5.2.2 I<sup>2</sup>C Slave Mode

In I<sup>2</sup>C slave mode, a write sequence from an external host controller is shown in Figure 22.. The host controller sends a write preamble consisting of a start condition followed by the slave address for the CS4812. The slave address byte consists of a 7-bit address field (00100|AD1|AD0) followed by a Read/Write bit (set to 0). AD1 and AD0 correspond to the logic levels applied to the these pins on the CS4812. The host controller then sends a MAP byte which contains the address of the control register to be accessed followed by the actual data byte to be written to the register designated by the MAP. Upon completion of this, the host controller then sends a stop condition to complete the transaction. Figure 21 shows the I<sup>2</sup>C slave mode write flow diagram

In I<sup>2</sup>C slave mode, a read sequence by an external host controller is shown in Figure 23. The host controller sends a write preamble to the CS4812 which

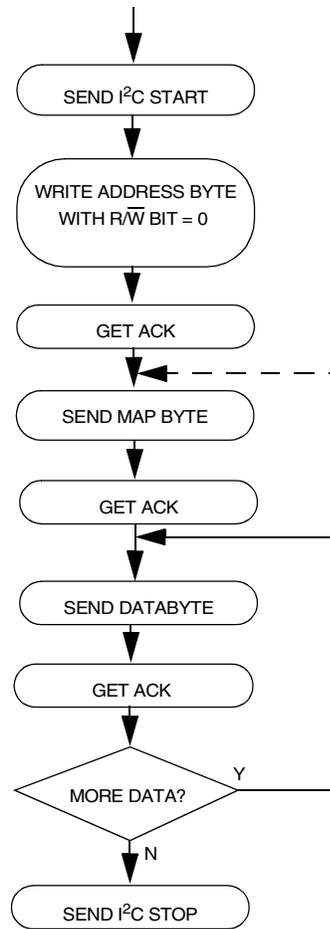


Figure 21. I<sup>2</sup>C Slave Mode Write Flow Diagram

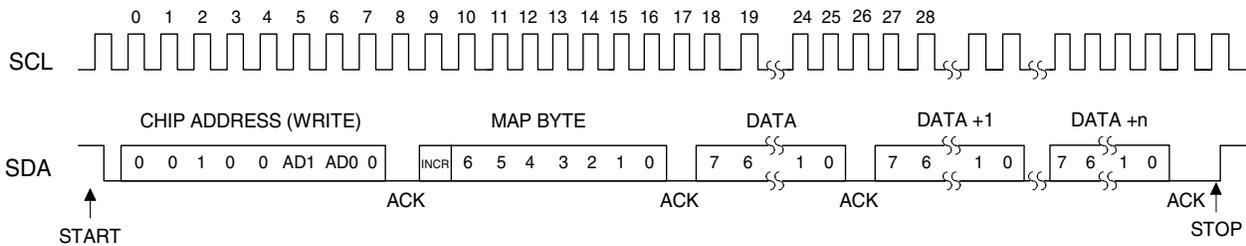


Figure 22. Control Port Timing, I<sup>2</sup>C Slave Mode Write

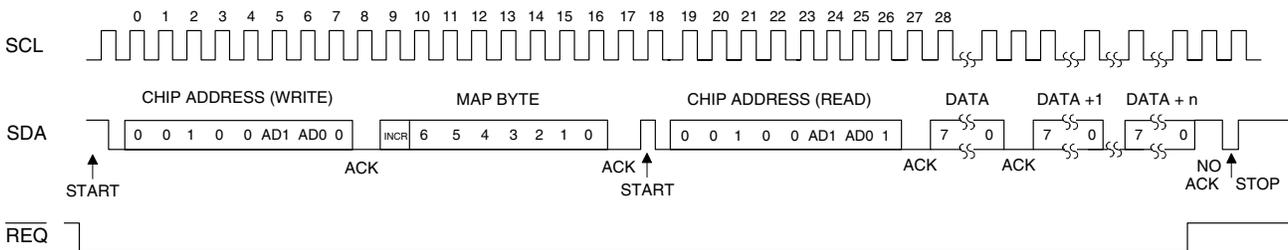


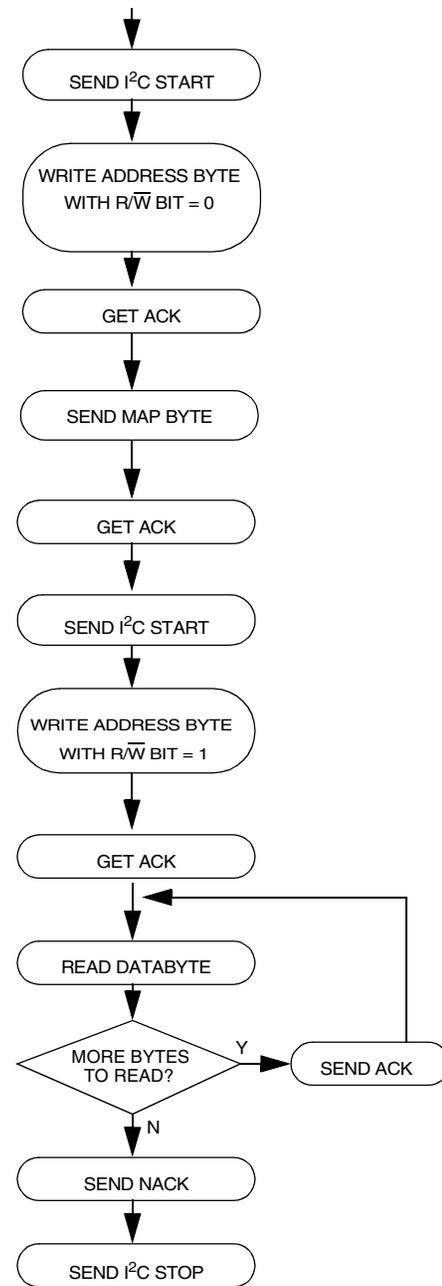
Figure 23. Control Port Timing, I<sup>2</sup>C Slave Mode Read

consists of a start condition followed by its slave address byte with the Read/Write bit set to 0. The host controller then initiates a read preamble. The read preamble is identical to the write preamble except for the state of the Read/Write bit. The host controller then sends a MAP byte which contains the address of the control register to be accessed. After receiving the MAP byte, the CS4812 returns the contents of this register to the host controller. The host controller may continue reading registers by sending additional MAP bytes or complete the transaction by initiating a stop condition. Figure 24 shows the SPI mode slave read flow diagram initiated by the host microcontroller. Figure 25 shows the I<sup>2</sup>C slave mode read flow diagram incorporating the DSP  $\overline{\text{REQ}}$  signal.  $\overline{\text{REQ}}$  is used to notify the host controller that a data byte from the DSP is waiting to be read.

The behavior of the  $\overline{\text{REQ}}$  signal is dependent on when data is written to the SCP output register in relation to SCL and bit 1 of the current byte being transferred. There are three cases of  $\overline{\text{REQ}}$  behavior:

1. The  $\overline{\text{REQ}}$  line will be de-asserted immediately following the rising edge of SCL on the D1 bit of the current byte being transferred if there is no data in the SCP output register. The  $\overline{\text{REQ}}$  line remains de-asserted and a stop condition should be issued by the bus master, thus completing the transfer.
2. If data is written to the SCP output register prior to the rising edge of SCL for the D1 bit,  $\overline{\text{REQ}}$  will remain asserted. The bus master should continue to shift out this new byte.
3. If data is placed in the SCP output register by the DSP after the rising edge of SCL for the D1 bit,  $\overline{\text{REQ}}$  will be immediately re-asserted, thus creating a pulse on  $\overline{\text{REQ}}$ . The byte in the SCP out register may be read by the bus master as part of the current transaction or may be read later as part of a new read transaction.

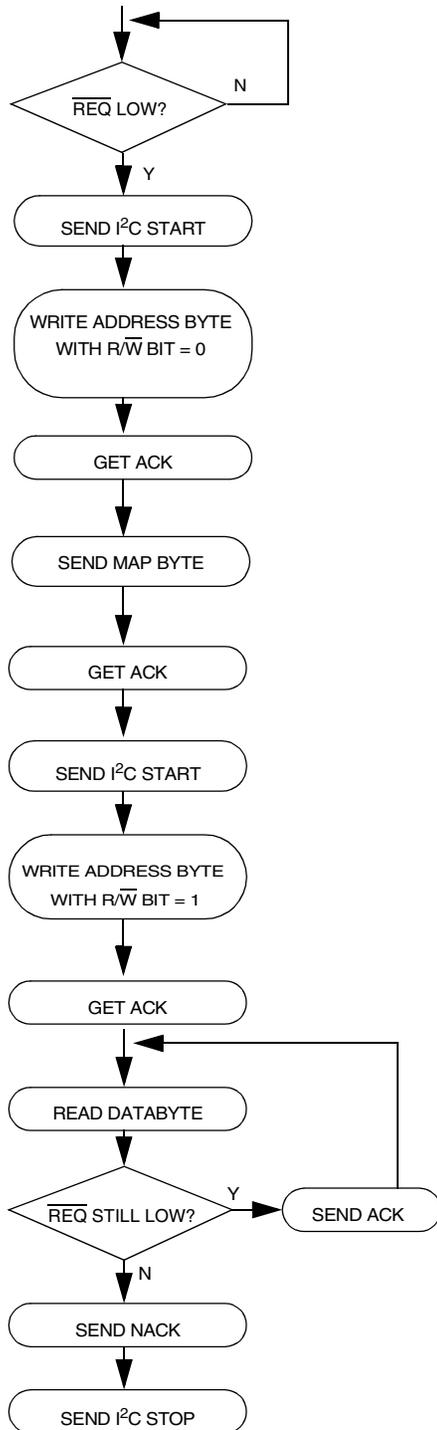
The CS4812 has a MAP auto increment capability which allows block reads or writes of successive



**Figure 24. I<sup>2</sup>C Slave Mode Read Flow Diagram**

control port registers. This feature is enabled by setting the INCR bit in the MAP byte.

During a write sequence, multiple bytes may be written by continuing to send data bytes to the CS4812 after the first data byte and before initiating a stop condition. If auto increment is disabled, the last data byte sent will appear in the register designated by the MAP. If auto increment is en-



**Figure 25. I<sup>2</sup>C Slave Mode Read from DSP Core Flow Diagram with DSP REQ**

abled, data bytes sent following the first data byte will be written to successive registers following that designated in the MAP.

During a read sequence, multiple bytes may be read by continuing to clock in data bytes to the CS4812 after the first data byte and before initiating a stop condition. If auto increment is disabled, the last data byte read will be the register designated by the MAP. If auto increment is enabled, data bytes read following the first data byte will be read from successive registers following that designated in the MAP.

### 3.6 Boot Modes

There are two different techniques that allow the system to load the application code into the CS4812. The first technique is called, “AutoBoot” and allows the application code to be loaded from an external serial EEPROM with an I2C or SPI interface. This technique is used in system applications that do not have a host. The second technique is called, “Host Boot” and allows the application code to be loaded directly from the host microcontroller via I2C or SPI communication interface. This method may eliminate the need for an external EEPROM.

#### 3.6.1 AutoBoot

The AutoBoot method simply requires an external EEPROM with an I<sup>2</sup>C or SPI serial bus interface. The DSP, automatically loads and runs the application code resident in the EEPROM upon deassertion of the  $\overline{\text{RESET}}$  line. It should be noted that this technique is used for systems that do not have a microcontroller and do not require real-time adjustment of the application code parameters. Please refer to Table 10 on page 6 for the timing requirements of the  $\overline{\text{RESET}}$  line.

#### 3.6.2 HostBoot

By using the HostBoot technique, an external microcontroller is required to download the applica-

tion code. This technique allows for real-time control of all parameters specific to the application code. Please refer to Figure 26 for the HostBoot procedure flow chart and to Section 1.2.1 of AN195 for an example of a host boot sequence.

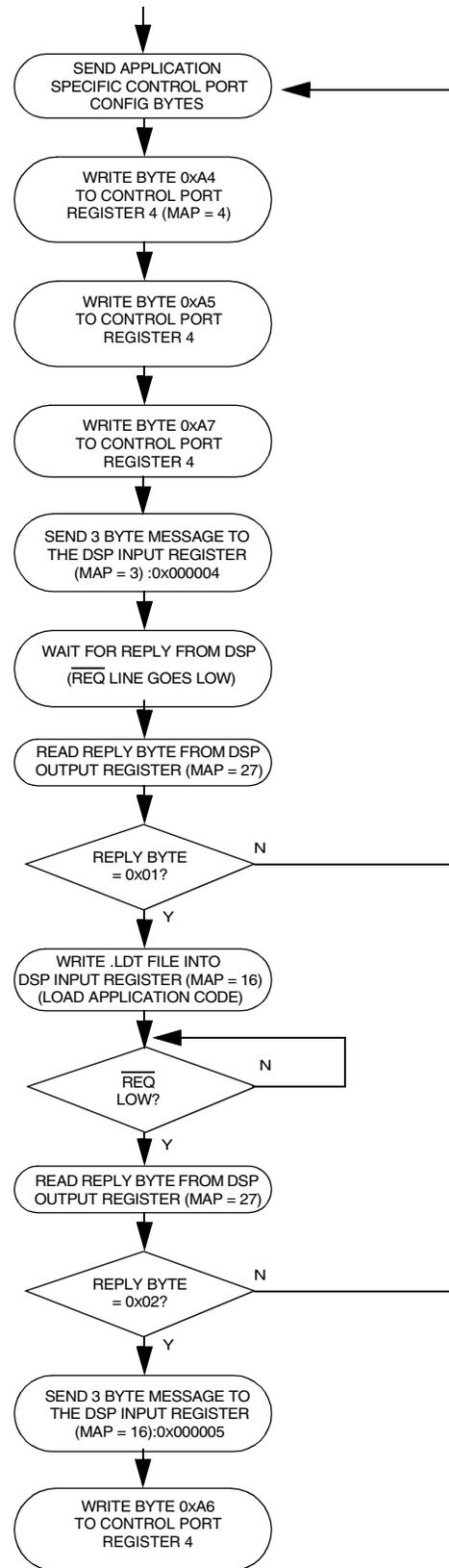
**3.7 Resets**

There are several reset mechanisms in the CS4812 which affect different parts of the chip. Full chip reset can only be achieved by asserting the external  $\overline{RST}$  pin. With  $\overline{RST}$  asserted, the chip enters low power mode during which the control port, CODEC and DSP are reset, all registers are returned to their default values and the DAC outputs are muted. The  $\overline{RST}$  pin should be asserted during power-up until the power supplies have reached steady state.

If the supply voltage drops below 4 Volts, the CODEC is reset, the DAC outputs are muted and the DSP automatically executes a soft reset.

Upon exit from a CODEC reset, the DSP restarts the application code and the CODEC performs the following procedure:

- The CODEC resynchronizes.
- The DAC outputs unmute.



**Figure 26. HostBoot Flow Diagram**

#### 4. POWER SUPPLY AND GROUNDING

Proper layout and grounding is critical to obtaining optimal audio performance in your system. The most important rule to remember is to not allow currents from digital circuitry to couple into sensitive analog circuitry. This is generally done by using a separate or filtered power supply for the analog circuitry, physically separating the analog and digital components and traces in the pcb layout and using wide traces or planes for ground and power. One misplaced component or trace can severely degrade overall system performance.

When using separate supplies, the analog and digital power should be connected to the CS4812 via a ferrite bead, positioned closer than 1" to the device (see Figure 21). The CS4812 VA pin should be derived from the quietest power source available. If

only one supply is available, use the suggested arrangement in Figure 5.

A single solid ground plane is the simplest grounding scheme that works well in many cases. All analog and digital grounds shown in Figure 5 should be tied to the one plane.

Decoupling capacitors should be placed as close as possible to the device with the lowest value capacitor closest to the chip. Any power and ground connection vias should be placed near their respective component pins and should be attached directly to the appropriate plane. If traces are used for the power supplies to the CS4812, they should be as wide as possible to maintain low impedance.

It is recommended to solder the CS4812 directly to the printed circuit board. Soldering improves performance and enhances reliability

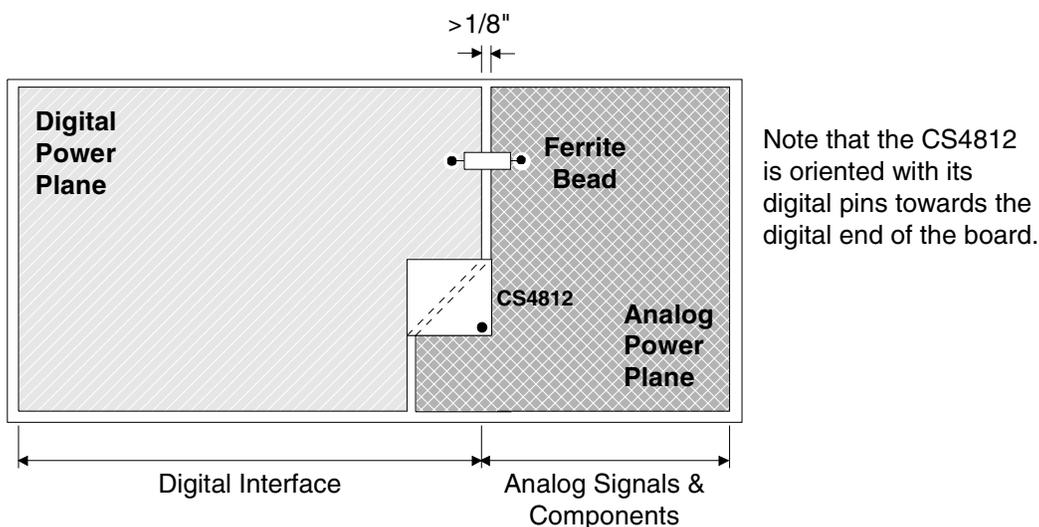
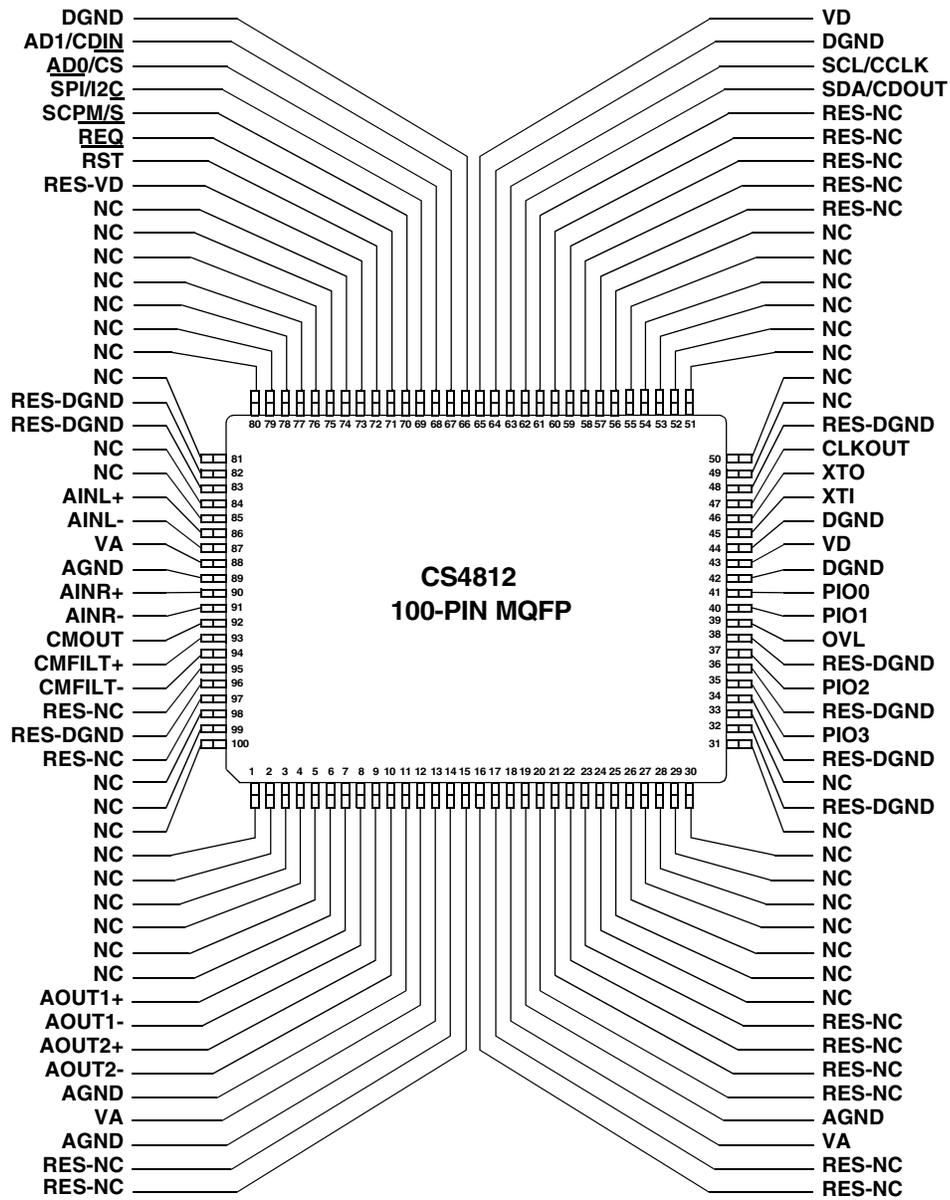


Figure 27. CS4812 Suggested Layout

**5. PIN DESCRIPTIONS**



**Figure 28. Pin Assignments**

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### Power Supply

**VA - Analog Power**

*Power:* analog supply, +5V.

**AGND - Analog Ground**

*Ground:* analog ground.

**VD - Digital Power**

*Power:* digital supply, +5V.

**DGND - Digital Ground**

*Ground:* digital ground.

### Analog Inputs

**AINL+/-, AINR+/- - Differential Analog Inputs**

*Inputs:* These pins accept differential analog input signals and are internally biased to the reference voltage of 2.3 V. The + and - input signals should be 180° out of phase. A single-ended signal may also be directly applied to either the + or - input with the other input AC coupled to ground through a capacitor. In general, differential input signals provide better performance. For best audio performance, a passive anti-aliasing filter is required. The typical connection diagram in Figure 5. shows the recommended single-ended input circuit. Figure 10 shows the recommended differential input circuit.

Inputs may be externally AC or DC coupled. This permits use of the ADCs for input of audio signals or for measurement of DC control voltages. By default, an internal high pass filter removes any DC offsets from both of the ADC inputs. If measurement of DC is required on either of the ADC inputs, then the internal high pass filter must be disabled. Analog audio input signals that are DC coupled must be biased at 2.3 V to maintain proper input signal swing. DC control input voltages may range from ground to Vcc and should be applied to only the + or - input with the other input coupled to ground through a capacitor.

**OVL - ADC Overload Indicator**

*Output:* This pin is asserted if either ADC is clipping. The pin does not latch and de-asserts when clipping stops.

### Analog Outputs

**AOUT1+/-, AOUT2+/- - Differential Audio Outputs**

*Outputs:* These pins output differential analog signals which are biased to the internal reference voltage of approximately 2.3V. The + and - output signals are 180° out of phase resulting in a nominal differential output voltage of twice the output pin voltage. For best performance, an anti-imaging filter is required. Figure 12 shows the recommended second and third order Butterworth differential-to-single-ended output buffer circuits.

### Voltage Reference

**CMOUT - Common Mode Output**

*Output:* This pin provides an internally generated reference of 2.3V to be used for biasing external analog circuitry. The load on CMOUT must be DC only, with an impedance of not less than 50 kΩ.

**CMFILT+, CMFILT- - Common Mode Filter Connections**

*Inputs:* These pins are connections for external filter components required by the internal common mode reference circuit. See the typical connection diagram in Figure 5. for details.

---

### Serial Control Port

#### **SCPM $\bar{S}$ - Serial Control Port Master/Slave Select**

*Input:* This pin configures the serial control port as a master if tied to VD or a slave if tied to DGND.

#### **SPI/I<sup>2</sup>C - Serial Control Port Format Select**

*Input:* This pin configures the control port for I<sup>2</sup>C format if tied to VD or SPI format if tied to DGND.

#### **SCL/CCLK - Serial Control Port Clock**

*Bidirectional:* This pin clocks serial control port data into and out of SDA in I<sup>2</sup>C mode. In SPI mode, it clocks control port data into CDIN and out of CDOUT. When the serial control port is configured as a master, SCL/CCLK is an output and is generated internally. When the serial control port is configured as a slave, SCL/CCLK is an input and may operate asynchronously to the master clock.

#### **AD0/ $\bar{CS}$ - I<sup>2</sup>C Address Bit 0 / SPI Chip Select**

*Bidirectional:* In I<sup>2</sup>C<sup>®</sup> mode, AD0 is an input and defines bit 0 of the partial chip address. The upper 5 bits of the 7-bit address must be 00100. In SPI mode,  $\bar{CS}$  is the chip select pin. When the serial control port is defined as a master in SPI mode,  $\bar{CS}$  is an output. When the serial control port is defined as a slave in SPI mode,  $\bar{CS}$  is an input.

#### **AD1/CDIN - I<sup>2</sup>C Address Bit 1 / SPI Data Input**

*Input:* In I<sup>2</sup>C<sup>®</sup> mode, AD1 is an input and defines bit 1 of the partial chip address. The upper 5 bits of the 7-bit address must be 00100. In SPI mode, CDIN is the serial control port data input and is clocked in on the rising edge of CCLK.

#### **SDA/CDOUT - I<sup>2</sup>C Data / SPI Data Output**

*Bidirectional:* In I<sup>2</sup>C<sup>®</sup> mode, SDA is the bidirectional data I/O line. In SPI mode, CDOUT is the serial control port data output and is clocked out on the falling edge of CCLK.

#### **REQ - DSP Output Request**

*Output:* This pin is used when the serial control port is configured for slave mode operation. This pin is asserted when the DSP has written a byte to a register in the control port. When this register is read by the master device, REQ is de-asserted.

### Clock and Crystal

#### **XTI, XTO - Crystal Oscillator Connections (Master Clock)**

*Input, Output:* These pins provide connections for an external parallel resonant quartz crystal. Alternately, an external clock source may be applied to XTI. The clock frequency must be 256xFs.

#### **CLKOUT - Clock Output**

*Output:* This pin provides a clock output which can be used to synchronize external components. Available output frequencies 1xFs, 128xFs and 256xFs are selectable via a control port register. The default frequency is 256xFs. It is recommended to externally buffer this signal with a CMOS gate as shown in Figure 5.

### Miscellaneous

#### **PIO0:3 - General Purpose Inputs/Outputs**

*Bidirectional:* These pins are general-purpose digital I/O pins. The Default state is input. The functionality of these pins after boot-up is determined by the application firmware code loaded into the device during the boot-up process.

#### **RST - Reset**

*Input:* This pin causes the device to enter a low power mode and forces all control port and i/o registers to be reset to their default values. The control port can not be accessed when reset is low.

**NC - No Connect**

*Input:* These pins are not internally connected and should be tied to ground for optimal performance.

**RES-NC - Reserved, No Connect**

These pins are reserved and must be left unconnected for normal operation.

**RES-VD - Reserved, Connect to VD**

These pins are reserved and must be tied to VD for normal operation.

**RES-DGND - Reserved, Connect to DGND**

These pins are reserved and must be tied to digital ground for normal operation.

**RES-AGND - Reserved, Connect to AGND**

These pins are reserved and must be tied to analog ground for normal operation.

## 6. PARAMETER DEFINITIONS

### Dynamic Range

The ratio of the full scale RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

### Total Harmonic Distortion + Noise

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1dBFS as suggested in AES 17-1991 Annex A.

### Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the RMS analog output level with 1kHz full scale digital input to the RMS analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

### Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the RMS sum of all the in-band harmonics of the test signal. Units in decibels.

### Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

### Frequency Response

A measure of the amplitude response variation from 20Hz to 20kHz relative to the amplitude response at 1kHz. Units in decibels.

### Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

### Gain Error

The deviation from the nominal full scale output for a full scale input.

### Gain Drift

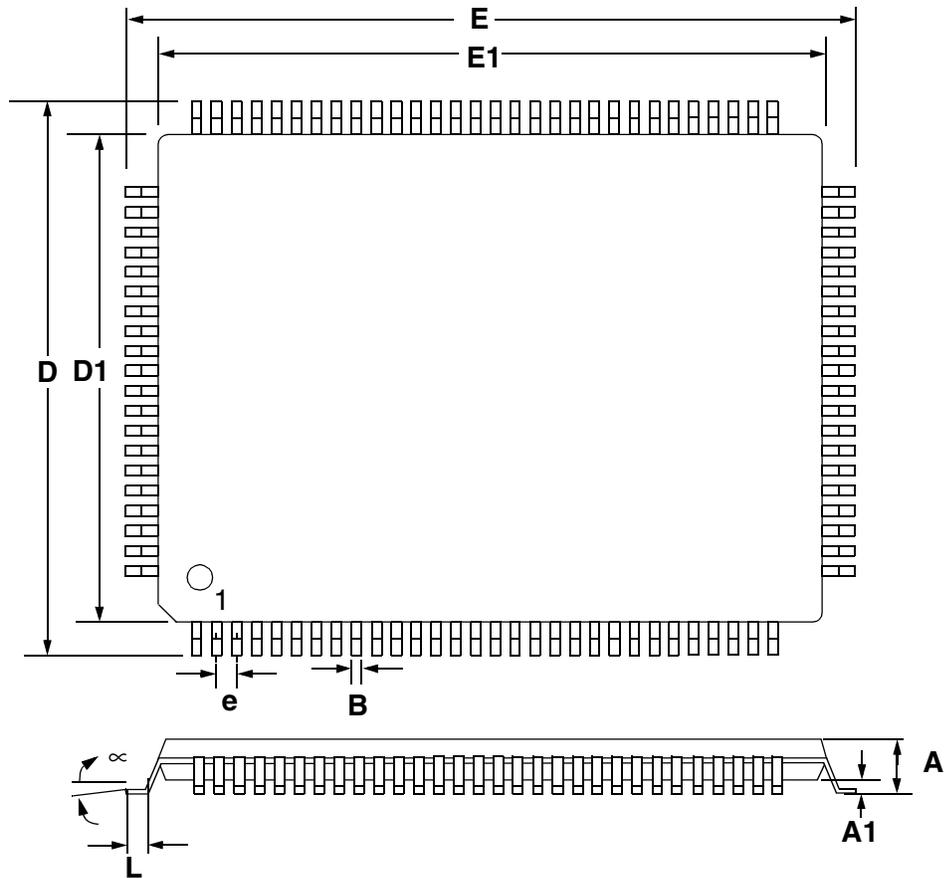
The change in gain value with temperature. Units in ppm/°C.

### Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input grounded. For the DACs, the deviation of the output from zero (relative to CMOUT) with mid-scale input code. Units are in volts.

7. PACKAGE DIMENSIONS

100L MQFP PACKAGE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.134	---	3.400
A1	0.010	0.014	0.250	0.350
B	0.009	0.015	0.220	0.380
D	0.667	0.687	16.950	17.450
D1	0.547	0.555	13.900	14.100
E	0.904	0.923	22.950	23.450
E1	0.783	0.791	19.900	20.100
e*	0.022	0.030	0.550	0.750
∞	0.000°	7.000°	0.00°	7.00°
L	0.018	0.030	0.450	0.750

\* Nominal pin pitch is 0.65 mm

Controlling dimension is mm.

JEDEC Designation: MS022

• **Notes** •

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