



W24512A

64K × 8 HIGH SPEED CMOS STATIC RAM

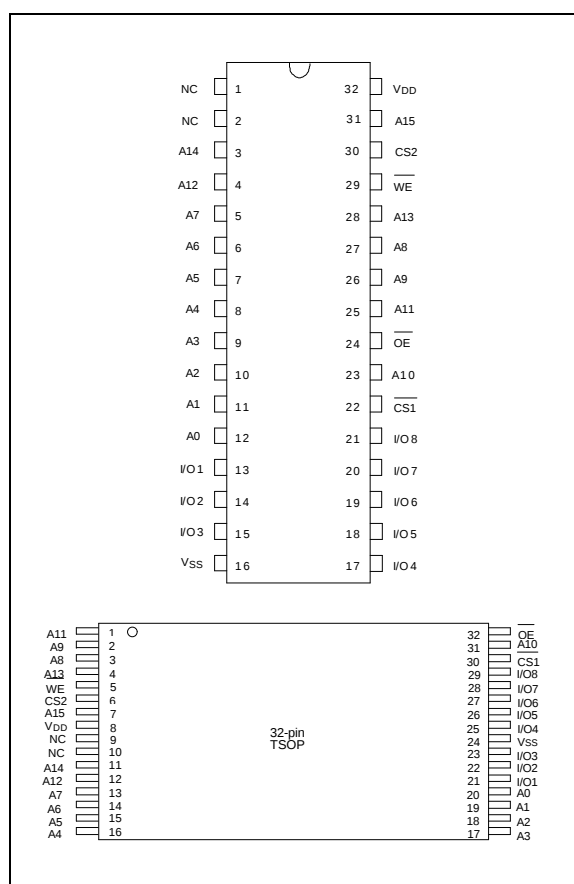
GENERAL DESCRIPTION

The W24512A is a high speed, low power CMOS static RAM organized as 65536 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

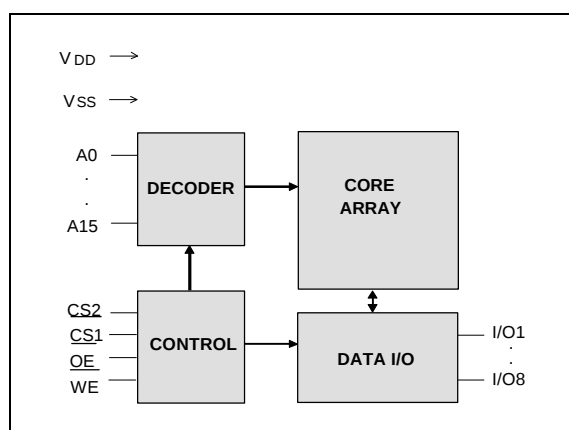
FEATURES

- High speed access time: 25 nS (max.)
- Low power consumption:
 - Active: 800 mW (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 32-pin 300 mil SOJ, 450 mil SOP, and standard type one TSOP (8 mm × 20 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0-A15	Address Inputs
I/O1-I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Inputs
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1- I/O8	V _{DD} CURRENT
H	X	X	X	Not Selected	High Z	ISB, ISB1
X	L	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	H	Output Disable	High Z	I _{DD}
L	H	L	H	Read	Data Out	I _{DD}
L	H	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +7.0	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V _{IH}	-	+2.2	-	V _{DD} +0.5	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} CS1 = V _{IH} (min.) or CS2 = V _{IL} (max.) or OE = V _{IH} (min.) or WE = V _{IL} (max.)	-10	-	+10	μA
Output Low Voltage	V _{OL}	I _{OL} = +8.0 mA	-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA	2.4	-	-	V
Operating Power Supply Current	I _{DD}	CS1 = V _{IL} (max.), CS2 = V _{IH} (min.) I/O = 0mA, Cycle = min Duty = 100%	-	-	160	mA
Standby Power Supply Current	ISB	CS1 = V _{IH} (min.) or CS2 = V _{IL} (max.) Cycle = min, Duty = 100%	-	-	30	mA
	ISB1	CS1 ≥ V _{DD} -0.2V or CS2 ≤ 0.2V	-	-	10	mA

Note: Typical characteristics are at V_{DD} = 5V, T_A = 25° C.



CAPACITANCE

($V_{DD} = 5V$, $T_A = 25^\circ C$, $f = 1\text{ MHz}$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	$V_{IN} = 0V$	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0V$	10	pF

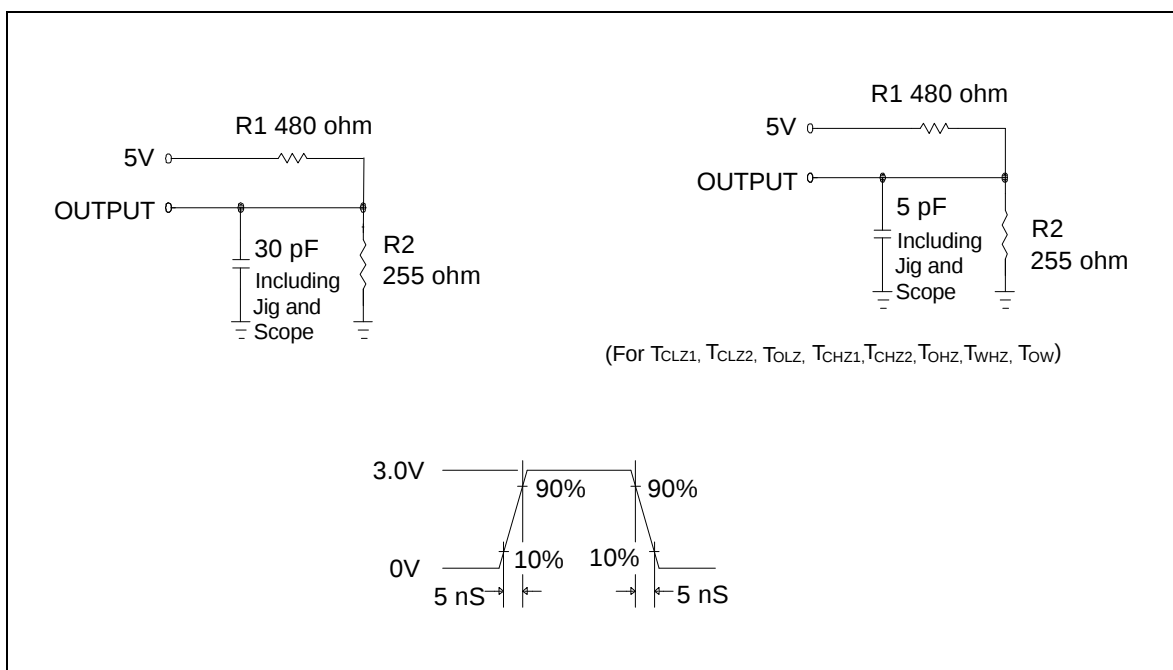
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 30\text{ pF}$, $I_{OH}/I_{OL} = -4\text{ mA}/8\text{ mA}$

AC Test Loads and Waveform





AC Characteristics, continued

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)**Read Cycle**

PARAMETER		SYM.	W24512A-25		UNIT
			MIN.	MAX.	
Read Cycle Time		TRC	25	-	nS
Address Access Time		TAA	-	25	nS
Chip Select Access Time	$\overline{\text{CS1}}$	TACS1	-	25	nS
	CS2	TACS2	-	25	nS
Output Enable to Output Valid		TAOE	-	12	nS
Chip Selection to Output in Low Z	$\overline{\text{CS1}}$	TCLZ1*	3	-	nS
	CS2	TCLZ2*	3	-	nS
Output Enable to Output in Low Z		TOLZ*	0	-	nS
Chip Deselection to Output in High Z	$\overline{\text{CS1}}$	TCHZ1*	-	12	nS
	CS2	TCHZ2*	-	12	nS
Output Disable to Output in High Z		TOHZ*	-	12	nS
Output Hold from Address Change		TOH	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

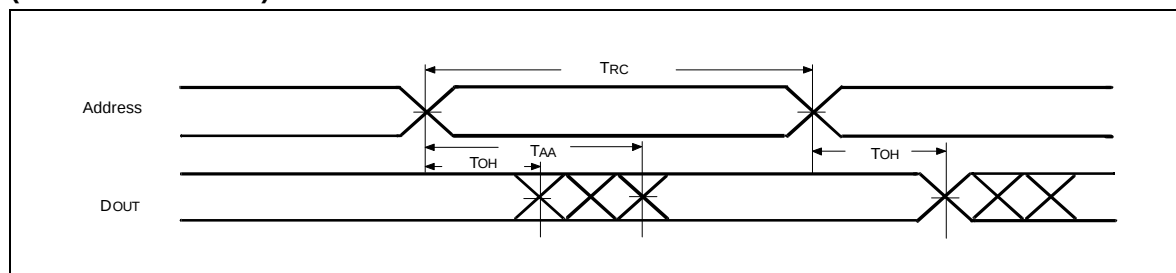
PARAMETER		SYM.	W24512A-25		UNIT
			MIN.	MAX.	
Write Cycle Time		TWC	25	-	nS
Chip Selection to End of Write	$\overline{\text{CS1}}$	TCW1	18	-	nS
	CS2	TCW2	18	-	nS
Address Valid to End of Write		TAW	18	-	nS
Address Setup Time		TAS	0	-	nS
Write Pulse Width		TWP	15	-	nS
Write Recovery Time	$\overline{\text{CS1}}, \overline{\text{WE}}$	TWR1	0	-	nS
	CS2	TWR2	0	-	nS
Data Valid to End of Write		TDW	12	-	nS
Data Hold from End of Write		TDH	0	-	nS
Write to Output in High Z		TWHZ*	-	12	nS
Output Disable to Output in High Z		TOHZ*	-	12	nS
Output Active from End of Write		TOW	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

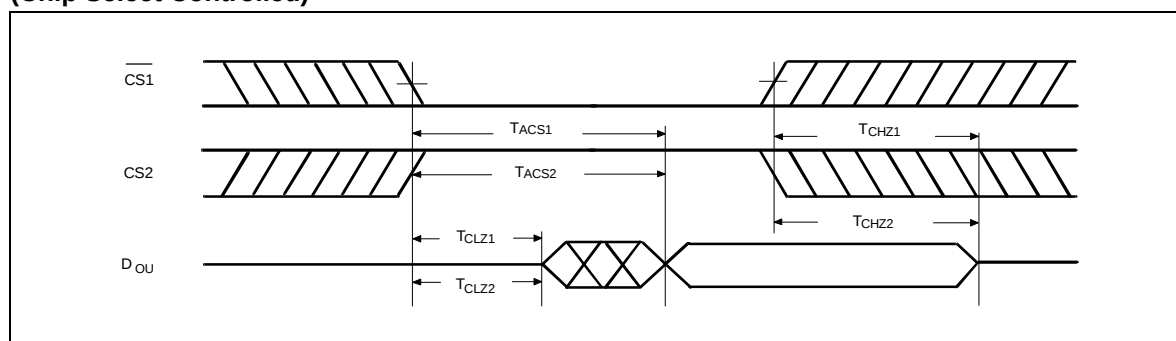
Read Cycle 1

(Address Controlled)



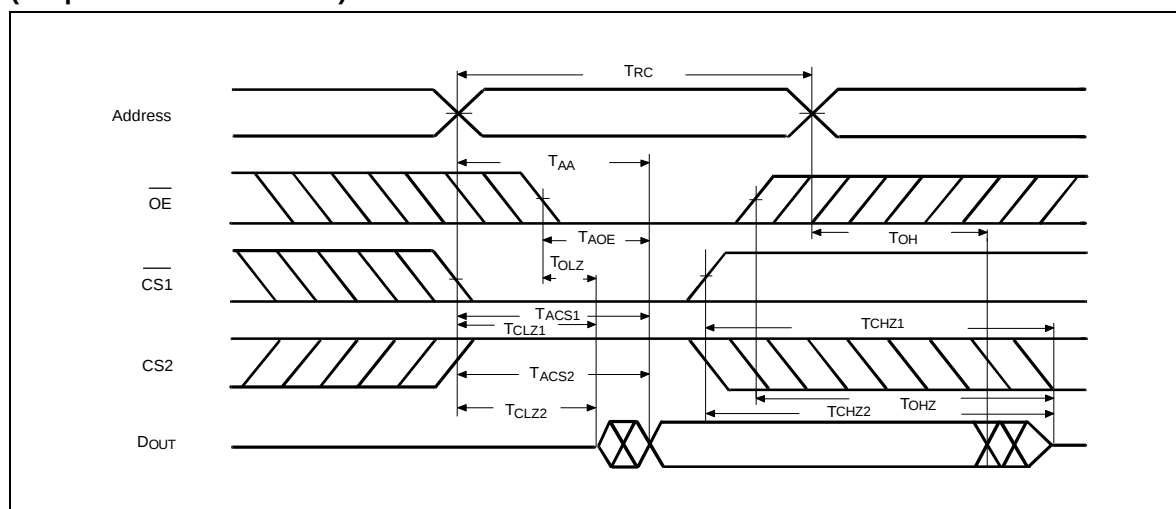
Read Cycle 2

(Chip Select Controlled)



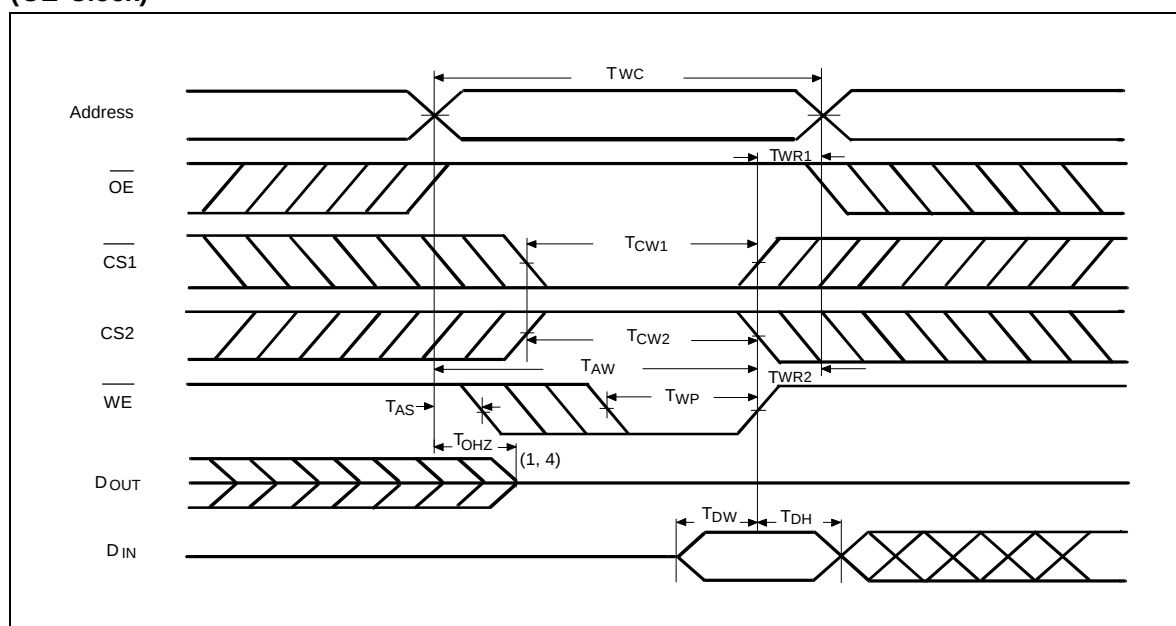
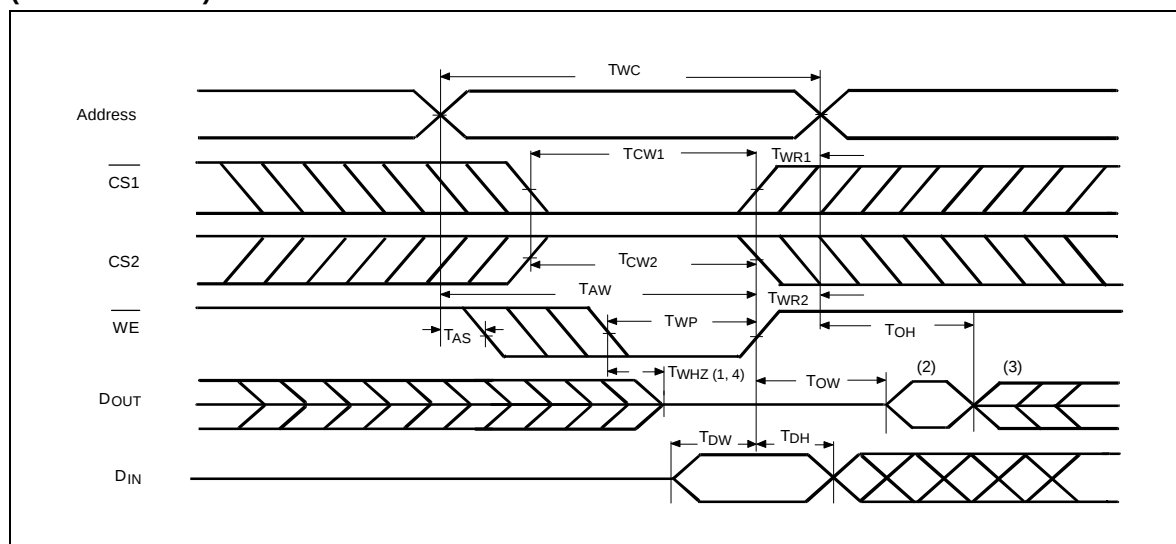
Read Cycle 3

(Output Enable Controlled)





Timing Waveforms, continued

Write Cycle 1**(OE Clock)****Write Cycle 2****(OE = V_{IL} Fixed)**

Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with C_L = 5 pF. This parameter is guaranteed but not 100% tested.

W24512A



ORDERING INFORMATION

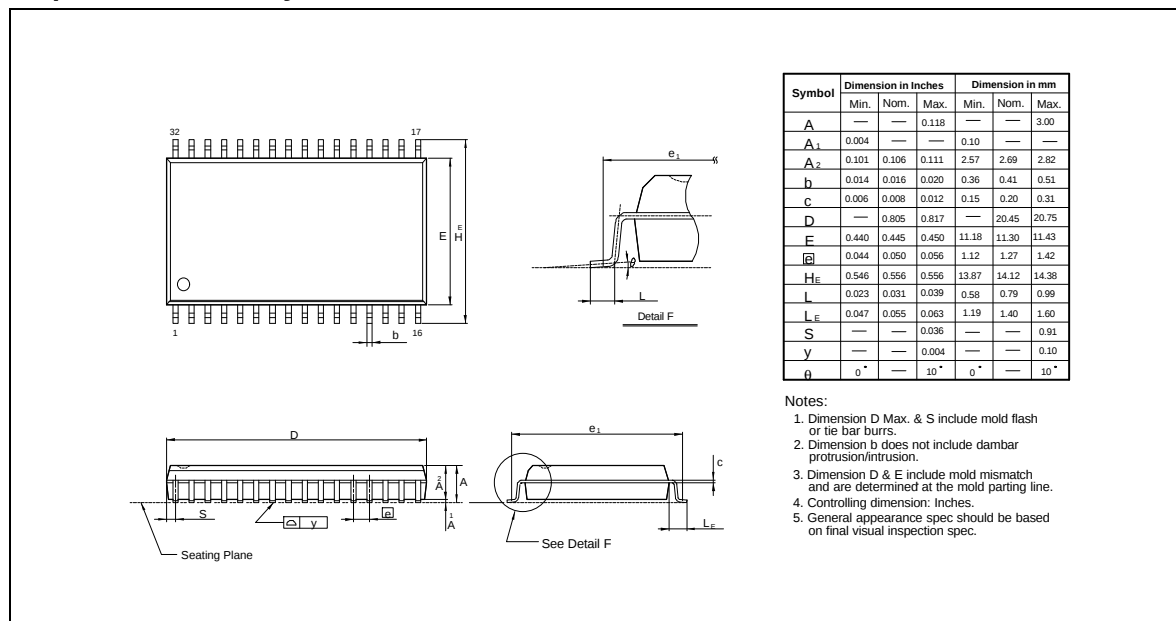
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24512AS-25	25	160	10	450 mil SOP
W24512AT-25	25	160	10	Standard type one TSOP
W24512AJ-25	25	160	10	300 mil SOJ

Notes:

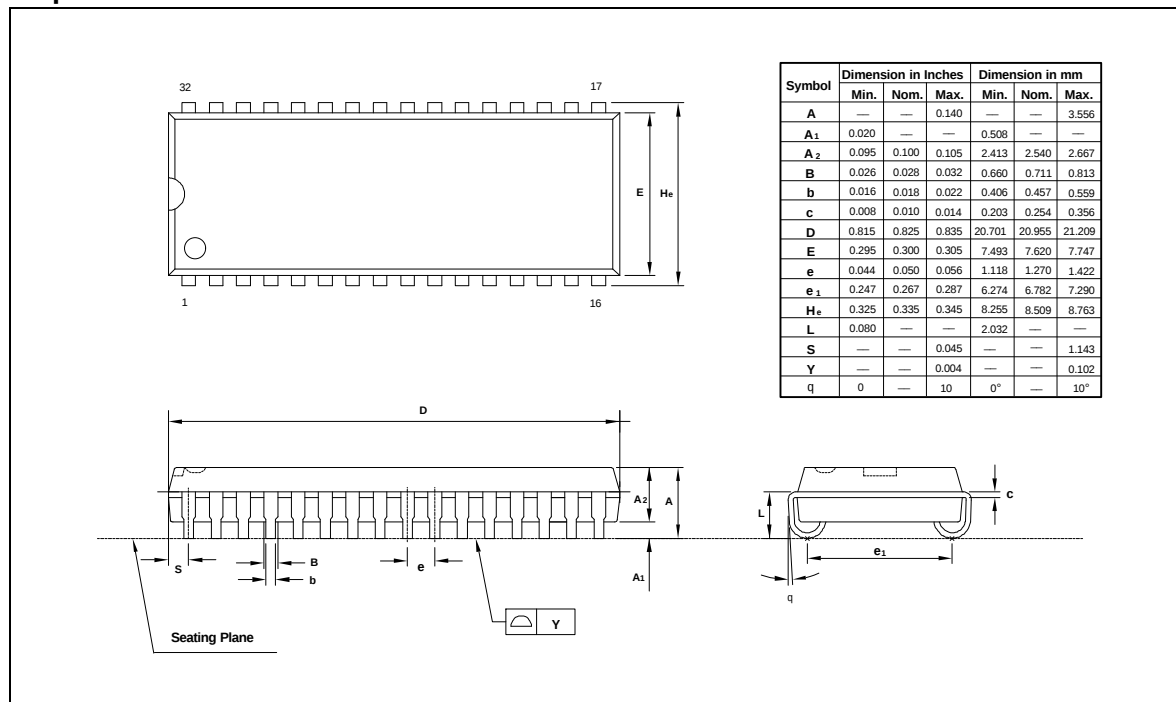
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin SO Wide Body



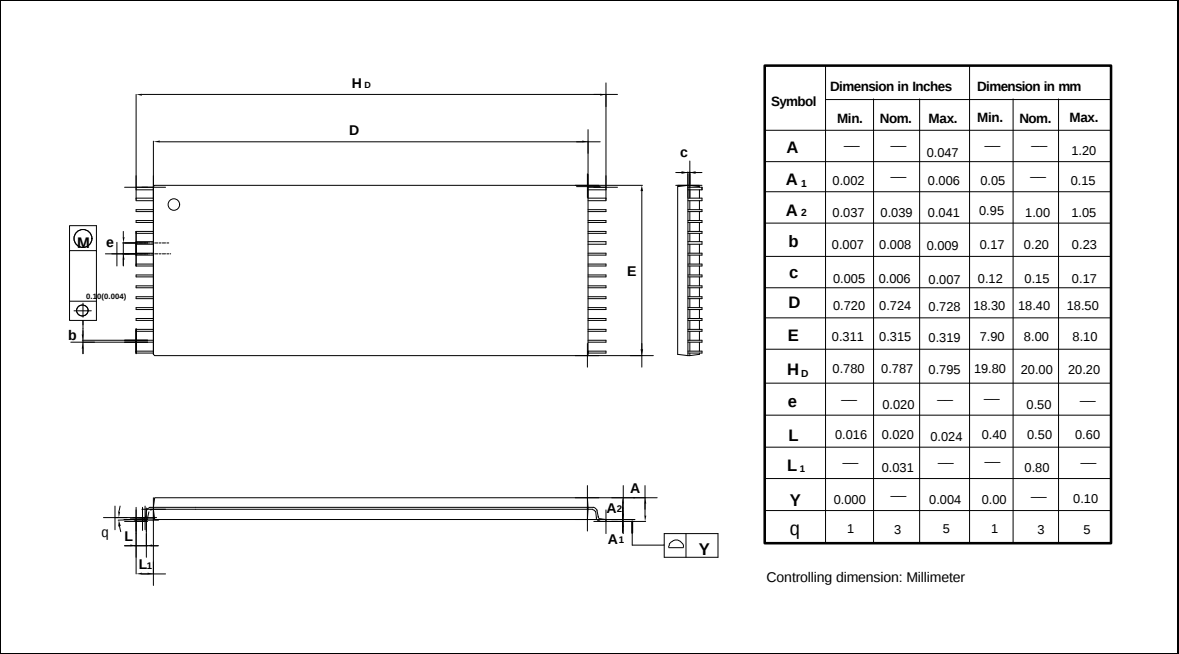
32-pin SOJ





Package Dimensions, continued

32-pin Standard Type One TSOP





VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A4	Apr. 2000	7	Typo Correction in Standby Current Max.: mA -> μ A



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Note: All data and specifications are subject to change without notice.