MOS INTEGRATED CIRCUIT
μPD6121

MULTI-PURPOSE REMOTE CONTROL TRANSMITTER IC
CMOS LSI

DESCRIPTION

The μPD6121 is an infrared remote control transmitter LSI for TV, VCR, stereo components, cassette decks, air conditioners, and other appliances. The 65 536 number customer codes (MAX.) are available by setting external diodes, resistors, and internal MASK ROM.

The transmission code consists of "leader pulse", "16 bit customer code", and "16 bit data code". Using micro-processors for decoder, various applications can be realized.

FEATURES

- Low voltage operation . . . . . V_{DD} = 2.0 to 3.3 V
- Low power consumption . . . . . $I_{DD} < 1$ μA at standby mode
- 32 function keys and 3 double action keys
- 64 + 6 function codes are available. (Using SEL terminal)
- 65 536 customer codes can be selected. (Using external R, Di or internal MASK ROM)
- The transmission format is compatible with μPD1913, μPD1943, μPD6102, μPD6120, μPD6122.
- Pin compatible with the μPD1943.
- NEC standard μPD6121G-001 (μPD1943 compatible), μPD6121G-002 (Built-in customer code ROM)

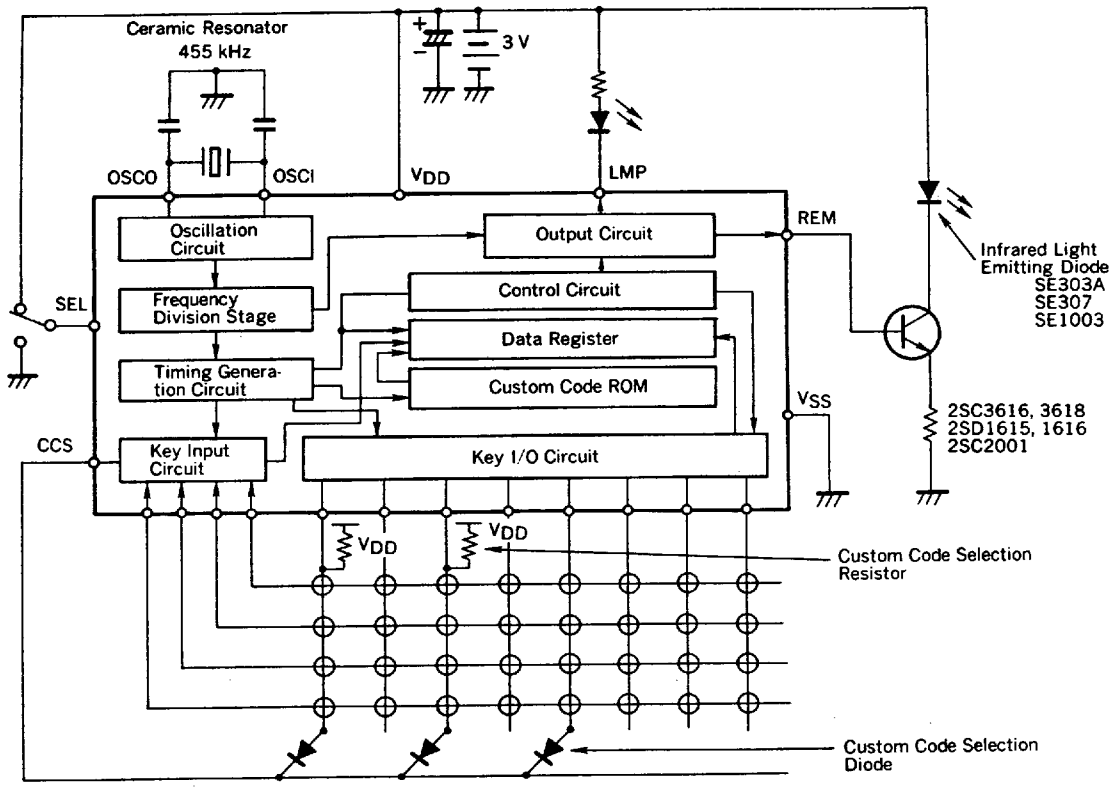
ORDERING INFORMATION

Order Code	Package	Features
μPD6121G-001	20 pin Plastic SOP (375 mil)	μPD1943G compatible
μPD6121G-002	20 pin Plastic SOP (375 mil)	Built-in customer code ROM
μPD6121G-xxx	20 pin Plastic SOP (375 mil)	Custom

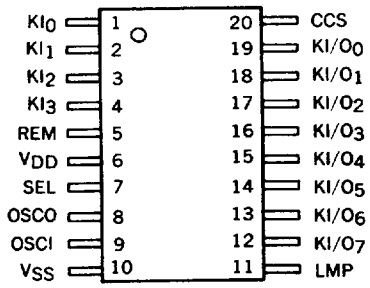
In addition to the above standard products, the μPD6121G can also be ordered as a custom product with custom codes in mask ROM. Incorporating custom codes in mask ROM reduces the number of external parts required.

Document No. IC-1813A
(O. D. No. IC-6857B)

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Terminal		
1	KI_0	Key Input 0
2	KI_1	Key Input 1
3	KI_2	Key Input 2
4	KI_3	Key Input 3
5	REM	Remote Output
6	V_{DD}	3 V
7	SEL	Data Select
8	OSCO	Oscillator Output
9	OSCI	Oscillator Input
10	V_{SS}	
11	LMP	Lamp Output
12	KI/O_7	Key I/O 7
13	KI/O_6	Key I/O 6
14	KI/O_5	Key I/O 5
15	KI/O_4	Key I/O 4
16	KI/O_3	Key I/O 3
17	KI/O_2	Key I/O 2
18	KI/O_1	Key I/O 1
19	KI/O_0	Key I/O 0
20	CCS	Customer Code Select Input

PIN DESCRIPTION

(1) Key input and key output pins KI_0 to KI_3, KI/O_0 to KI/O_7

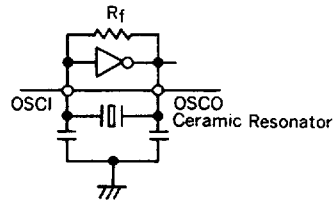
A pull-down resistor is inserted between the key input pins and the V_{SS} pin. If two or more keys are depressed simultaneously, transmission is disabled by the multi-depression prevention circuit. As regards the key transmission priority in the case of two depressions, with simultaneous depressions (±36 ms) transmission is disabled, and first depression, later remainder priority is used.

When a key is depressed, reading of the custom code and key data code is started, and REM output begins 36 ms later, so that if the key is being depressed during this 36 ms interval one transmission is performed. If a key is held down for 108 ms or longer, consecutive transmissions of the leader code only are performed while the key is depressed. As a key interruption operation can handle an interval of up to 126 ms (from ON to ON). It is possible to configure a system with an extremely fast response time.

(2) Oscillation pins OSCI, OSCO

The oscillation circuit starts to operate when a key is depressed.

Use of a ceramic resonator with a 400 to 500 kHz oscillation is designed for non-adjustment operation.



(3) Power supply pin

The power supply voltage is provided by two 3 V batteries, and covers a wide operating supply voltage range of 2.0 to 3.3 V. Also, as oscillation is stopped except during a key operation, the power supply current is 1 μA or less.

(4) REM pin

Outputs the transmission code consisting of the leader code, custom code (16 bits) and data code (16 bits) see "Transmission Code" on page 4).

(5) SEL pin

Data code D_7 can be controlled by this pin, allowing 64 kinds of data to be transmitted.

D_7 is set to "0" by connecting the SEL pin to V_{DD}, and to "1" by connecting the SEL pin to V_{SS}.

As the input of this pin is high-impedance, it must be connected to either V_{DD} or V_{SS}.

(6) CCS pin

The custom code can be set by the diodes connected to the CCS pin and the KI/O pins. Connecting the CCS pin and KI/O pins via diodes gives a corresponding custom code of "1", while no connection gives "0".

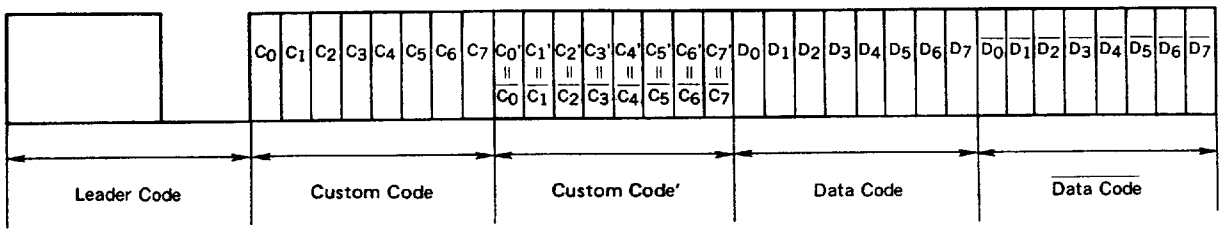
(7) LMP pin

Outputs "L" while the REM pin is outputting a transmission code.

TRANSMISSION CODE

(1) REM output

The transmission code consists of a leader code, 16-bit custom code, and 8-bit data code. The inverse code of the data code is also sent simultaneously, giving a total configuration of 32 bits per transmission.



REM Output Code

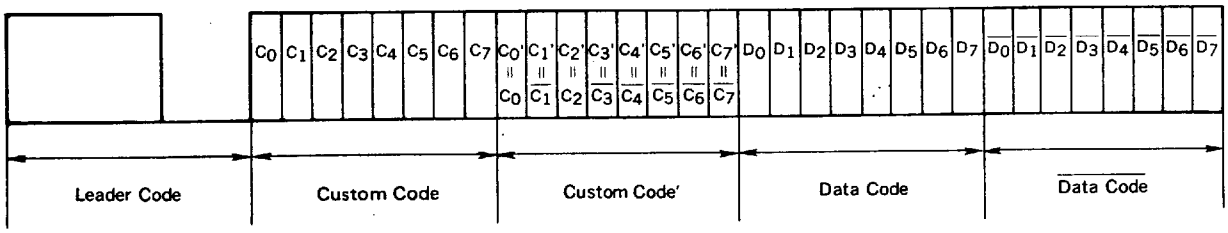
The leader code consists of a 9 ms carrier waveform plus a 4.5 ms OFF waveform, and is used as the leader for the following code. Thus when reception is configured by a microcomputer, the time relationship between reception detection and other processing can be managed efficiently. The code uses the PPM (Pulse Position Modulation) method, with "1" and "0" differentiated by the time between pulses. Each code consists of 8 bits, and simultaneous transmission of the inverse code allows configuration of a system with an extremely low error rate.

(2) Custom code extension

As with the μPD1943G, the above output codes can be obtained by custom code selection using diodes only.

To further extend the number of custom codes, 200 kΩ pull-up resistors are added to pins KI/O_0 through KI/O_7, and the bit corresponding to a pin from among the custom code' outputs is output without being inverted.

By encoding the custom code' part, 256 times the number of μPD1943G custom codes, i.e. 65 536, can be selected.



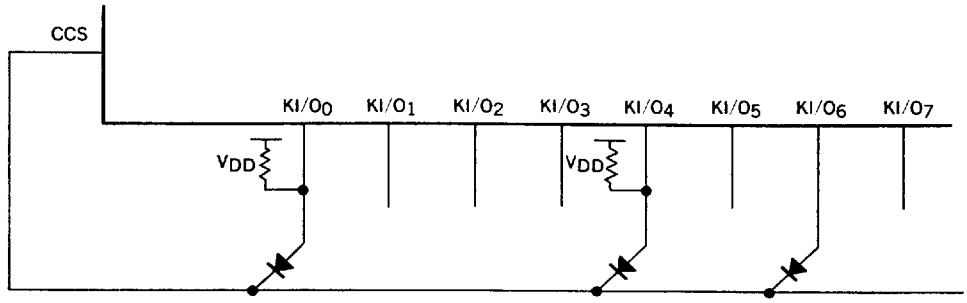
*: Pull-up resistor added to pins KI/O_0 and KI/O_2.
C_0 and C_2 output without inversion (non-inverted bits).

(3) Custom code

The REM output custom code can be set in any of 65 536 ways by means of the diodes attached to the CCS (Custom Code Select) pin and the KI/O pins and the pull-up resistors attached to the KI/O pins. When a code other than code 00000000 (no diode connection) is used, please contact NEC since custom codes are managed by NEC to prevent errors between various systems.

Setting Example

(Configuration example)



The custom code high-order 8 bits are determined by the diode attached to the CCS pin and KI/O pins.

Set custom code

Custom code high-order 8 bits

1	0	0	0	1	0	1	0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7

"1" specified by diode

The custom code' low-order 8 bits are determined by the pull-up resistor attached to the KI/O pins.

Set custom code

Custom code' low-order 8 bits

1	0	0	0	1	0	0	0
C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'

"1" specified by pull-up resistor

That is, custom code non-inverted bit specification

(1 . . . Non-inversion for C_0 to C_7
0 . . . Inversion for C_0 to C_7)

When the above setting is made, the output custom code is as follows:

Custom code

Custom code high-order 8 bits								Custom code' low-order 8 bits							
1	0	0	0	1	0	1	0	1	1	1	1	1	1	0	1
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'
								C_0	$\overline{C_1}$	$\overline{C_2}$	$\overline{C_3}$	C_4	$\overline{C_5}$	$\overline{C_6}$	$\overline{C_7}$

(4) Custom code mask ROM specification

The custom code can also be set by mask ROM. When the mask ROM specification is used the custom code can be set without the connection of external diodes and resistors, and by combining external diodes and resistors with mask ROM it is possible to output a code with different contents from those set by the mask ROM. When mask ROM specification is used, (Ver. I) or (Ver. II) can be selected.

	Custom Code High-Order 8 Bits	Custom Code' Low-Order 8 Bits
Ver. I	Determined by logical OR of internal ROM1 and external diode positions.	Determined by logical OR of internal ROM2 and external pull-up resistor positions
Ver. II	C_0, C_1, C_2: Determined by wiring one of pins KI/O_0 thru KI/O_7 to CCS pin. C_3 thru C_7: Determined by internal ROM3 and absence/presence of KI/O_6 & KI/O_7 external pull-up resistors.	Determined by logical OR of internal ROM2 and external pull-up resistor (KI/O_0 thru KI/O_5) positions.

* Standard product μPD6121G-001 uses the Ver. I specification, and is pin-compatible with the μPD1943G. When using this as pin-compatible with the μPD1943G, the following points should be noted:

(1) The SEL pin (pin 7) should be connected to V_{DD}.

(2) The capacity of the capacitor connected to the oscillation pins (OSCO pin 8, and OSCI pin 9) should be changed. (See page 18.)

Internal ROM is set as follows:

ROM1								ROM2							
Custom code high-order 8 bits								Custom code' low-order 8 bits							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'

* Standard product μPD6121G-002 uses the Ver. II specification.

Internal ROM is set as follows:

ROM3

C_7, C_6, C_5, C_4, C_3 of Custom Code High-Order 8 Bits

Pull-Up Resistor

ROM3	C_7	C_6	C_5	C_4	C_3	KI/O_6	KI/O_7
ROM3 to ROM0	0	0	0	0	0	No	No
ROM3 to ROM1	1	0	0	1	1	No	Yes
ROM3 & ROM2	1	0	0	0	0	Yes	No
ROM3 & ROM3	1	1	1	0	1	Yes	Yes

ROM2

Custom code' low-order 8 bits

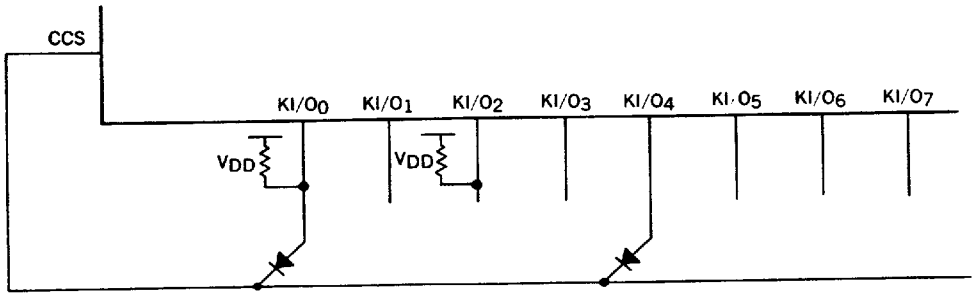
0	0	0	0	0	0	0	0
C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'

(Ver. I)

Internal custom code ROM1 and ROM2 (total 16 bits) are effective, with 8 bits being the part (ROM1) corresponding to the external diodes, and 8 bits the part (ROM2) corresponding to the external pull-up resistors.

Setting Example

Configuration example



The custom code high-order 8 bits are determined by the logical OR of the external diode positions and internal ROM1.

External setting (see above figure)

Custom code high-order 8 bits

1	0	0	0	1	0	0	0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7

Diode positions

(KI/O_0, KI/O_4)

Internal ROM1 (setting example)

ROM1

0	1	0	1	0	0	0	0

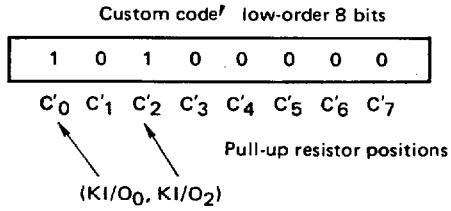
External setting V Internal ROM1

1	1	0	1	1	0	0	0

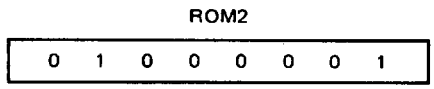
Custom code

The custom code' low-order 8 bits are determined by the logical OR of the external pull-up resistor positions and internal ROM2.

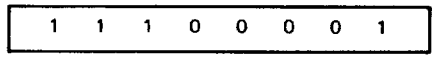
External setting (see above figure)



Internal ROM2 (setting example)



External setting V Internal ROM2



Custom code non-inverted bit specification
(1 . . . Non-inversion for C_0 to C_7
0 . . . Inversion for C_0 to C_7)

When pull-up resistors, diodes and ROM1/ROM2 and set, as mentioned before, the output custom code is as follows:

Custom code

Custom code high-order 8 bits								Custom code' low-order 8 bits							
1	1	0	1	1	0	0	0	1	1	0	0	0	1	1	0
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'
								C_0	C_1	C_2	$\overline{C_3}$	$\overline{C_4}$	$\overline{C_5}$	C_6	$\overline{C_7}$

*: The code to be transmitted is output LSB-first.

(Ver. II)

With Ver. II, the CCS pin does not have the function of reading the external diodes.

Internal custom code ROM2 and ROM3 (total 28 bits) are effective, with 20 bits being the part (ROM3) for setting the 4 channels of custom code C_7, C_6, C_5, C_4 and C_3 as 5 bits each, and 8 bits being the part (ROM2) corresponding to the external pull-up resistors (excluding KI/O_6 and KI/O_7).

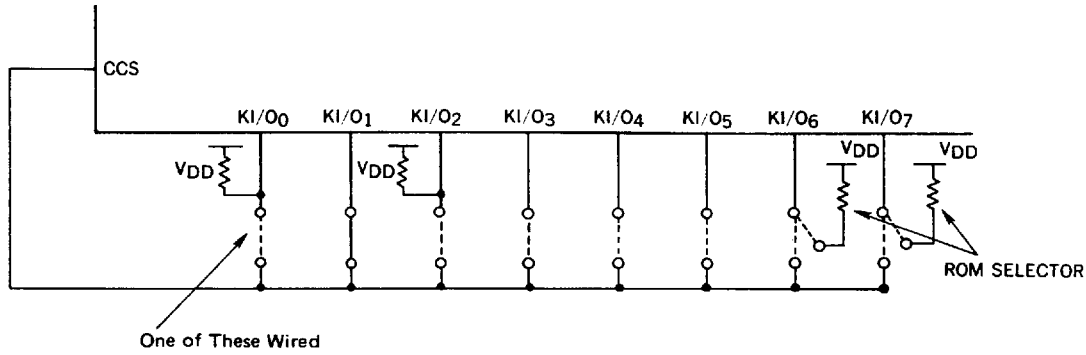
With Ver. II, 0/1 allocation to C_2, C_1 and C_0 of the custom code high-order bits is set as shown in the following table according to the pin connection status of KI/O_0 through KI/O_7.

CCS-	C_2	C_1	C_0
KI/O_0	0	0	0
KI/O_1	0	0	1
KI/O_2	0	1	0
KI/O_3	0	1	1
KI/O_4	1	0	0
KI/O_5	1	0	1
KI/O_6	1	1	0
KI/O_7	1	1	1

When CCS pin is open
$(C_2\ C_1\ C_0) = (0, 0, 0)$

Setting Example

Configuration example



Bits C_2, C_1, C_0 of the custom code high-order 8 bits are determined by wiring between the CCS pin and pins KI/O_0 thru KI/O_7, and thus in the above figure is:

1	0	0
C_0	C_1	C_2

Bits C_7, C_6, C_5, C_4, C_3 of the custom code high-order 8 bits are determined by selection by the pull-up resistors added to KI/O_6 & KI/O_7 among the 4 channels of internal ROM3.

Pull-Up Resistors

KI/O_6	KI/O_7	ROM3	C_7	C_6	C_5	C_4	C_3	
No	No	ROM3 to ROM0	1	0	1	1	0	(Setting example)
No	Yes	ROM3 to ROM1	0	0	1	1	1	
Yes	No	ROM3 & ROM2	1	1	0	1	1	
Yes	Yes	ROM3 & ROM3	1	1	1	1	1	

In the above figure, C_3 thru C_7 of the custom code high-order 8 bits are:

1	1	0	1	1
C_3	C_4	C_5	C_6	C_7

The custom code' low-order 8 bits are determined by the logical OR of the KI/O_0 thru KI/O_5 external pull-up resistor positions and internal ROM2.

External setting

Custom code' low-order 8 bits
(see configuration example)

1	0	1	0	0	0
C_0'	C_1'	C_2'	C_3'	C_4'	C_5'

Pull-up resistor positions

(KI/O_0, KI/O_2)

Internal ROM2 (setting example)

ROM2

0	1	0	0	0	0	1	0
C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'

External setting V Internal ROM2

1	1	1	0	0	0	1	0

Custom code non-inverted bit specification

(1 . . . Non-inversion for C_0 to C_7
0 . . . Inversion for C_0 to C_7)

When pull-up resistors, wiring and ROM2, ROM3 are set, as mentioned before, the output custom code is as follows:

Custom code

Custom code high-order 8 bits								Custom code* low-order 8 bits							
1	0	0	1	1	0	1	1	1	0	0	0	0	1	1	1
C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_0'	C_1'	C_2'	C_3'	C_4'	C_5'	C_6'	C_7'
								C_0	C_1	C_2	$\overline{C_3}$	$\overline{C_4}$	$\overline{C_5}$	C_6	$\overline{C_7}$

*: The code to be transmitted is output LSB-first.

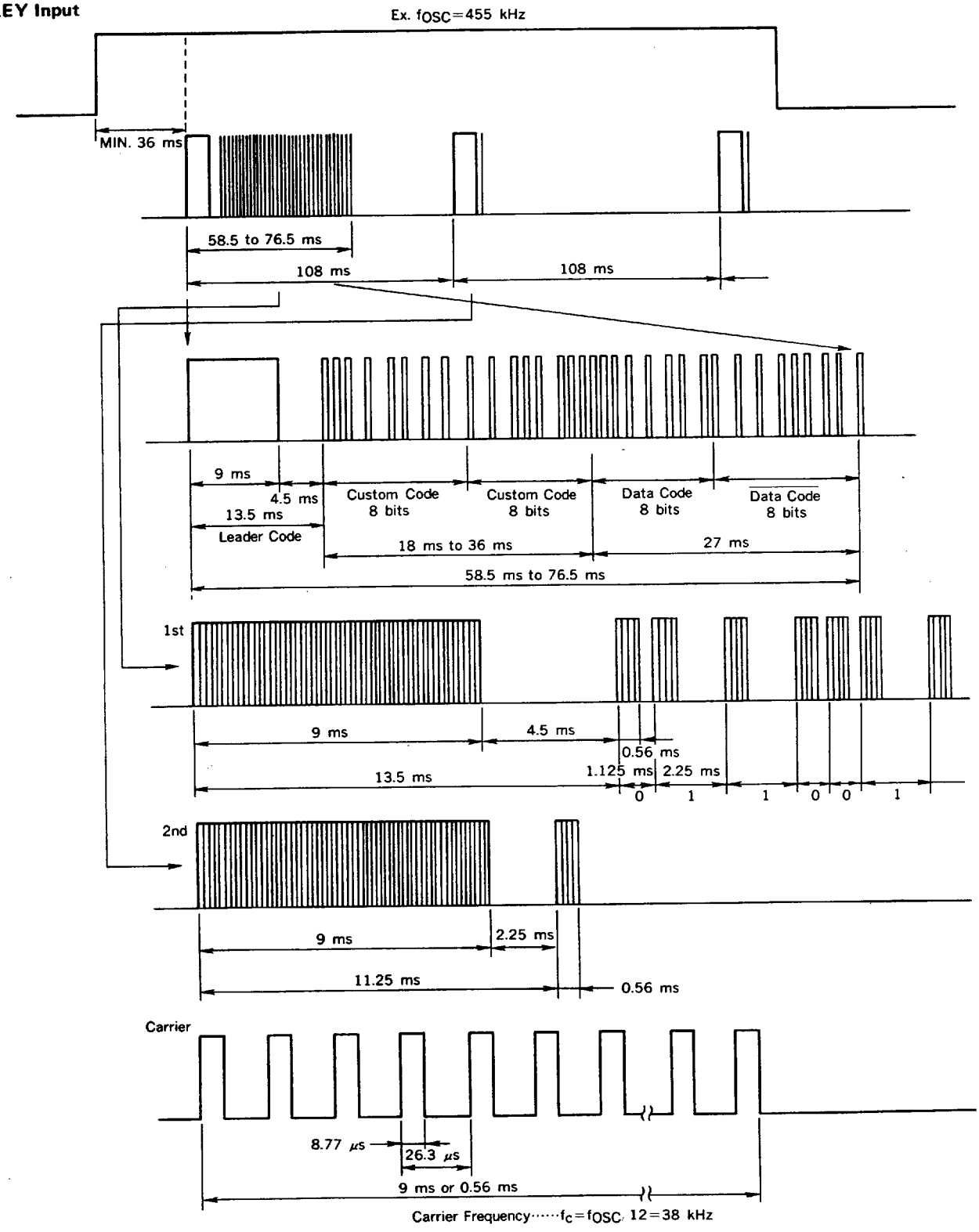
Key Data Code

KEY	CONNECTION					DATA CODE								NOTES
	KI_0	KI_1	KI_2	KI_3	KI/O	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	
K 1	*				KI/O_0	0	0	0	0	0	0	0	0/1	
K 2		*				1	0	0	0	0	0	0	0/1	
K 3			*			0	1	0	0	0	0	0	0/1	
K 4				*		1	1	0	0	0	0	0	0/1	
K 5	*				KI/O_1	0	0	1	0	0	0	0	0/1	N/A for μPD1913C μPD6120C
K 6		*				1	0	1	0	0	0	0	0/1	
K 7			*			0	1	1	0	0	0	0	0/1	
K 8				*		1	1	1	0	0	0	0	0/1	
K 9	*				KI/O_2	0	0	0	1	0	0	0	0/1	
K10		*				1	0	0	1	0	0	0	0/1	
K11			*			0	1	0	1	0	0	0	0/1	
K12				*		1	1	0	1	0	0	0	0/1	
K13	*				KI/O_3	0	0	1	1	0	0	0	0/1	N/A for μPD1913C μPD6120C
K14		*				1	0	1	1	0	0	0	0/1	
K15			*			0	1	1	1	0	0	0	0/1	
K16				*		1	1	1	1	0	0	0	0/1	
K17	*				KI/O_4	0	0	0	0	1	0	0	0/1	
K18		*				1	0	0	0	1	0	0	0/1	
K19			*			0	1	0	0	1	0	0	0/1	
K20				*		1	1	0	0	1	0	0	0/1	
K21	*				KI/O_5	0	0	1	0	1	0	0	0/1	
K22		*				1	0	1	0	1	0	0	0/1	
K23			*			0	1	1	0	1	0	0	0/1	
K24				*		1	1	1	0	1	0	0	0/1	
K25	*				KI/O_6	0	0	0	1	1	0	0	0/1	
K26		*				1	0	0	1	1	0	0	0/1	
K27			*			0	1	0	1	1	0	0	0/1	
K28				*		1	1	0	1	1	0	0	0/1	
K29	*				KI/O_7	0	0	1	1	1	0	0	0/1	N/A for μPD1913C μPD6120C
K30		*				1	0	1	1	1	0	0	0/1	
K31			*			0	1	1	1	1	0	0	0/1	
K32				*		1	1	1	1	1	0	0	0/1	

N/A = Not Available

Remote Output Waveforms

KEY Input



9. Double Key Operation

When more than two keys except K21 + K22, K21 + K23 and K21 + K24 are depressed at the same time, the transmission output stops.

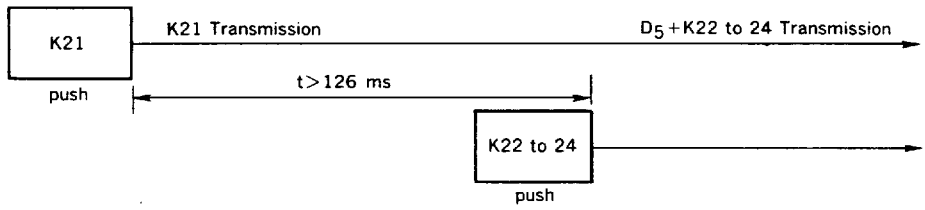
Double key operation is useful for tape deck recording operation.

Double key operation form are following.

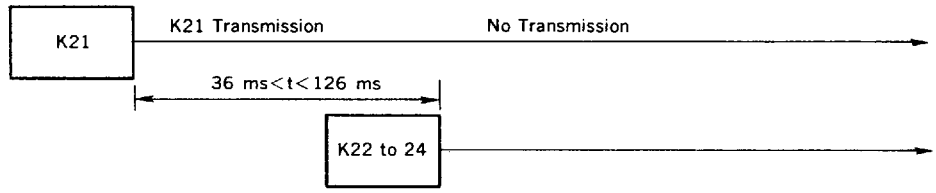
Double Key Operation

KEY	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
K21 + K22	1	0	1	0	1	1	0	0/1
K21 + K23	0	1	1	0	1	1	0	0/1
K21 + K24	1	1	1	0	1	1	0	0/1

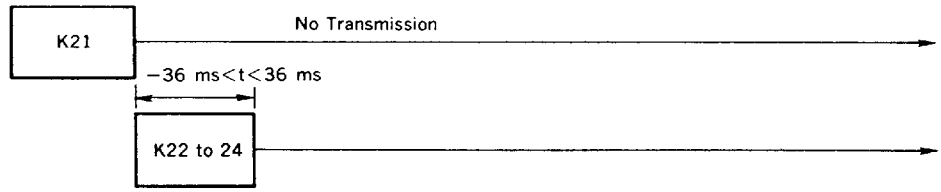
(a) Operation



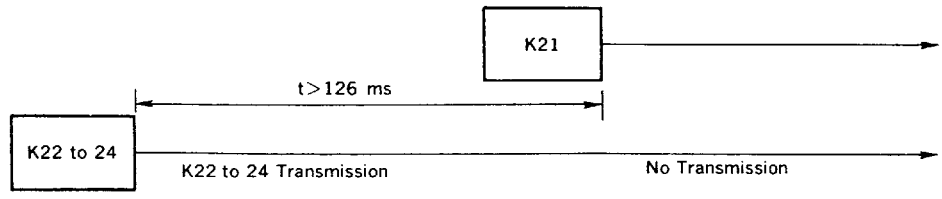
(b) No operaiton



(c) No operation



(d) No operation



10. Customer Code ROM Format

This LSI has customer code table ROM on the chip. So users can generate customer codes without external parts. The customer code ROM format is following.

		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
Ver. 1 or 2 SEL		0	0	0	0	0	0	1/0	1/0		
ROM1		1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	ROM PULL	SEL UP
ROM2		1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	KI/O_6	KI/O_7
ROM3	0	1/0	1/0	1/0	1/0	1/0	0	0	0	NO	NO
	1	1/0	1/0	1/0	1/0	1/0	0	0	0	NO	YES
	2	1/0	1/0	1/0	1/0	1/0	0	0	0	YES	NO
	3	1/0	1/0	1/0	1/0	1/0	0	0	0	YES	YES

1) Ver. 1 or Ver. 2 selection . . . . . Ver. 1 = 01_H, Ver. 2 = 02_H
2) When a user selects Ver. 1, ROM1 is available for the customer code (C_7 to C_0) selection.
3) ROM2 is available for the customer code' (C_7' to C_0') selection.
4) When a user selects Ver. 2, ROM3 is available for the customer code (C_7 to C_3) selection. And a user can select ROM3 –0, ROM3–1, ROM3–2 or ROM3–3 by the KI/O_6 and KI/O_7 pull up resistances.

Mask ROM Ordering Procedure

The ordering medium for custom code mask ROM is PROM.

- Ordering medium — PROM
  (μPD2716, μPD2732A, μPD2764, μPD27128, μPD27256 and equivalent products)
- Quantity — 3
- Data storage method
  ① Ver. I or Ver. II selection is stored in PROM address 0.
  ② ROM1 data is stored in PROM address 1.
  ③ ROM2 data is stored in PROM address 2.
  ④ ROM3 data is stored in PROM address 3 to 6.

		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Ver. I or Ver. II SEL		0	0	0	0	0	0		
ROM1									
ROM2									
ROM3	0						0	0	0
	1						0	0	0
	2						0	0	0
	3						0	0	0

HEX Code

C_7 to C_4	C_3 to C_0
0	

PROM

Write Data		PROM Address
0		0
		1
		2
		3
		4
		5
		6

NOTE 1: When Ver. I is selected, ROM1 and ROM2 data is stored in PROM address 1 and address 2, and 00H is stored as ROM3 data (addresses 3 to 6).

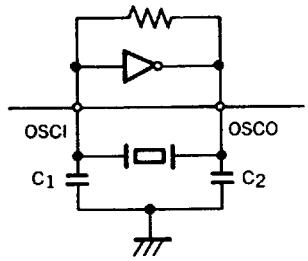
2: When Ver. II is selected, ROM2 and ROM3 to 6, and 00H is stored as ROM1 data (address 1).

The μPD6121G oscillation circuit is designed for use of a 400 kHz or 500 kHz ceramic resonator, but there may be mutual influence between variations in the IC and the ceramic resonator resulting in abnormal oscillation.

The following table shows the recommended values of C_1 and C_2 when using the μPD6121G. These recommended values have been obtained through the cooperation of the ceramic resonator manufacturers.

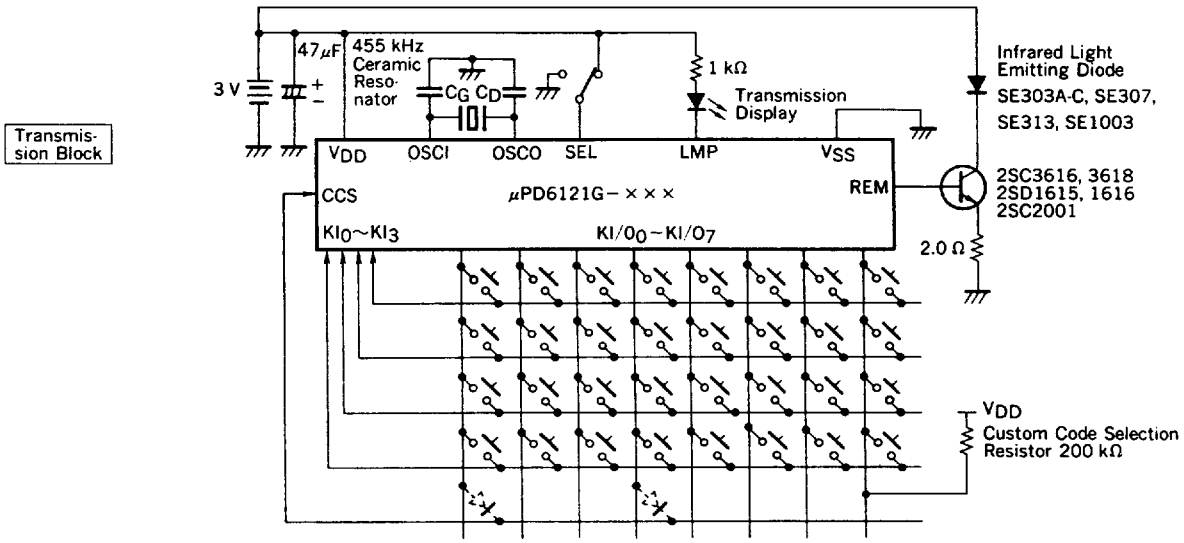
Recommended Ceramic Resonators

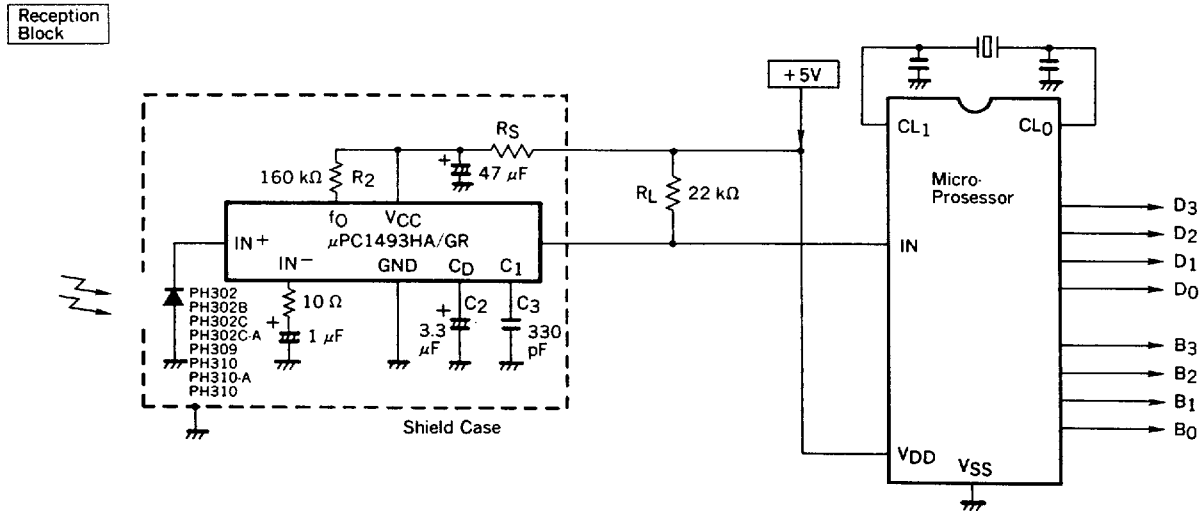
Manufacturer	Product	External Capacitance (pF)		Oscillation Voltage Range (V)	
		C_1	C_2	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSB455E	220	220	2.0	3.3
	CSB480E	220	220	2.0	3.3
Toko, Inc.	P46CRK455-M11	120	300	2.0	3.3
Kyocera Corp.	KBR-455BTLR	220	220	2.0	3.3



Sample Application Circuit

In this example a 4-bit single-chip microcomputer is used for reception. The microcomputer is not used exclusively for reception; this can be included among other functions.





The application circuits and circuit constants shown in this document are not designed for volume production with parts variance and temperature characteristics taken into consideration. NEC Corporation cannot accept liability for patent infringements in connection with these circuits.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	−0.3 to V_{DD}	V
Power Dissipation	P_d	250	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

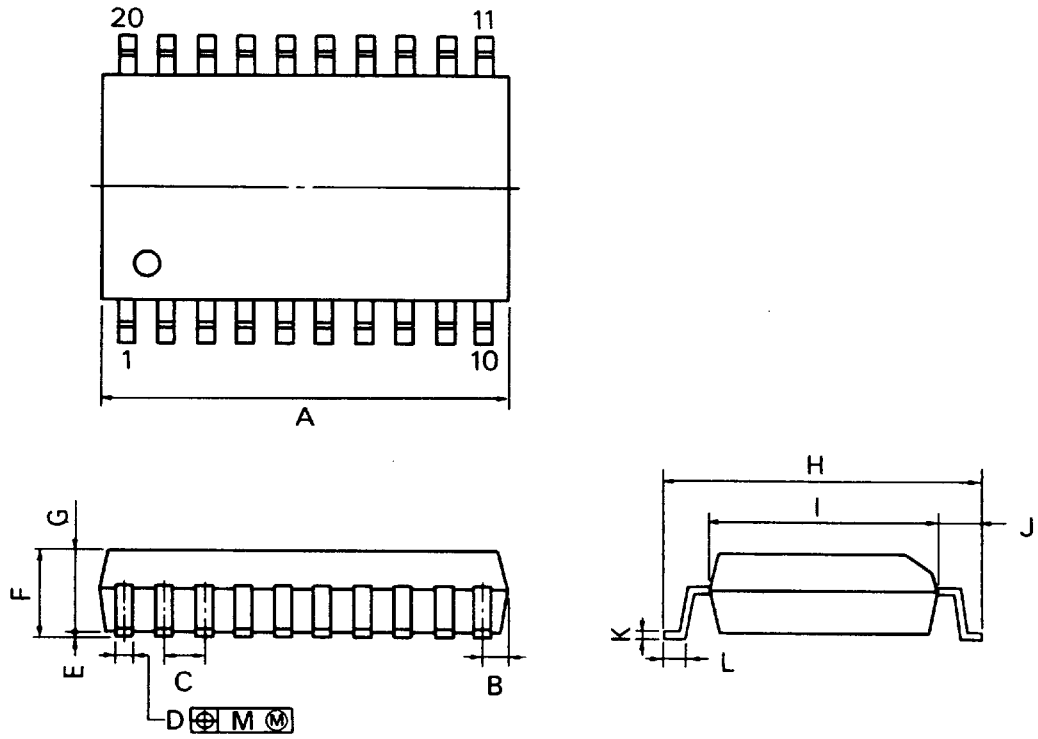
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	2.0	3.0	3.3	V
Oscillation Frequency	f_{osc}	400	455	500	kHz
Input Voltage	V_{IN}	0		V_{DD}	V
Custom code select Pull up Resistance	R_{up}	160	200	240	kΩ

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD} = 3.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD}	2.0	3.0	3.3	V	
Current Consumption 1	I_{DD1}		0.1	1.0	mA	f_{osc} = 455 kHz
Current Consumption 2	I_{DD2}			1.0	μA	f_{osc} = STOP
REM High Level Output Current	I_{OH1}	−5.0	−8.0		mA	V_O = 1.5 V
REM Low Level Output Current	I_{OL1}	15	30		μA	V_O = 0.3 V
LMP High Level Output Current	I_{OH2}	−15	−30		μA	V_O = 2.7 V
LMP Low Level Output Current	I_{OL2}	1	1.5		mA	V_O = 0.3 V
KI High Level Input Current	I_{IH1}	10		30	μA	V_{IN} = 3.0 V
KI Low Level Input Current	I_{IL1}			−0.2	μA	V_{IN} = 0 V
KI High Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	
KI Low Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	
KI/O High Level Input Voltage	V_{IH2}	1.3		V_{DD}	V	
KI/O Low Level Input Voltage	V_{IL2}	0		0.4	V	
KI/O High Level Input Current	I_{IH2}	2		7	μA	V_{IN} = 3.0 V
KI/O Low Level Input Current	I_{IL2}			−0.2	μA	V_{IN} = 0 V
KI/O High Level Output Current	I_{OH3}	1.0		2.5	mA	V_O = 2.5 V
KI/O Low Level Output Current	I_{OL3}	35		100	μA	V_O = 1.7 V
CCS High Level Input Voltage	V_{IH3}	1.1			V	
CCS High Level Input Current	I_{IH3}			0.2	μA	Pull up V_{IN} = 3.0 V
CCS Low Level Input Current	I_{IL3}	−3		−8	μA	Pull up V_{IN} = 0 V
CCS High Level Input Current	I_{IH4}	10		30	μA	Pull down V_{IN} = 3.0 V
CCS Low Level Input Current	I_{IL4}			−0.2	μA	Pull down V_{IN} = 0 V

20PIN PLASTIC SOP (375 mil)



P20GM-50-375B-1

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	$0.1^{+0.2}_{-0.1}$	$0.004^{+0.008}_{-0.004}$
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	$10.3^{\pm0.3}$	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	$0.8^{\pm0.2}$	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.
Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD6121G

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature : 230 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow process : 1, Exposure limit* : None	IR30-00
VPS	Peak package's surface temperature : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow process : 1, Exposure limit* : None	VP15-00
Wave soldering	Solder temperature : 260 °C or below. Flow time : 10 seconds or below. Number of flow process : 1, Exposure limit* : None	WS60-00
Pertial heating method	Terminal temperature : 300 °C or below, Flow time : 10 seconds or below. Exposure limit* : None	

* : Exposure limit before soldering after dry-pack package is opened.
Storage conditions : 25 °C and relative humidity at 65 % less.

Note: Do not apply more than a single process at once, except for "Partial heating method".