NEC®

T-43-25

TRANSISTOR ARRAY

UPA101B
UPA101G

FEATURES

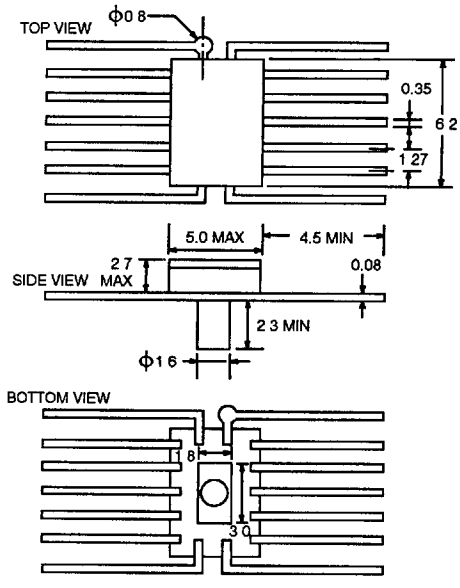
- **BUILT-IN ULTRAHIGH FREQUENCY MULTIPLIER:** (9 GHz Single Transistors)
- **OUTSTANDING h_{FE} LINEARITY**
- **TWO PACKAGE OPTIONS:**
  UPA101B: Superior thermal dissipation due to studded 14-pin ceramic package
  UPA101G: Reduced circuit size due to 8-pin mini-flat package for surface mounting

DESCRIPTION AND APPLICATIONS

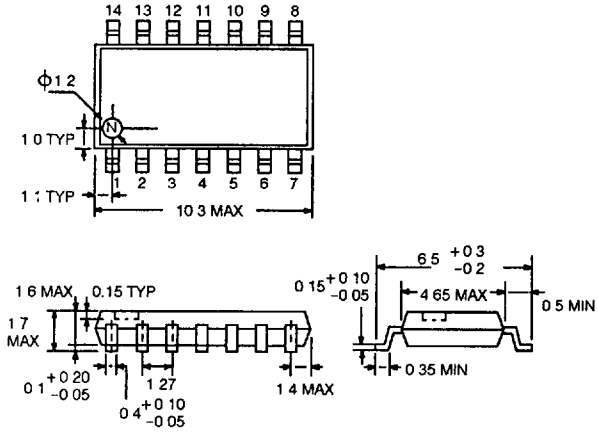
This Si MMIC transistor array contains six (6), 9 GHz bipolar transistors. Applications include a multiplier, double balanced mixer, phase detector, or AGC circuit. The two package options offer a choice of excellent heat dissipation or 35% size reduction.

OUTLINE DIMENSIONS (Units in mm)

OUTLINE BS14



OUTLINE G14



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CBO}*	Collector to Base Voltage	V	15
V_{CEO}*	Collector to Emitter Voltage	V	6
V_{EBO}*	Emitter to Base Voltage	V	2.5
I_C*	Collector Current	mA	40
P_T	Power Dissipation UPA101B UPA101G	 mW mW	 650 250
T_J	Junction Temperature UPA101B UPA101G	 °C °C	 200 125
T_{STG}	Storage Temperature UPA101B UPA101G	 °C °C	 −55 to +200 −55 to +125

*Absolute maximum ratings for each transistor.

See connection diagram for description of leads.

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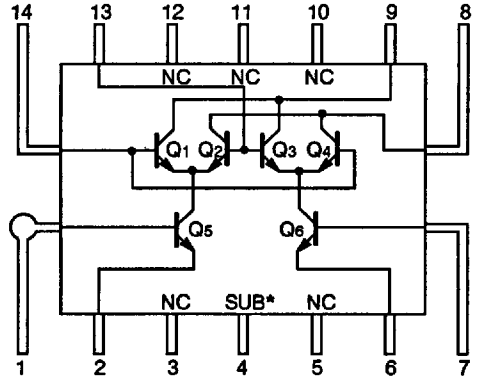
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE			UPA101B, UPA101G BS14, G14		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{CBO}	Collector Cut-off Current at V_{CB} = 5 V, I_E = 0 (Q1 thru Q6)	µA			1.0
I_{EBO}	Emitter Cut-off Current at V_{EB} = 1 V, I_C = 0 (Q5 and Q6)	µA			1.0
h_{FE}	Direct Current Amplification, V_{CE} = 3 V, I_C = 1 mA (Q5 and Q6)		40	100	250
h_{FE1}/h_{FE2}	Direct Current Amplification Ratio, V_{CE} = 3 V, I_C = 1 mA, (Q5 and Q6)		0.9	1.0	1.1
C_{EB}	Emitter to Base Capacitance at V_{EB} = 0, f = 1 MHz	pF		1.4	2.8
f_T	Gain Bandwidth Product* at V_{CE} = 3 V, I_C = 10 mA	GHz		9	

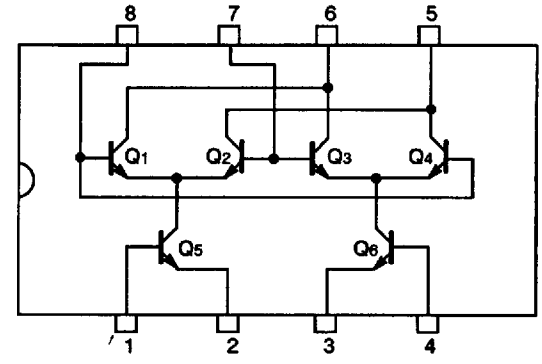
*Measured by installing a single transistor in a Micro-X package: the value shown is a reference value.

CONNECTION DIAGRAM (Top View)

UPA101B

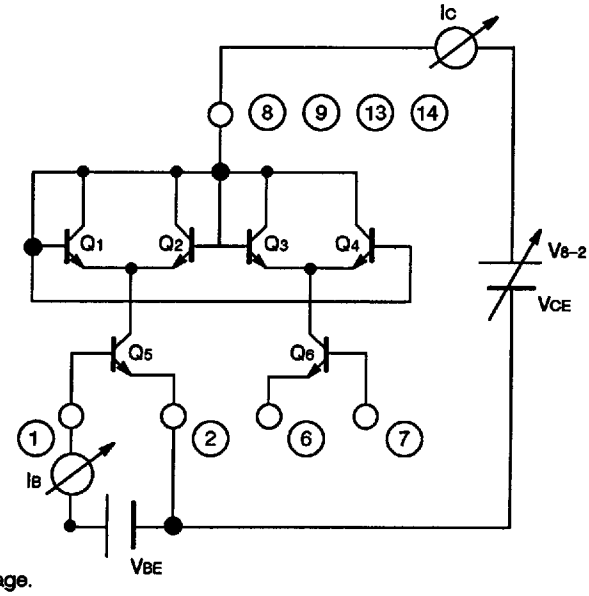


UPA101G



*Note: Substrate should be connected to the lowest voltage point to prevent latch-up.

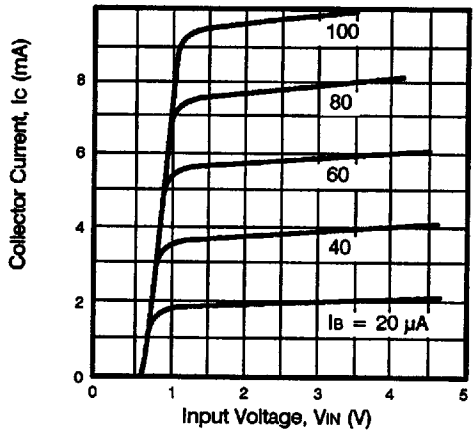
TEST CIRCUIT SCHEMATIC* (For Electrical Characteristics Measurements excluding f_T)



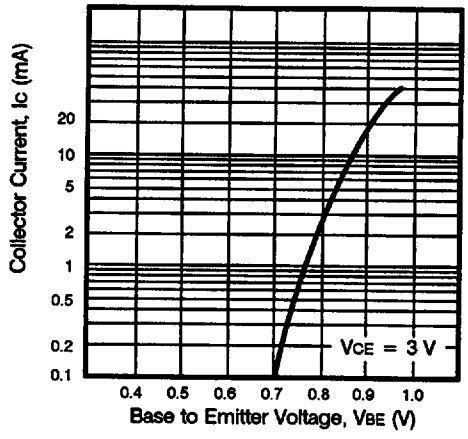
*See performance characteristics for voltage.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C)

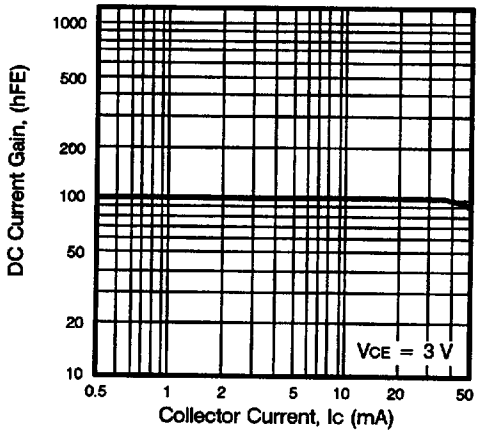
COLLECTOR CURRENT vs.
PIN 8 TO PIN 2 OR 6 VOLTAGE



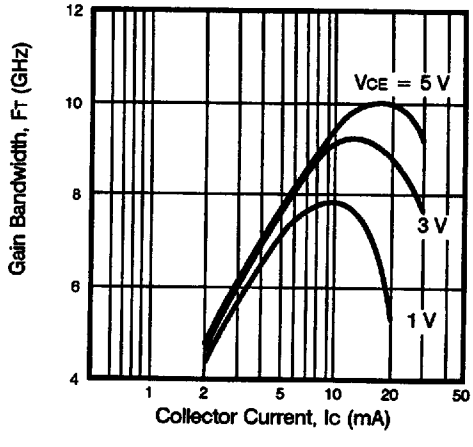
COLLECTOR CURRENT vs.
BASE TO EMITTER VOLTAGE



DC CURRENT GAIN vs.
COLLECTOR CURRENT



GAIN BANDWIDTH PRODUCT vs.
COLLECTOR CURRENT



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