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SIEMENS AKTIENGESELLSCHAF

T-65-15

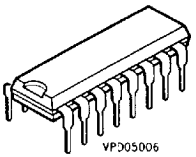
Intelligent Double High-Side Switch 2 × 0.5 A

TLE 4215

Bipolar IC

Features

- Double high-side switch, 2 × 0.5 A
- Power limitation
- Overtemperature shutdown
- Status monitoring
- Shorted-load protection
- Integrated clamp diodes
- Temperature range – 40 to 125 °C



P-DIP-16

Type	Ordering Code	Package
S TLE 4215	Q67000-A8184	P-DIP-16

Applications

Applications in automotive electronics require intelligent power switches activated by logic signals which are shorted-load protected and provide error feedback.

The IC contains two of these power switches (high-side switches). In case of inductive loads the integrated clamp diodes clamp the discharging voltage.

If a "high" signal is applied to the enable input both switches can be activated independently of one another through TTL signals at the control inputs (active high). The inputs are highly resistive and must therefore not be left unconnected, but should always be connected to a fixed potential (noise immunity).

The status output (open collector) signals the following malfunctions with high potential:

- Overload,
- Open load,
- Short-load to ground and supply,
- Overvoltage,
- Overtemperature.

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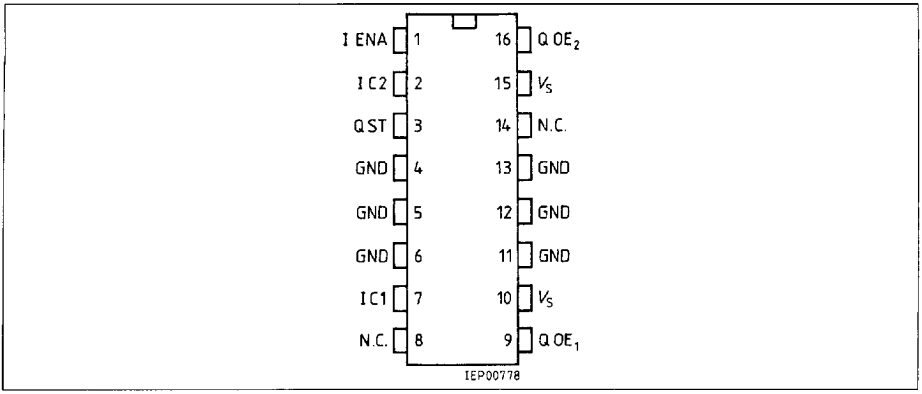
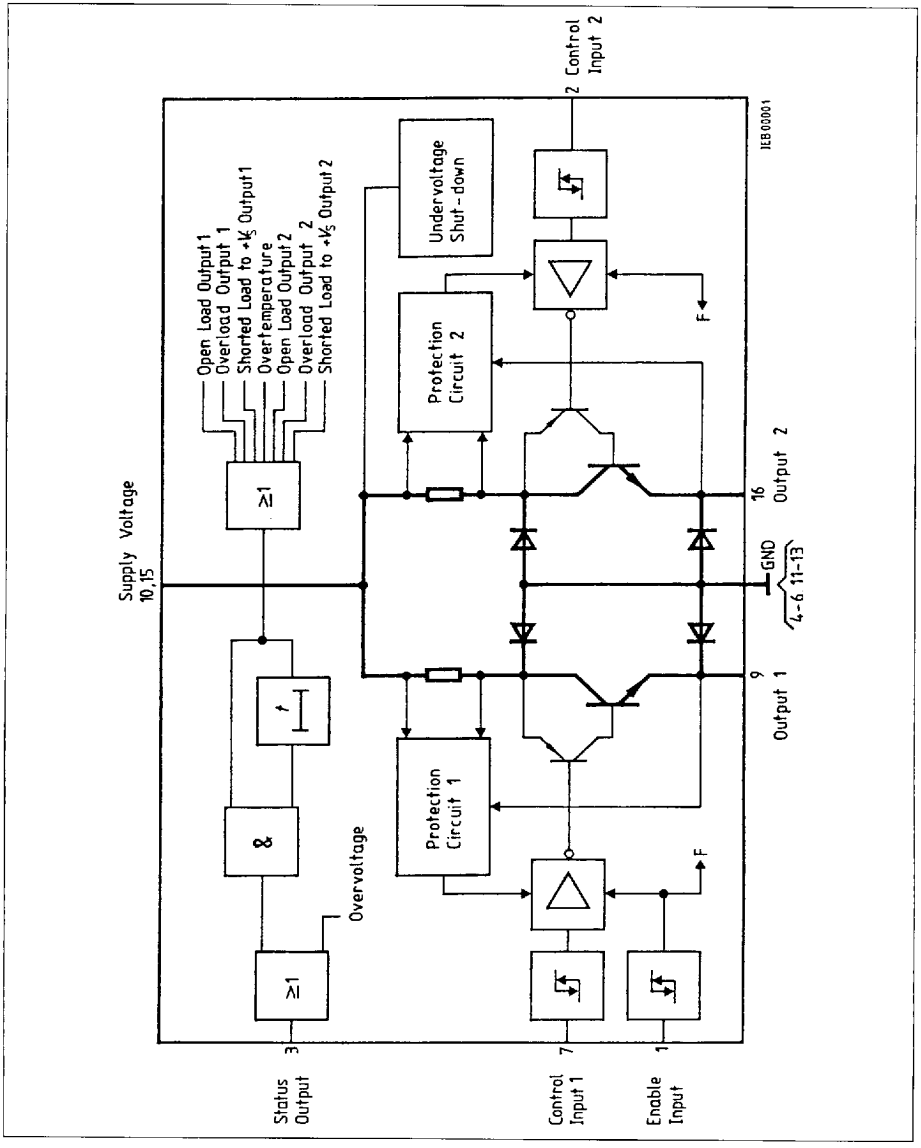


Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	ENA	**Enable input,** active high
2	IN2	**Control input 2** activates output transistor 2 (active high)
3	ST	**Status output** (open collector) for both outputs; monitors overtemperature, overload, open load, shorted load and supply overvoltage on pin 10 or 15; is switched off after a delay time in the event of a malfunction (exception: overvoltage).
4, 5, 6, 11, 12, 13	GND	**Ground**
7	IN1	**Control input 1** activates output transistor 1 (active high)
8	N.C.	Not connected
9	Q1	**Output 1,** shorted-load protected open emitter with negative clamp diode
10	V_S	**Supply voltage;** large parts of the circuit are deactivated if overvoltage appears on this pin; the status output will signal this malfunction without a delay time
14	N.C.	Not connected
15	V_S	**Supply voltage,** connected internally to pin 10; both pins should be put on + V_S
16	Q2	**Output 2,** shorted-load protected open emitter with negative clamp diode



Block Diagram

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Circuit Description

Input Circuits

The control inputs and the enable input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors.

Switching Stages

The output stages consist of NPN power transistors with an open emitter. Each stage has its own protective circuit for limiting power dissipation, which makes the outputs shorted-load protected to ground throughout the operating range. Integrated clamp diodes limit the discharging voltage of inductive loads.

Monitoring and Protective Functions

If the supply voltage V_S is too high or there is overtemperature, several parts of the circuit are shut down. Each output is monitored for open load and overload while activated. Furthermore, any shorting to the supply voltage is detected. The ORed information from these malfunctions are flagged on the status output (open collector, active high). An internally defined delay time for all malfunctions, except for overvoltage, prevents short-term faults from being signalled.

If the minimal supply voltage for a function is not maintained, the output stages become inactive.

Status Output (H = Error)

	Undervoltage	**Operating Range**		**Overvoltage**
	> 3.5 V	V_I = L (passive)	V_I = H (active)	
Normal function	L	L	L	H
Overload	L	L	H	H
Open load	L	L	H	H
Shorted load to +V_S	L	H	H	H
Overtemperature	L	H	H	H

Absolute Maximum Ratings
$T_j = -40$ to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage (pin 10, 15)	V_S	–	60	V	$t < 0.2$ s
Supply voltage (pin 10, 15)	V_S	– 0.3	42	V	–
Input voltage (pin 1, 2, 7)	V_{IN}	– 32	42	V	–
Output voltage (pin 3)	V_O	– 0.3	42	V	–
Output voltage (pin 9, 16)	V_O	– 0.3	+ V_S	V	–
Currents					
Output current (pin 9, 16)	I_Q	–	–	–	limited internally
Output clamp neg. current	I_Q	–	0.7	A	$t < 0.1$ s
Ground current (pin 4-6, 11-13)	I_{GND}	– 1.4	0.05	A	–
Output current (pin 3)	I_Q	–	10	mA	–
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Supply voltage	V_S	6 [1]	25	V	$T_j \leq 150$ °C
		–	16	V	for shorted load
Supply voltage slew rate	dV_S/dt	–1	1	V/µs	–
Output current	I_Q	–	500	mA	–
Input voltages	V_{IN}	– 10	40	V	–
Output current (pin 3)	I_O	0	5	mA	–
Ambient temperature	T_A	– 40	125	°C	$T_j \leq 150$ °C
Thermal Resistance					
Junction to ambient	$R_{th\,JA}$	–	60	K/W	–
Junction to case	$R_{th\,JC}$	–	15	K/W	–

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[1] Lower limit = 5.2 V if previously V_S was greater than 6 V (turn-on hysteresis)

Characteristics
V_S = 6 to 16 V; T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Data						
Quiescent current	I_S	–	2	5	mA	$V_E < V_{EL}$
Supply current	I_S	–	10	20	mA	$V_I = V_I > V_{IH}$; $V_E > V_{EH}$
Supply overvoltage shutdown threshold	V_{Sov}	30	36	40	V	V_L = 5 V; V_O > 4.5 V
Hysteresis of overvoltage shutdown	ΔV_{Sov}	3	6	9	V	V_L = 5 V; V_O > 4.5 V
Open load voltage switching threshold	V_{Ou}	–	200	800	mV	V_L = 5 V; V_O > 4.5 V
Open load current threshold	I_{Ou}	0.5		5	mA	$V_Q = V_{Qu}$
Logic						
Control inputs						
H-switching threshold	V_{IH}	1.2	1.8	2.2	V	pin 2, 7
L-switching threshold	V_{IL}	0.9	1.2	1.5	V	pin 2, 7
Hysteresis of input voltage	ΔV_I	0.2	0.6	1.0	V	pin 2, 7
H-switching threshold	V_{FH}	1.7	2.1	2.8	V	pin 1
L-switching threshold	V_{FL}	1.4	1.8	2.3	V	pin 1
Hysteresis of input voltage	ΔV_F	0.1	0.3	0.7	V	pin 1
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V; pin 1, 2, 7
L-input current	$-I_{IL}$	–	–	10	µA	V_I = 0.5 V; pin 1, 2, 7
Status Output (open collector)						
L-saturation voltage	V_{OSat}	0.1	0.2	0.4	V	I_O = 5 mA
Status delay time	t_{DS}	8	25	40	µs	1)
Switching Stages						
L-saturation voltage	V_{Lsat}	0.9	1.2	1.5	V	I_O = 0.5 A; $V_I > V_{IH}$; $V_E > V_{EH}$
Leakage current	I_{QL}	–	–	75	µA	$V_I < V_{IL}$; V_S = 6V; V_Q=0 V
Turn-ON time	t_{DON}	0.2	0.5	5	µs	**see Timing**
Turn-OFF time	t_{DOFF}	0.2	1	5	µs	**Diagram;** I_Q = 0.5 A
Output voltage negative clamp	$-V_Q$	0.8	1.3	1.7	V	I_Q = 0.5 A; t < 0.1 s

1) Time from beginning of malfunction on channel (exception: overvoltage) up to 50 % value of status switching edge

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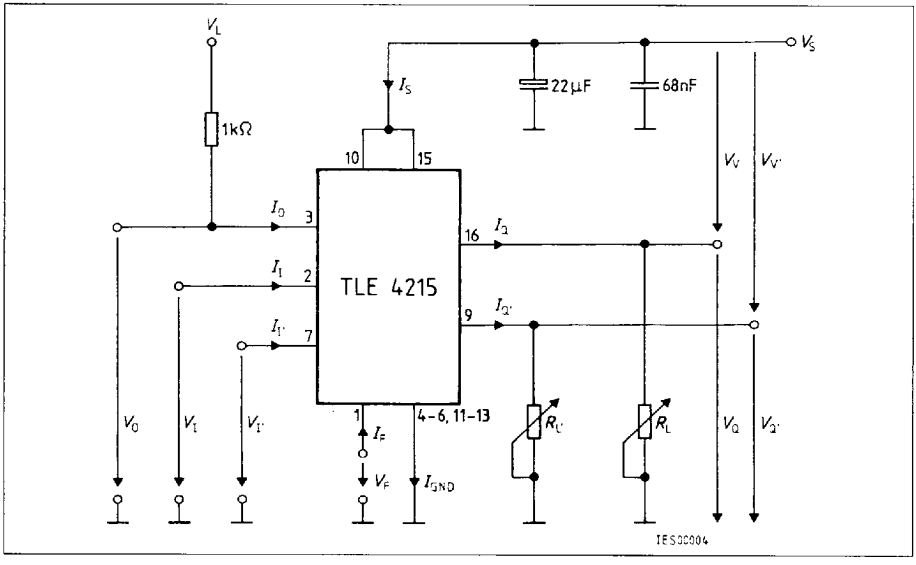
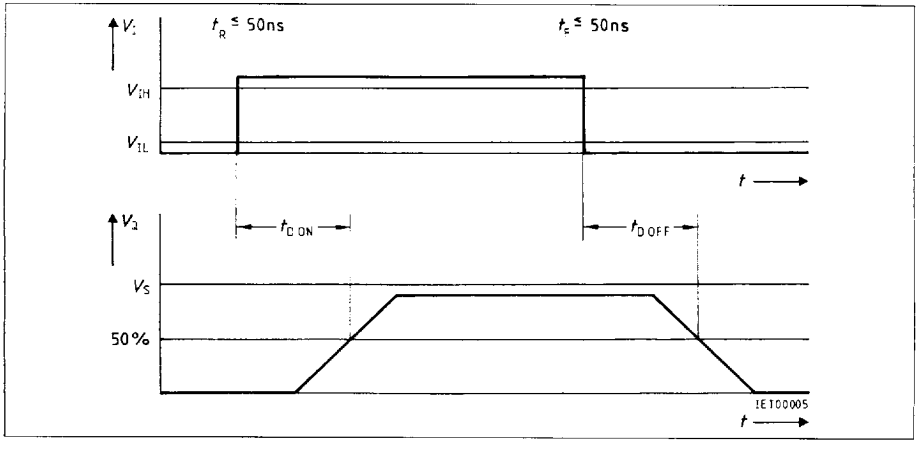


Test Circuit



Timing Diagram

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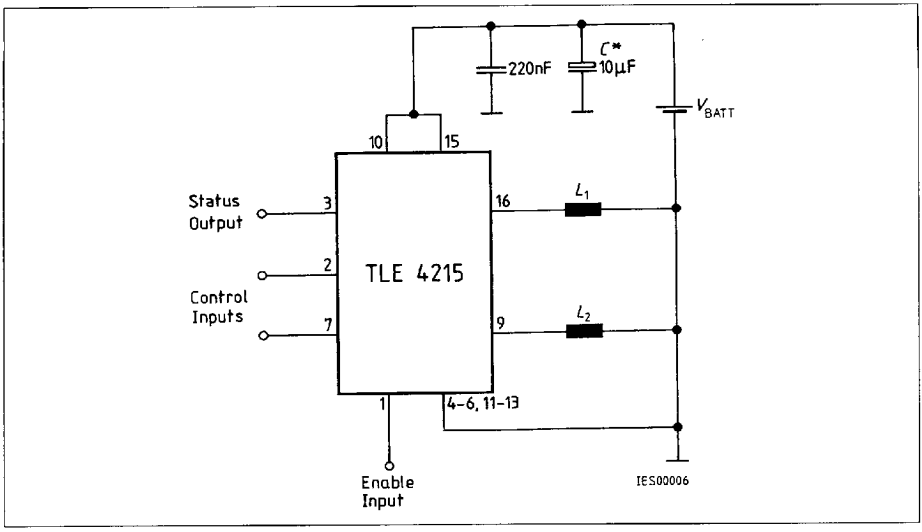

Application Circuit

C^* is to be dimensioned such that in case of an incoming-line failure the maximum ratings are not exceeded by the recirculation energy of L_1, L_2.

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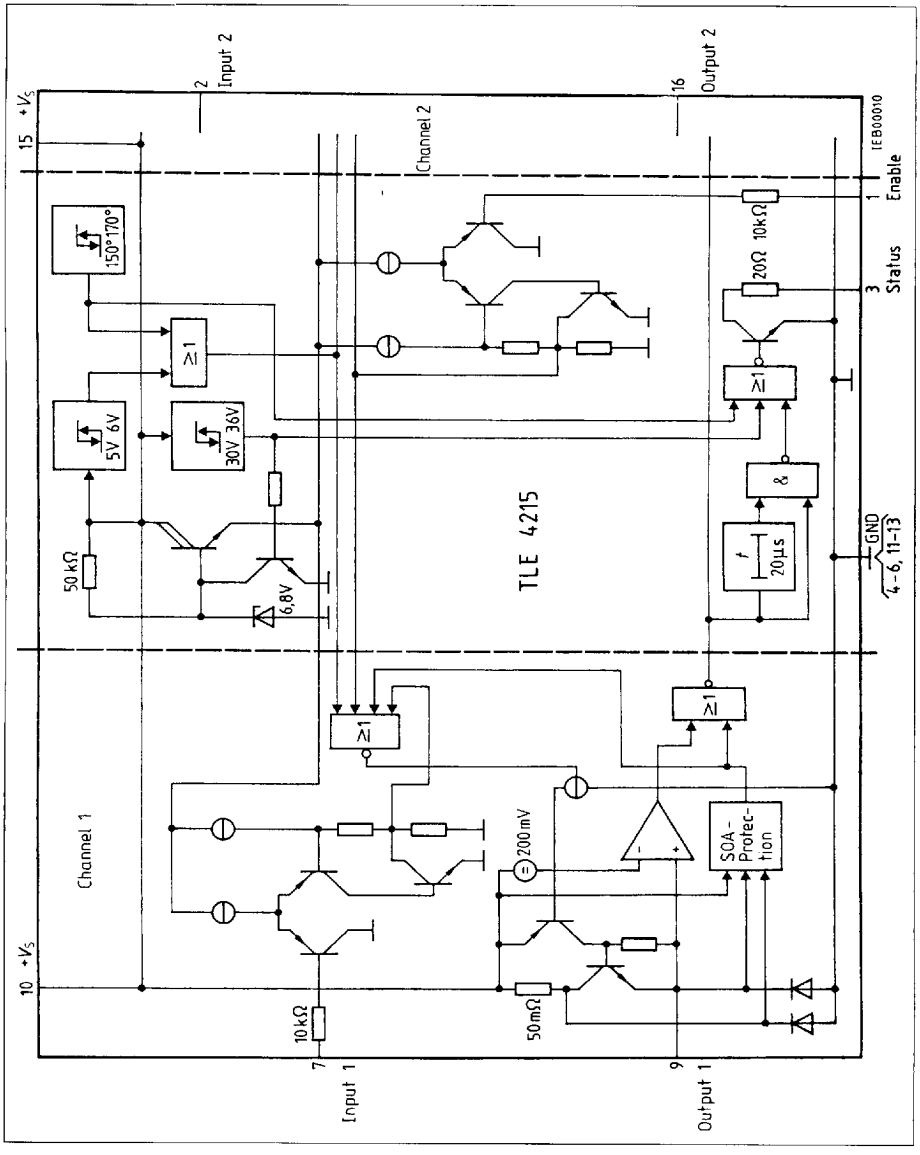

Circuit Diagram

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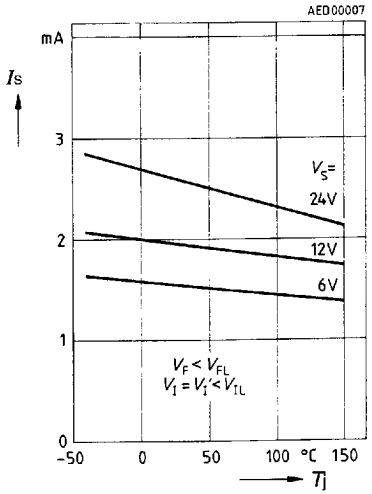
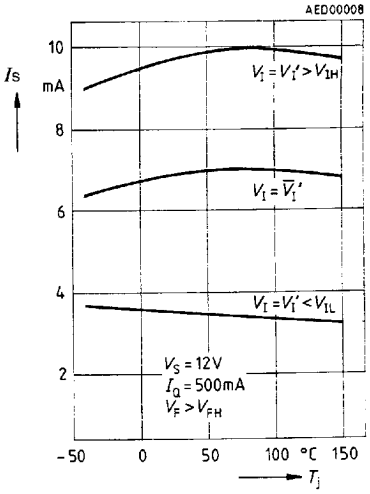
Diagrams

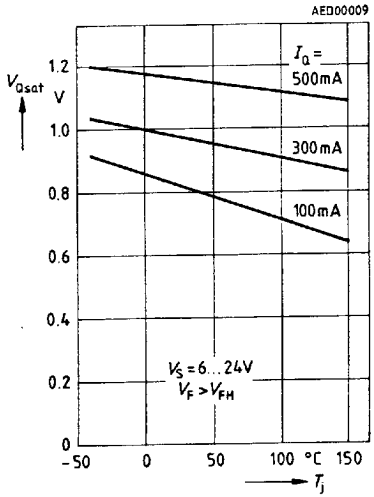
Typ. Quiescent Current I_S versus T_j in the OFF-State



Typ. Supply Current I_{GND} versus Chip Temperature T_j in ON-State



Typ. Output Saturation Voltage V_{Qsat} versus Chip Temperature T_j



Typ. Output Leakage Current I_{QL} versus Supply Voltage V_S