

TC40H166P/F

**C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC****TC40H166 8-BIT SHIFT REGISTER (P/S-IN, S-O)**

The TC40H166 is an 8-bit PARALLEL-IN and SERIAL-OUT shift register, permitting SERIAL-IN and SERIAL-out operations.

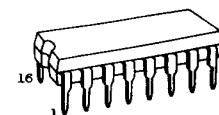
In PARALLEL operation, PARALLEL-IN DATA are shifted at the rising edge of CLOCK in sequence and outputted from the final stage of F/F.

In SERIAL operation, each F/F is triggered at the rising edge of CLOCK.

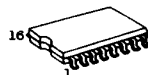
Switching of PARALLEL operation and SERIAL operation is made by SHIFT/LOAD input

When SHIFT/LOAD input is at "H" level, SERIAL operation is performed, and when SERIAL operation is at "L" level, PARALLEL operation is performed.

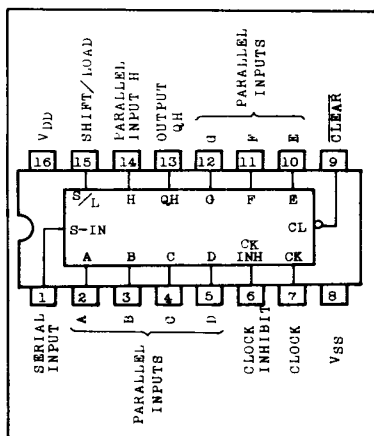
The function and pin assignment of the TC40H166 are the same as those of the 74LS166.



DIP16 (3D16A-P)



MFP16 (F16GC-P)

PIN CONNECTION**MAXIMUM RATINGS**

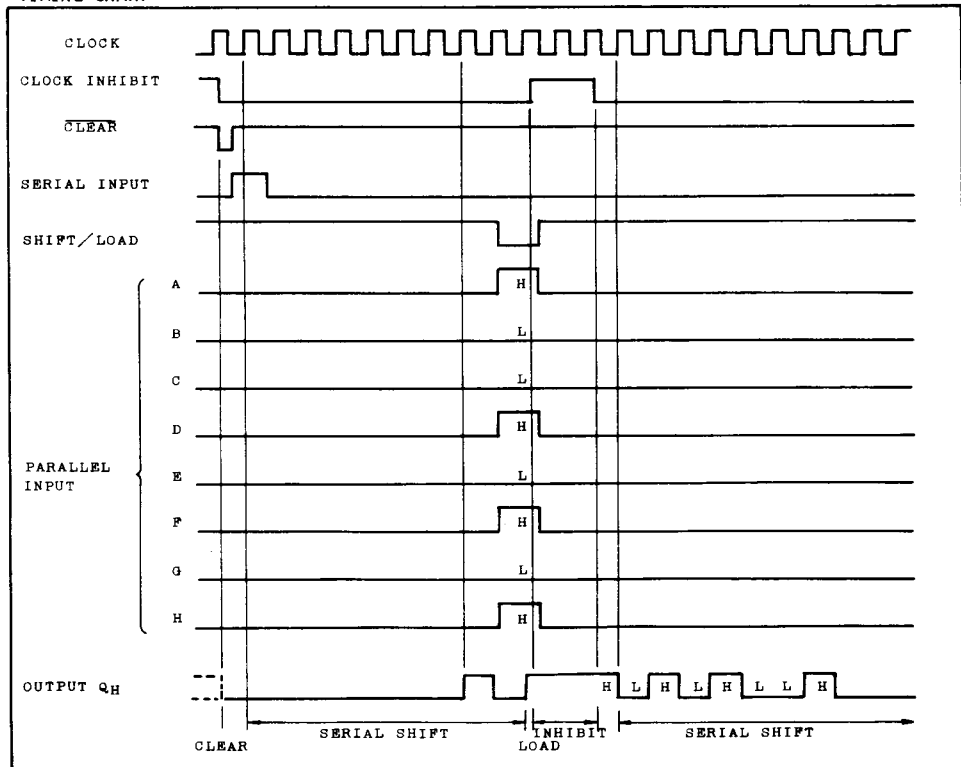
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	VIN	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	VOUT	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	IIN	± 10	mA
Power Dissipation	PD	300(DIP)/180(MFP)	mW
Storage Temperature	Tstg	$-65 \sim 150$	°C
Lead Temp./Time	Tsol	$260^{\circ}\text{C} \cdot 10 \text{ sec}$	

RECOMMENDED OPERATING CONDITIONS (VSS=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	-	2.0	-	8.0	V
Input Voltage	VIN	-	0	-	VDD	V
Operating Temperature	Topr	-	-40	-	85	°C

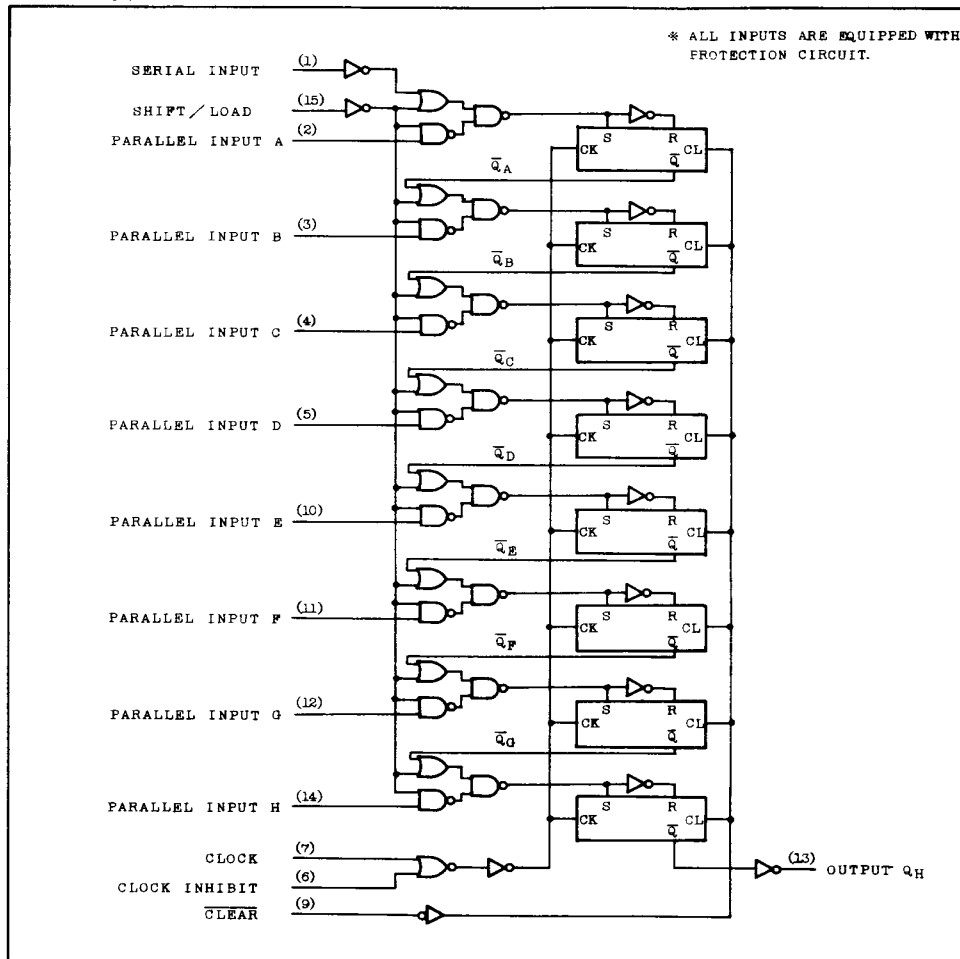
TC40H166P/F**TRUTH TABLE**

CLEAR	SHIFT/ LOAD	INPUTS					OUTPUTS			FUNCTION MODE
		CLOCK INHIBIT	CLOCK	SERIAL INPUT	PARALLEL INPUT		INTERNAL		QH	
L	*	*	*	*	*	*	L	L	L	Clear
H	H	L	↑	L	*	*	L	Q _{An}	Q _{Qn}	Shift
H	H	L	↑	H	*	*	H	Q _{An}	Q _{Qn}	
H	L	L	↑	*	L	L	L	P _{INB}	L	Parallel Load
H	L	L	↑	*	L	H	L	P _{INB}	H	
H	L	L	↑	*	H	L	H	P _{INB}	L	
H	L	L	↑	*	H	H	H	P _{INB}	H	
H	*	H	*	*	*	*	Q _{AO}	Q _{BO}	Q _{HO}	Hold
H	*	*	↓	*	*	*	Q _{AO}	Q _{BO}	Q _{HO}	No change

* = Don't care Q_{no} = Data one clock before**TIMING CHART**

TC40H166P/F

BLOCK DIAGRAM



TC40H166P/F

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current	I _{OH}	V _{OH} =4.6V V _{IN} =V _{SS} , V _{DD}	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I _{OL}	V _{OL} =0.4V V _{IN} =V _{SS} , V _{DD}	5	1.4	-	1.1	-	-	0.8	-	
Input Voltage	"H" Level V _{IH}	I _{OUT} < 1μA V _{OUT} =0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level V _{IL}	V _{OUT} =4.5V	5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level I _{IH}	V _{IH} =8.0V	8	-	0.3	-	10 ⁻⁵	0.3	-	1.0	μA
	"L" Level I _{IL}	V _{IL} =0.0V	8	-	-0.3	-	10 ⁻⁵	-0.3	-	-1.0	
Quiescent Supply Current	I _{DD}	*V _{IN} =V _{SS} , V _{DD}	5	-	12.5	-	10 ⁻³	12.5	-	75	μA

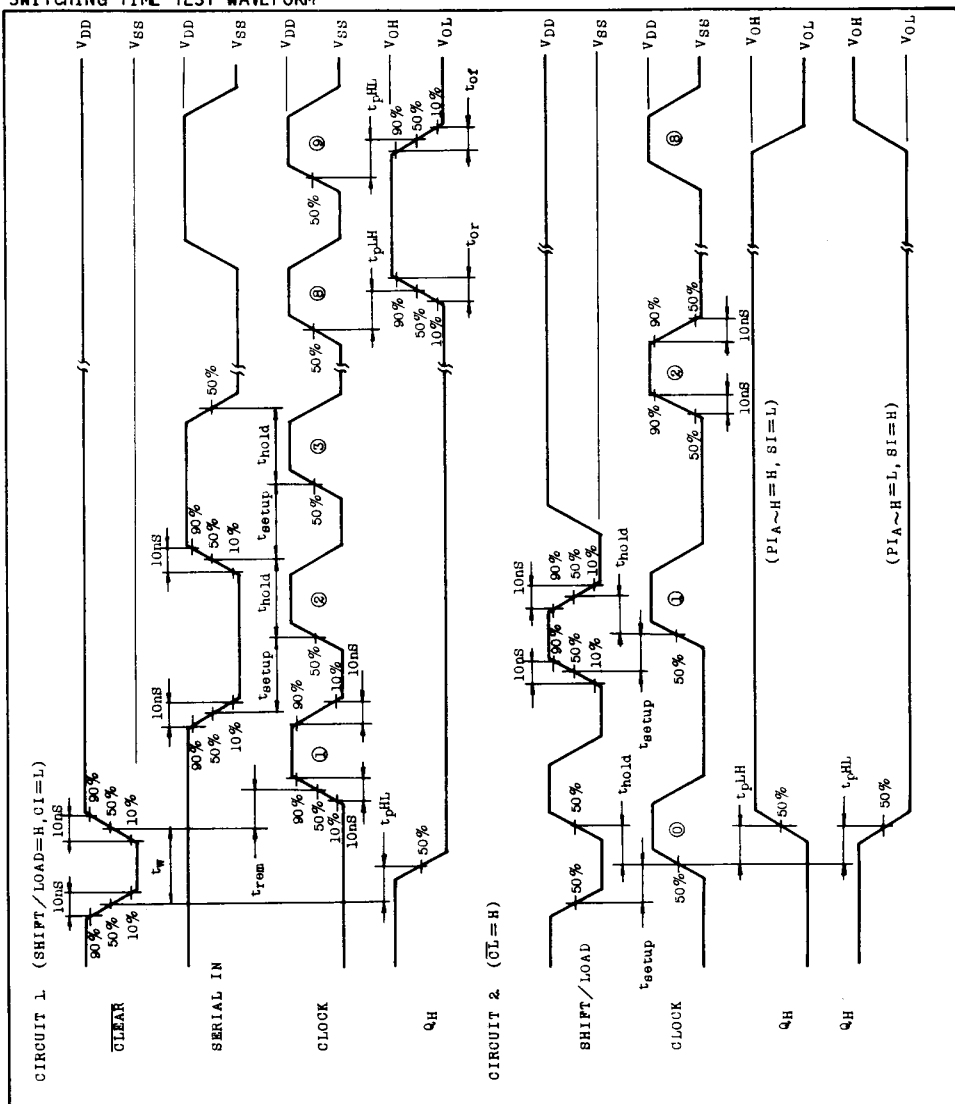
*All valid input combinations.

SWITCHING CHARACTERISTICS (T_a=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t _{or}	Fig. 1	-	17	35	ns
Output Fall Time		t _{of}		-	14	30	
Propagation Delay Time	(Low-High)	t _{pLH}	CLOCK - Q _H Figs.1,2,3	-	29	44	ns
	(High-Low)	t _{pHL}		-	36	54	
Propagation Delay Time (High-Low)		t _{pHL}	CLEAR - Q _H Fig. 1	-	38	57	ns
Maximum Clock Frequency		f _{maxφ}		15	25	-	MHz
Max Clock Rise Time Fall Time		t _{rφ} , t _{fφ}			20	-	μs
Min. Clear Width of Pulse		t _W	Fig. 1	-	15	27	ns
Min. Clear Remobal Time		t _{rem}	Fig. 2	-	12	25	ns
Min. Data Setup Time		t _{set-up}	PI, SI Fig. 1, 3	-	-	25	ns
Min. Data Setup Time		t _{set-up}	SHIFT/LOAD Fig. 2	-	-	35	ns
Min. Data Hold Time		t _{hold}	PI, SI Fig. 1, 3	-	-	0	ns
Min. Data Hold Time		t _{hold}	SHIFT/LOAD Fig. 2	-	-	0	ns
Input Capacitance		C _{IN}		-	5	-	pF

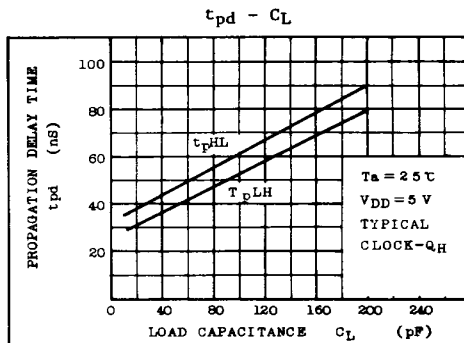
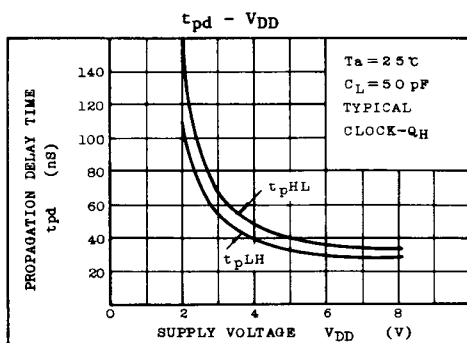
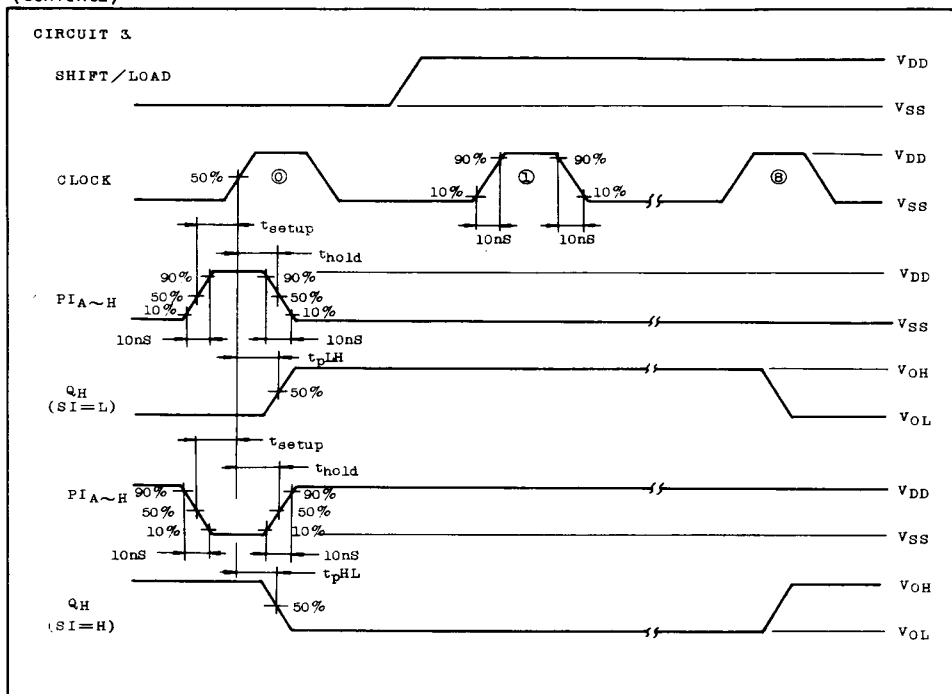
TC40H166P/F

SWITCHING TIME TEST WAVEFORM



TC40H166P/F

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TC40H166P/F

