

TC35190F

(Video-data Compression and Expansion Controller*)

1988-11-03

DESCRIPTION

TC35190F (VCEC*) performs encoding and decoding of video-data based on the CCITT Recommendations T.4 and T.6.

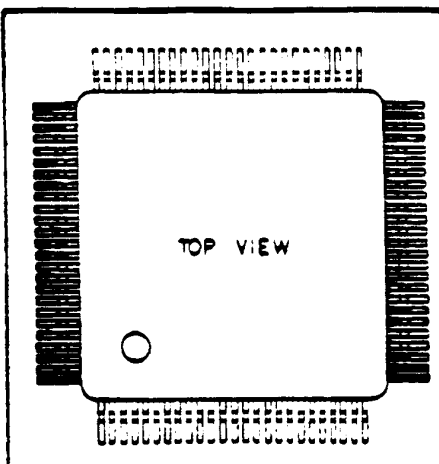
Only with simple initialization, the VCEC* processes a page of data without any host processor's help.

FEATURES

- ☐ High speed data transfer
- ☐ 3 independent 8-bit buses
- ☐ Directly connectable with Intel/Zilog 8bit MPU
- ☐ Can access maximum 8k-byte line memory
- ☐ Horizontal video sizes from 32 to 7736pels/line
- ☐ A variety of processing mode by parameter set-up
 - Minimum number of transmission bit
 - Line-Pad-Bit
 - Number of 'RTC' component 'EOL'
 - Number of 'RTC' detective 'EOL'
- ☐ 8-bit error line counter
- ☐ CMOS Low Power (Typical 100 nA)
- ☐ +5V single power supply
- ☐ LFP100 Plastic Package

Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit
Supply Voltage	VDD	- 0.5 ~ 7.0	V
Input Voltage	Vin	- 0.5 ~ 7.0	V
Output Voltage	Vout	- 0.5 ~ 7.0	V
Operating Temperature	Topr	0 ~ 70	°C
Storage Temperature	Tstg	- 55 ~ 150	°C
Soldering Temperature	Tsol	260°C • 10 sec	



No	Name	No	Name	No	Name	No	Name
1	VDD	26	T6	51	MDC	76	VSS
2	CD0	27	RAS	52	MD1	77	IRQ
3	CD1	28	RTR	53	MD2	78	PREQ
4	CD2	29	CAS	54	MD3	79	PACK
5	CD3	30	VDD	55	VDD	80	VR
6	VSS	31	VSS	56	VSS	81	RES
7	VDD	32	MA12	57	MD4	82	VSS
8	CD4	33	MA11	58	MD5	83	VDD
9	CD5	34	MA10	59	MD6	84	D0
10	CD6	35	MA9	60	MD7	85	D1
11	CD7	36	MA8	61	VDD	86	D2
12	VDD	37	VDD	62	VDD	87	D3
13	VSS	38	VSS	63	VSS	88	VSS
14	VSS	39	MA7	64	VSS	89	VDD
15	VDD	40	MA6	65	PDC	90	D4
16	CREQ	41	MA5	66	PD1	91	D5
17	CACK	42	MA4	67	PD2	92	D6
18	T1	43	VDD	68	PD3	93	D7
19	T2	44	VSS	69	VDD	94	VSS
20	T3	45	MA3	70	VSS	95	AC
21	T4	46	MA2	71	PD4	96	A1
22	T5	47	MA1	72	PD5	97	CS
23	CLK	48	MA0	73	PD6	98	RD
24	VSS	49	VSS	74	PD7	99	VSS
25	VDD	50	VDD	75	VDD	100	VDD

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PIN DESCRIPTION

System Terminals

Pin Name	I/O	Functions
VDD	Input	Connect +5V
VSS	Input	Connect +5V
CLK	Input	Input VCEC+ system clock
RES	Input	When VCEC+ is reset by hardware, this pin is set at 'L' level
IRQ	Output	Interrupt request signal to 'NPU'

MPU BUS Control Terminals

Pin Name	I/O	Functions
CS	Input	When 'NPU' access VCEC+, this pin is set at 'L' level
RD	Input	When 'NPU' reads data from internal register, this pin is set at 'L' level
WR	Input	When 'NPU' writes data into internal register, this pin is set at 'L' level
A0	Input	Internal register selecting address
A1		
D0	I/O 3State	This pin is LSB
D1		8-bit bus to read/write data from/into Internal Register Connect 'NPU' data buses
D2		
D3		
D4		
D5		
D6		
D7		This pin is MSB

PIX BUS Control Terminals

Pin Name	I/O	Functions
PREQ	Output	Signal requesting data transfer to Scanner & Printer side
PACK	Input	Response signal from the Scanner & Printer side to 'PREQ' signal
PD0	I/O 3State	- This pin is LSB
PD1		- Decoding mode • PIX data output
PD2		- Decoding mode • Enable signal input
PD3		- Decoding mode • Synchronous signal input
PD4		- Decoding mode • Line-End signal output
PD5		- Encoding mode • Synchronous signal input
PD6		- Encoding mode • Enable signal input
PD7		- This pin is MSB
		- Encoding mode • PIX data input

Note) Serial mode is future function. Not supported!

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CODE BUS Control Terminals

Pin Name	I/O	Functions			
CREQ	Output	Signal requesting data transfer to Communication-Line & data-storage side			
CACK	Input	Response signal from Communication-Line & data-storage side to 'CREQ' signal			
CD0	I/O 3State	-	This pin is LSB	-	Encoding mode • data data output CODE
CD1		u		-	Encoding mode • Enable signal input
CD2		-		-	Encoding mode • Synchronous signal input
CD3		-		-	
CD4		u		u	
CD5		-		u	Decoding mode • Synchronous signal input
CD6		u		u	Decoding mode • Enable signal input
CD7		-	This pin is MSB		Decoding mode • data data input CODE

Note) Serial mode is future function. Not supported.

Line-Memory Control Terminals

Pin Name	I/O	Functions			
RAS	Output	Reserved. Use in open state. For future connection of Dynamic RAM.			
CAS	Output	Use for 'OE' signal of Static RAM. ('CAS' signal of Dynamic RAM)			
MWR	Output	Use for 'Write' signal of RAM			
MD0	I/O 3State	-	This pin is LSB	8-bit buses for exchanging data with Line memory	
MD1					
MD2					
MD3					
MD4					
MD5					
MD6					
MD7		-	This pin is MSB		
MA0	Output	-	This pin is LSB	18-bit address signals of RAM.	
MA1					
MA2					
MA3					
MA4					
MA5					
MA6					
MA7					
MA8					
MA9					
MA10					
MA11					
MA12		-	This pin is MSB		

Note) Dynamic RAM is not supported.

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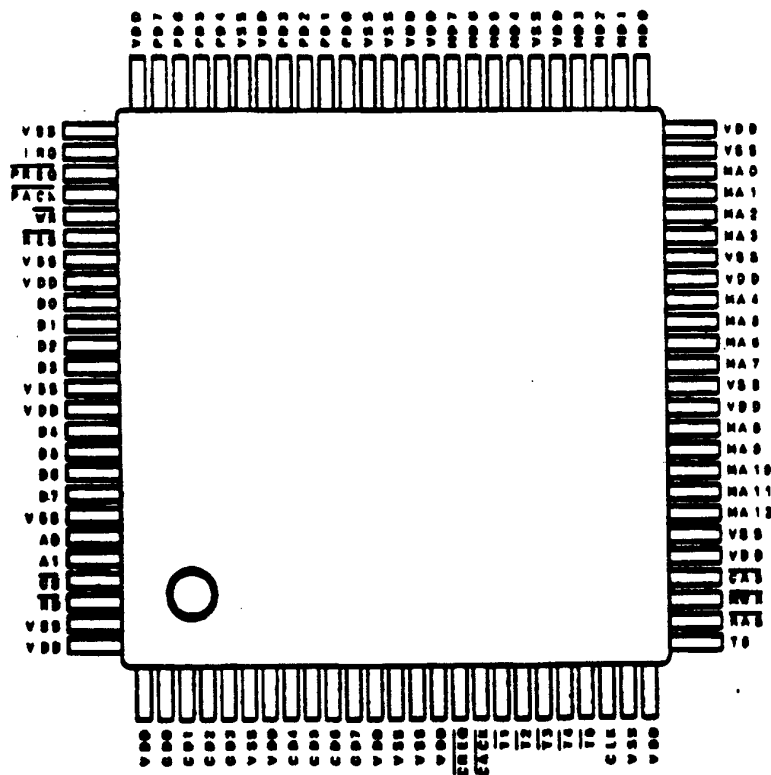
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□ Test Terminals

Pin Name	I/O	Functions
T 1	Input	Test terminal 1. Keep at 'H' level during normal operation.
T 2	Input	Test terminal 2. Keep at 'H' level during normal operation.
T 3	Input	Test terminal 3. Keep at 'H' level during normal operation.
T 4	Input	Test terminal 4. Keep at 'H' level during normal operation.
T 5	Input	Test terminal 5. Keep at 'H' level during normal operation.
T 6	Output	Test terminal 6. Use in 'OPEN' state during normal operation.



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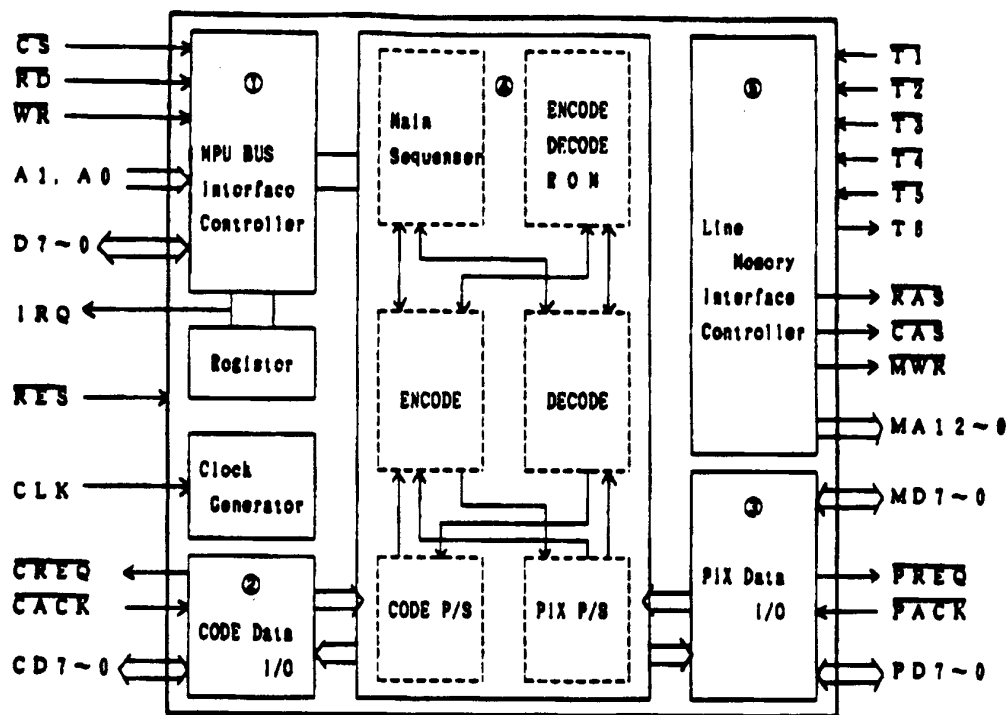
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BLOCK DIAGRAM



Internal Block Diagram

① MPU BUS Interface Block

This block consists of the MPU BUS interface, connectable with 80Series MPU, and Registers. Processing mode is set by write access operations. If the IMR (Interrupt Mask Register) is set at no-masking mode, the VCEC⁺ drives the 'IRQ' signal at High level, whenever the 'IRQ' line is occurred. The host processor finds the operating status or interrupt request line by reading operation.

② CODE BUS Interface Block

This block controls the coded-data transfer timing. Coded-data-BUS (CD7-0) connects to the 'Communication Line' or 'Data storage memory'. When the VCEC⁺ prepare for the coded-data, the 'CREQ' signal is active. More detailed timing, refer to after page: CODE BUS AC Timing.

③ PIX BUS Interface Block

This block controls the Pix-data transfer timing. Pix-data-BUS (PD7-0) connects to the Scanner and Printer side. When the Line-memory has enough space for data storage, the 'PREQ' signal is active. More detailed timing, refer to after page: PIX BUS AC Timing.

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④ Encoding and Decoding Block

This block consists of 'the Main Sequencer', 'Code/Decode ROM', 'Coding control', 'Decoding-control', 'Code-data parallel to serial transfer' and 'Pix-data parallel to serial transfer'

☐ Main sequencer unit

Controls each block of VCEC[®] according as the micro-program stored in Main-Sequencer-ROM. This is compatible with CCITT recommendations T.4 and T.8 for Group-III and Group IV facsimile. [Modified Huffman coding / Modified READ / Modified Modified READ]

☐ Code/Decode ROM unit

Consists of 3-Encoding ROMs and 3-Decoding ROMs.

Encoding ROM : Run-Length ROM , Encoding mode set ROM , Minimum Number of Transition bit set ROM

Decoding ROM : Run-Length ROM , Decoding mode set ROM , Uncompressed mode decoding ROM

☐ Encoding unit

Detects color changing point, and generates coded-data using MH,MR,or,MMR coding algorithms.

☐ Decoding unit

Compares the data with code-table, and generates the video-image-data corresponding with Run-Length Decode ROM.

☐ Video-image-data parallel to serial converter unit

In the case of encoding, 8-bit parallel Video-image-data, inputs from PIX BUS interface, converts into serial data. And send to Encoding unit. In the case of decoding, serial to parallel conversion is carried out.

☐ Coded-data parallel to serial converter unit

This unit acts in similar fashion, as video-image-data parallel to serial converter unit. But, in this unit, parallel to serial conversion carries out in decoding operation. Serial to parallel conversion is in encoding operation.

⑤ Line memory Interface control Block

This block consists of Memory address BUS (18 bit), and Memory control signals (RAS , CAS , NVR). Controls Write/Readaccess timing ; Stops write operation before the line-memory becomes full, or stops read operation before short. In the case of decoding, if any error occurs, performs the pre-coding line substitution.

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OPERATIONAL DESCRIPTION

□ Summary

The VCEC[®] is facsimile CODEC Processor. After initialization, the VCEC[®] processes a page of data automatically. If the document consists of more than one sheet, initialization procedure should be done before coding (decoding) starts. More details of initialization process explains after page : Initialization and Termination Process

Note) Following sentence

- '1' means High level input
- '0' means Low level input
- 'H' means High level output
- 'L' means Low level output

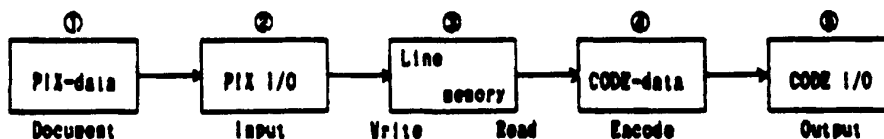
□ Encoding

When 'STRT' bit of the System Control Set Register (SCSR), is set at '1', then coding process starts. Coded-data generates according to the coding algorithm, setting in Register by initialization. In case of coding, PIX BUS interface functions as INPUTS, and CODE BUS interface functions as OUTPUTS. If the system detects 'PREG' is 'L', NPU should be ready for PIX-data, and keeps 'PACK' signal at '0' for the resolving time. Data is gotten by system in rising edge of 'PACK', and stored in the line memory. When this stored data reaches a set-up paper width, the coding is started. A coded-data is generated whenever the VCEC[®] detects changing color point. Further, the 'EOL' code is generated every line's data has been coded. In the CODE BUS interface, a valid data is output during 'CACK' is at '0'. When the MH or MR coding is started, the system generates the End-Of-Line code (EOL) at first. After PIX-data has been input, the NPU should be done Terminating procedure. When the VCEC[®] is set to Waiting-mode, the data remains in the line memory, is encoded.

After this, Return-To-Control code (RTC) is generated. In this time, 'PKD' bit of the Interrupt Mask Register (IMR) is active, then 'IRQ' becomes 'H'. After coding a page of data, IF the document has next page, NPU could be done re-start procedure. And whole pages data of the document has been coded, NPU sets the VCEC[®] is in initializing state.

In MH coding, 'EOL' code is not using, then coded-data is generated serially. And End-Facsimile-Block code (EOPB) uses instead of 'RTC' code.

Note) PIX : picture element



Encoding mode Data Flow

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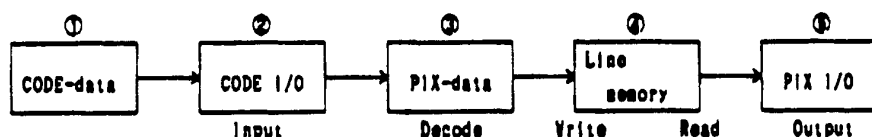
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□ Decoding

In the case of decoding, CODE BUS interface functions as INPUT, and PIX BUS interface functions as OUTPUT. The VCEC⁺ decodes the coded-data, and it is stored in the line memory. When the MH or MR decoding mode is selected, the VCEC⁺ searches 'EOL' code at first. If the coded-data contains any error, or the paper width could not be re-generated, the VCEC⁺ prepares the previous decoded-line's data instead of this one. If the MNR mode is selected, the VCEC⁺ stops all the operations after 'DERM' bit of Interrupt Request Register (IRR) is active. In this moment, VCEC⁺ should be initialized again by host processor.



Decoding mode Data Flow

□ EOL code and RTC code

'EOL' code is composed of 11 bit of '0' + 1 bit of '1' : (00000000001). In practice, decoder recognizes 'EOL' code, detects more than 11 bit of '0' + 1 bit of '1'. In MR coding, the system using 'EOL'+1' or 'EOL'+0' for distinguish one-dimensional-coding-line or two-dimensional-coding-line. The one-dimensional coding line is encoded by using MH coding algorithm, and the two-dimensional-coding-line is encoded by MR. In coding side, the VCEC⁺ transmits 8 or 9 times of 'EOL' codes continuously. In decoding side, a series of 2 or 3 times of 'EOL' codes detection means 'RTC' code detection. These are able to select by Register setting. In MNR coding, 'EOPB' code is used, instead of 'RTC' code. 'EOPB' code composed of 2 times of 'EOL' code.

□ Fill-bit and Line-pad-bit

If every line's coded-data is less than Minimum Number Of Transmission Bit (MNTB), add '0' to the end of every line's coded-data, reaches to MNTB. This '0' data, additional coded-data is called Fill-bit. If the coded-data is not composed of in unit of byte, '0' data is added. This '0' data is called Line-pad-bit.

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□ Transparent mode

If this mode is selected, the data is transmitted without coding, and received data is not decoded. This mode has a time lag, from data input to output. Because the data is stored in the line memory once, and it is not output until equivalent of one-line's data is stored.

□ White line skip mode

In this mode, if a coded-data of one-line composed of white pels only is short to 'NMTB', the system adds '0' data equivalent to a half of the 'NMTB'. For using in this mode, the MPU set at half of 'NMTB' by setting the 'NMTB' set bits of Parameter Register (PR).
ex.) the codes speed is 9600 bps : 10 ns/line

$$9600 \times 10^{-3} = 96 \text{ (bit/sec)} \quad 96 / 2 = 48 \text{ (bit/sec)}$$

In this case, 'NMTB' should be set 48 bit/line. More detail of 'NMTB' setting is explained at the following page : Parameter Register (Setting table for 'NMTB')

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Register

VCEC+ is able to a variety of processing mode by parameter set-up. The set-up depends on register setting by initialization. These registers are consists of 8-words of mode-set-registers and 4-words of status registers. In the first case, it is accessible to writing operation from MPU, and in the latter case, accessible to reading operation.

Mode set Registers

For setting the VCEC+ 's processing mode (Writing Operation)

Register address		Access	Register Name
A 1	A 0		
0	0	1st.	SCSR Register (System Control Set Register)
0	1	1st.	IMR Register (Interrupt Mask Register)
1	0	1st.	RSR Register (RAM Size Register)
1	0	2nd.	PR Register (Parameter Register)
1	1	1st.	PVWL Register (Paper Width Register of Low)
1	1	2nd.	PVRH Register (Paper Width Register of High)

Note) In writing operation, if the register address is (A1.A0)=(1.0) or (A1.A0)=(1.1) is selected, the difference register is accessed in the first or the second access.

Status Registers

For indicating the VCEC+ 's operating status (Read Operation)

Register address		Access	Register Name
A 1	A 0		
0	0	1st.	SCNR Register (System Control Notice Register)
0	1	1st.	IRR Register (Interrupt Request Register)
1	0	1st.	LSR Register (Line-memory Status Register)
1	1	1st.	ELR Register (Error Line Register)

Note) More details of Register setting are following topics : Initialization and Termination process.

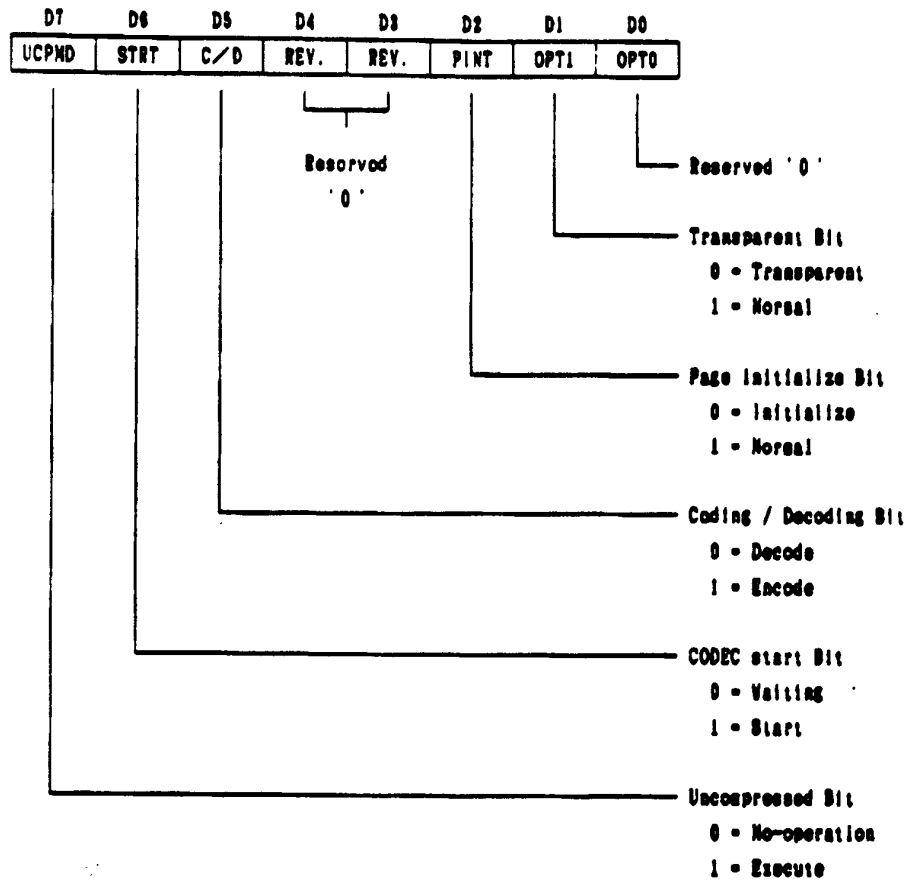
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□ SCSR (System Control Set Register)



'SCSR' is accessible to writing operation by setting register address (A1.A0)=(0.0).

Bit D1 of 'SCSR' is Transparent mode set bit. The Transparent mode is explained by another topics : Operational Description. Page Initialize bit should be set at 'Initialize' whenever set-up the VCCEC*. Coding/Decoding Bit selects the Coding or the Decoding. CODEC start Bit should be set at 'waiting' during initialization. Uncompressed Bit works in Decoding mode. Uncompressed mode is the optional coding of the Recommendation of T4 or T8. More details of this coding, refer to the Recommendation of CCITT.

Note) Reserve bits of this register are always set at '0'

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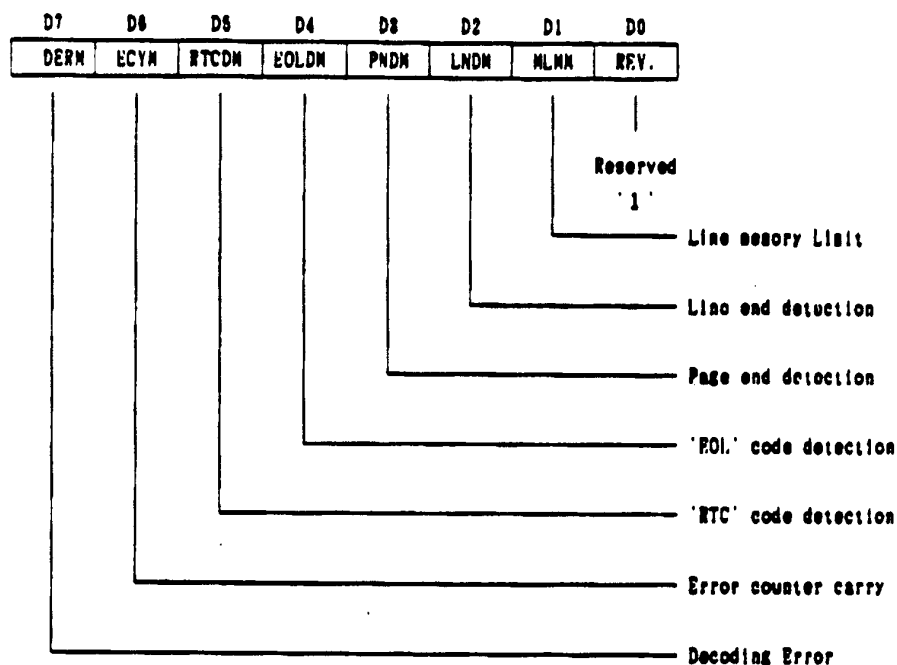
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☐ I M R (Interrupt Mask Register)



'IMR' is accessible to writing operation by setting register address (A1.A0)=(0.1).

This register controls for interruption to the host processor. Meaning of each bit is explains following table. If each bit is set at '0', VCEC+ carries out the interruption of meaning of the bit. All the bits of this register are set at '1', the interruption is not occurred.

Rit	Name	Encoding	Decoding
D7	DERN		Error detection(unit of line)
D6	ECYN		Error counter carry (8-bit counter)
D5	RTCDN		'RTC' code detection
D4	EOLDN		'EOL' code detection
D3	PNDN	Output the last code of a page	Output the last data of a page
D2	LNDN	Generate the 'EOL' code	Output the last data of a line
D1	MLNN	Memory is Full	Line memory is empty
D0	REV.		

Note) Reserve bit of this register is always set at '1'

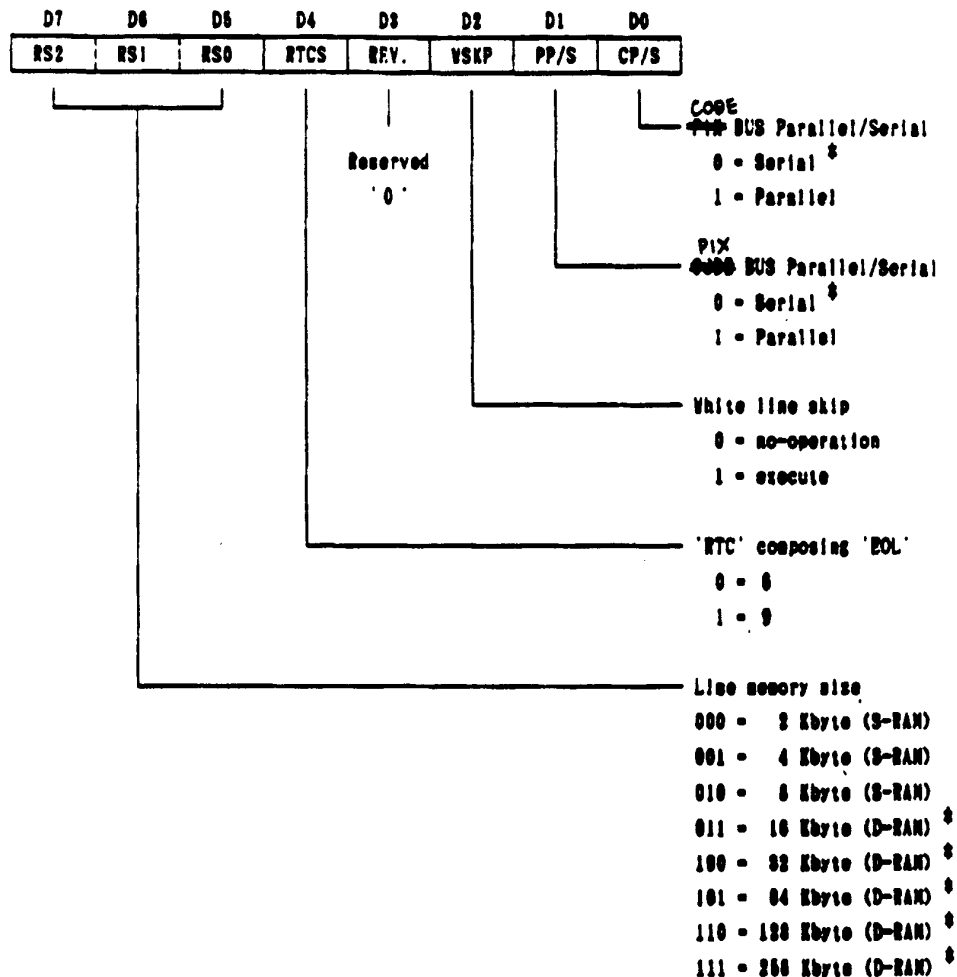
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□ RSR (Ram Size Register)



'RSR' is accessible to writing operation by setting register address (A1.A0)=(1.0) of the first access.

Serial mode is not supported now, then bit D0 and D1 is always set at '1'. And now the VCEC[†] can connect static-RAM only for the line memory. Then bit D7.D6 and D5 is able to set at (0.0.0), (0.0.1), or (0.1.0) only. White line skip is explained another topics. 'RTC' composing 'EOL' is selectable in bit D4.

Note) Reserve bit of this register is always set at '0'

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□ PR (Parameter Register)

D7	D6	D5	D4	D3	D2	D1	D0
MTB4	MTB3	MTB2	MTB1	MTB0	K2	K1	K0

K-Parameter and mode

000 - MH

001 - MR (K=2)

010 - MR (K=4)

011 - MR (K=8)

100 - MR (K=16)

101 - MR (K=32)

110 - MR (K=∞)

111 - MMR

'MNTB' ‡

Refer to following table

D7	D6	D5	D4	D3	MNTB	D7	D6	D5	D4	D3	MNTB	D7	D6	D5	D4	D3	MNTB
0	0	0	0	0	0	0	0	1	0	1	144	1	0	1	1	0	32
0	0	0	0	1	51	0	1	1	0	0	192	1	0	1	1	1	80
0	0	0	1	0	15	0	1	1	0	1	240	1	1	0	0	0	160
0	0	0	1	1	30	0	1	1	1	0	288	1	1	0	0	1	320
0	0	1	0	0	24	0	1	1	1	1	384	1	1	0	1	0	480
0	0	1	0	1	36	1	0	0	0	0	80	1	1	0	1	1	24
0	0	1	1	0	48	1	0	0	0	1	102	1	1	1	0	0	48
0	0	1	1	1	64	1	0	0	1	0	114	1	1	1	0	1	57
0	1	0	0	0	72	1	0	0	1	1	12	1	1	1	1	0	68
0	1	0	0	1	96	1	0	1	0	0	18	1	1	1	1	1	128
0	1	0	1	0	128	1	0	1	0	1	29						

Note) 'MNTB' means 'Minimum Number of Transmission Bit'

'PR' is accessible to writing operation by setting register address (A1.A0)=(1.0) of the second access.

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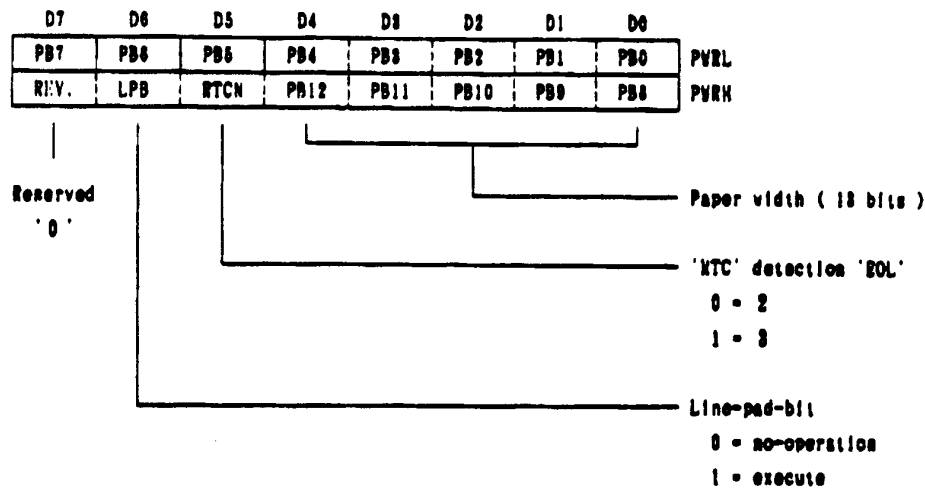
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□ PWRL / PWRH (Paper Width Register of Low/High)



'PWRL/H' is accessible to writing operation by setting register address (A1.A0)=(1.1)
The first access, 'PWRL' is accessed, and the second access, 'PWRH' is accessed.

Paper width (the number of pels composing one-line) is set by following procedure.

Example) Set B4 (8dot/mm)= 2048 bit/line

- ① $2048(D) - 1(D) = 2047(D)$ since 1
- ② $2047(D) = 7FF(H)$ HEX code
- ③ $7FF(H) = 0111\ 1111\ 1111(D)$ Binary code
- ④ $0111\ 1111\ 1111(D) = 0\ 0111\ 1111\ 1111(D)$ 18 bits of Binary code

(PB12.PB11.PB10.....PB1.PB0)=(0.0.1.1.1.1.1.1.1.1.1)

But, if the paper width is set more than 7748 bit/line or less than 88 bit/line, the VCEC*
is not processes the correct data. Then following setting is INHIBIT.

Less than (PB12.PB11.PB10.....PB1.PB0)=(0.0.0.0.0.0.0.1.1.1.1)

More than (PB12.PB11.PB10.....PB1.PB0)=(1.1.1.1.0.0.0.1.1.1.1)

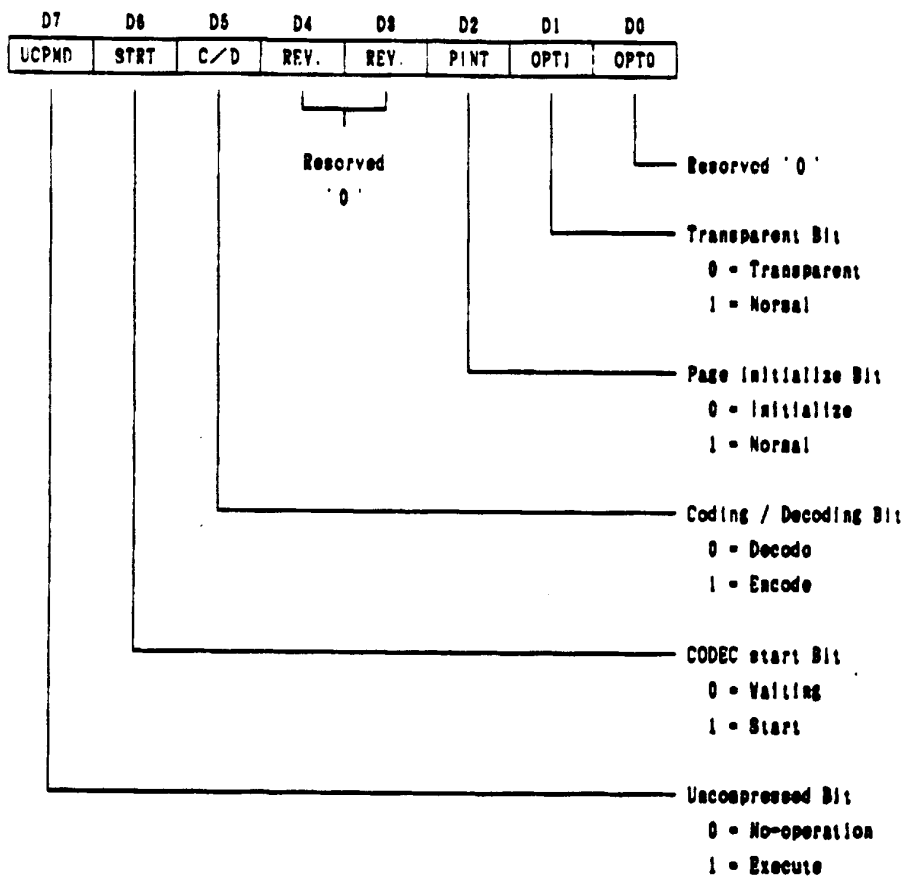
Note) Reserve bit of this register is always set at '0'

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SCNR (System Control Notice Register)



'SCNR' is accessible to reading operation by setting register address (A1.A0)=(0.0).

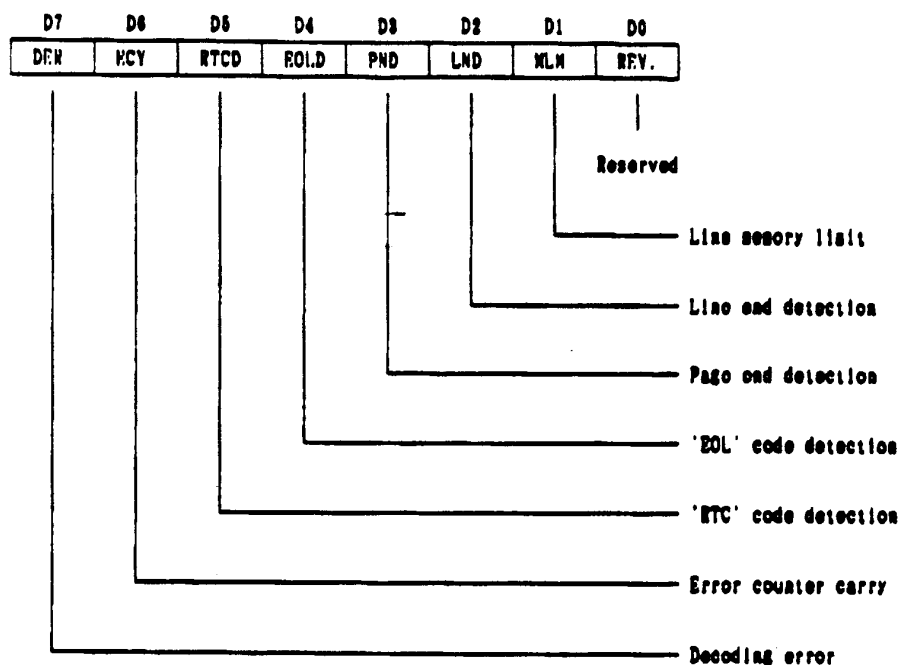
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□ IRR (Interrupt Request Register)



'IRR' is accessible to reading operation by setting register address (A1.A0)=(0.1).

Reading in this register, and the system finds the cause of the interruption. 'IRQ' signal and this register is reset, by reading this register. Meaning of each bit, see following table.

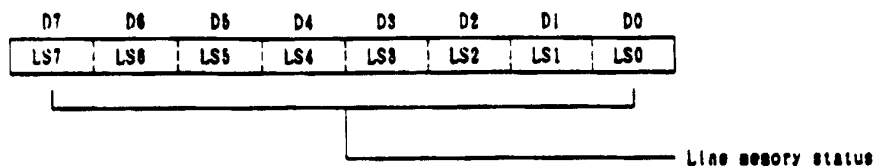
Name	Coding/Decoding	Meaning
NLM	Coding	Line memory is Full
	Decoding	Line memory is empty
LND	Coding	generate 'EOL' code
	Decoding	Outputs the last data of a line
PND	Coding	Outputs the last coded-data of a page
	Decoding	Outputs the last PIX-data of a page
EOLD	Decoding	'EOL' code detection
RTCD	Decoding	'RTC' code detection
ECY	Decoding	Carry of error line counter (8-bit) This bit is active then error line counter is reset.
DER	Decoding	Decoding error detection Error line counter is increment in this time.

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☐ LSR (Line memory Status Register)



'LSR' is accessible to reading operation by setting register address (A1.A0)=(1.0).

This register shows the number of line's data stored in the line memory. If using 64kbyte RAM for line memory, this register is function as follows

Stored line	MLM [IRR(D1)]	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0 line	L	0	0	0	0	0	0	0	0
1 line	L	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
2 5 4 line	L	1	1	1	1	1	1	1	0
2 5 5 line	L	1	1	1	1	1	1	1	1
2 5 6 line	L	1	1	1	1	1	1	1	1
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
3 0 2 line	H	1	1	1	1	1	1	1	1

302 line's data is able to stored in this memory. when this memory stored 302 line's data, the register drives the 'MLN' bit of 'INR' is active, and stops the data input.

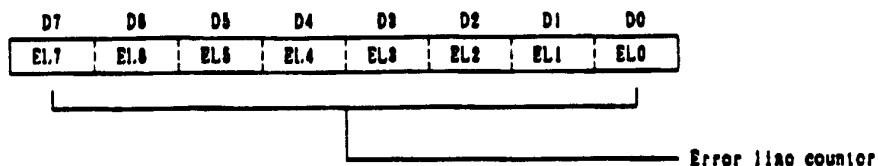
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INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

☐ ELR (Error Line count Register)



'ELR' is accessible to reading operation by setting register address (A1.A0)=(1.1).

This register counts the number of line contains error. This register drives 'IRQ' signal is active. every 256 error line is counted. This register and 'ECV' bit of 'IRR' functions as follows

Error Line	ECV [IRR(D6)]	D7	D6	D5	D4	D3	D2	D1	D0
0 line	L	0	0	0	0	0	0	0	0
1 line	L	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
254 line	L	1	1	1	1	1	1	1	0
255 line	H	1	1	1	1	1	1	1	1
256 line	L	0	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
510 line	L	1	1	1	1	1	1	1	0
511 line	H	1	1	1	1	1	1	1	1
512 line	L	0	0	0	0	0	0	0	0
513 line	L	0	0	0	0	0	0	0	1
:	:	:	:	:	:	:	:	:	:

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INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

Line memory Selection

Memory selection

Connects the Static-RAM as the line memory. The Memory size is decided by maximum number of pels for coding. The RAM size involved in the maximum number of pels is explained following table (next page). It should be selected that more than 8-lines of data is stored in.

If the decoding error is occurred, the VCEC+ is not increment the address of the line memory in this action, previous line's data is output instead of the error line's data. But during this action, data is transmitted continuously. The time for the recovering error line involved in the line memory access time is following table.

Access time paper width	250 ns		500 ns		1000 ns	
	Time	Bit	Time	Bit	Time	Bit
256 bit	0.016	0.15	0.016	0.15	0.016	0.15
512 bit	0.032	0.31	0.032	0.31	0.032	0.31
1024 bit	0.064	0.61	0.064	0.61	0.064	0.61
1728 bit	0.108	1.04	0.108	1.04	0.108	1.04
2048 bit	0.128	1.23	0.128	1.23	0.128	1.23
4096 bit	0.256	2.46	0.256	2.46	0.256	2.46
7743 bit	0.484	4.65	0.484	4.65	0.484	4.65

Note) Time means the time for recovering error line [unit : ns]
 Bit means the total number of bit during the Time is past [unit : bit/sec]
 (Transmission rate is 9600 bps)
 Access time 250 ns equivalent to 16MHz master clock input

$$T = \frac{x}{8} \times y \times 2 + a \quad (\text{ ns })$$

$$D = T \times Z \quad (\text{ bit })$$

T : Time for recovering error line
 x : Total number of bit composing paper width
 y : Memory access time
 a : Dynamic refresh time (not supported)
 D : total number of bit during Time is past
 Z : Data transmission rate

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INTEGRATED CIRCUIT

TECHNICAL DATA

TC35180F

Line memory selection Table

[Unit : Para/Line]

RAM Size Paper Size (Byte)	Maximum storage line size							
	2K	4K	8K	16K	32K	64K	128K	256K
24 - 256	63	127	255	511	1023	2046	2046	2046
257 - 512	31	63	127	255	511	1023	2046	2046
513 - 768	20	41	84	169	340	681	1364	2046
769 - 1024	15	31	63	127	255	511	1023	2046
1025 - 1280	11	24	50	101	203	406	812	1627
1281 - 1536	9	20	41	84	169	340	681	1364
1537 - 1792	8	17	35	72	145	291	584	1169
1793 - 2048	7	15	30	63	127	255	511	1023
2049 - 2304	6	13	27	55	112	226	454	909
2305 - 2560	6	11	24	50	101	203	406	812
2561 - 2816	4	10	22	45	92	185	371	743
2817 - 3072	4	9	19	41	84	169	340	681
3073 - 3328	3	8	16	33	77	156	314	629
3329 - 3584	3	8	17	35	72	145	291	584
3585 - 3840	3	7	16	33	67	135	272	545
3841 - 4096	3	7	15	31	63	127	255	511
4097 - 4352	×	6	14	29	59	119	239	480
4353 - 4608	×	6	13	27	55	112	226	454
4609 - 4864	×	5	12	25	52	106	214	430
4865 - 5120	×	5	11	24	50	101	203	406
5121 - 5376	×	5	11	23	47	96	194	389
5377 - 5632	×	4	10	22	45	92	185	371
5633 - 5888	×	4	10	21	43	86	177	356
5889 - 6144	×	4	9	20	41	84	169	340
6145 - 6400	×	4	9	19	39	80	162	326
6401 - 6656	×	3	8	18	36	77	156	314
6657 - 6912	×	3	8	17	35	74	150	302
6913 - 7168	×	3	8	17	35	72	145	291
7169 - 7424	×	3	7	16	34	69	140	281
7425 - 7680	×	3	7	15	33	67	135	272
7681 - 7743	×	3	7	15	32	65	131	263
RAM Type	S - RAM			D - RAM				

Note) Dynamic ROM is not supported now. Can connect Static-RAM only.

× mark : not for use as the line memory

Recommendable RAM TC5585APL-10/-12/-15 (8k x 8bit)

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INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

Initialization and Termination process

□ Initialization

The MPU should be done following initialization, before VCEC* starts the processing.

Example for Initialization explains after follows :

Conditions

- Paper width A4 (1728 bit/line)
- Interrupt Mask Register no-mask
- Line memory size 2K byte
- Line-pad-bit no operation
- 'RTC' composing 'EOL' 8
- 'RTC' detective 'EOL' 2
- Coding mode Modified Huffman
- Coding or Decoding Encoding

No.	M e a n s	Register	Example for setting	
			D 7 ~ D 0	HEX code
①	Set initializing mode	SCSR	(0.0.1.0.0.0.1.1)	2 3
②	Interrupt Mask Register setting	IMR	(0.0.0.0.0.0.0.0)	0 0
③	RAM size Register setting	RSR	(0.0.0.0.0.0.1.1)	0 3
④	Parameter Register setting	PR	(0.0.0.0.0.0.0.0)	0 0
⑤	Paper width Register of Low setting	PVRL	(1.0.1.1.1.1.1.1)	B F
⑥	Paper width Register of High setting	PVRH	(0.0.0.0.0.1.1.0)	0 6
⑦	Set waiting mode	SCSR	(0.0.1.0.0.1.1.1)	2 7
⑧	CODRC start	SCSR	(0.1.1.0.0.1.1.1)	8 7

□ Termination 1 (Encoding mode Termination)

No.	M e a n s	Register	Example for setting	
			D 7 ~ D 0	HEX code
①	Input last data of a page			
②	Set waiting mode	SCSR	(0.0.1.0.0.1.1.1)	2 7
③	Detection of 'PND' bit of 'IRR'			
④	Set initializing mode	SCSR	(0.0.1.0.0.0.1.1)	2 3

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INTEGRATED CIRCUIT

TECHNICAL DATA

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□ Termination II (Decoding mode Termination).

No.	M e s s	Register	Example for setting	
			D 7 ~ D 0	HEX code
①	Detects 'RTC' code			
②	Detects the 'PND' bit of 'IRR'			
③	Set waiting mode	SCSR	(0.0.0.0.0.1.1.1)	07
④	Set Initializing mode	SCSR	(0.0.0.0.0.0.1.1)	03

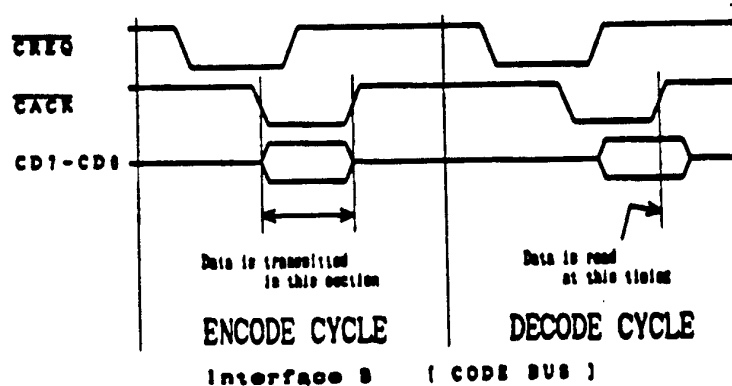
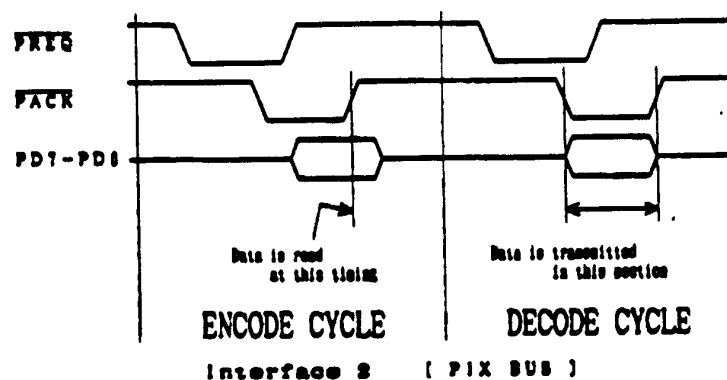
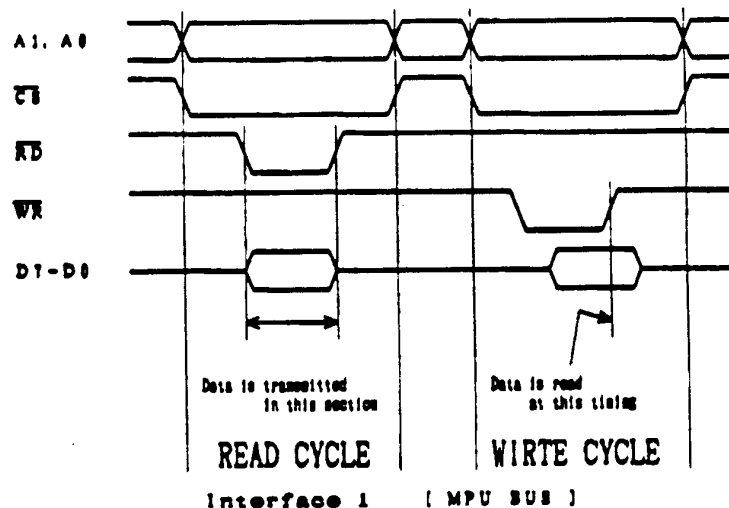
If any changes are needed for initial setting before CEDEC re-start, initialization is should be done at the beginning.

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35180F

BUS INTERFACE

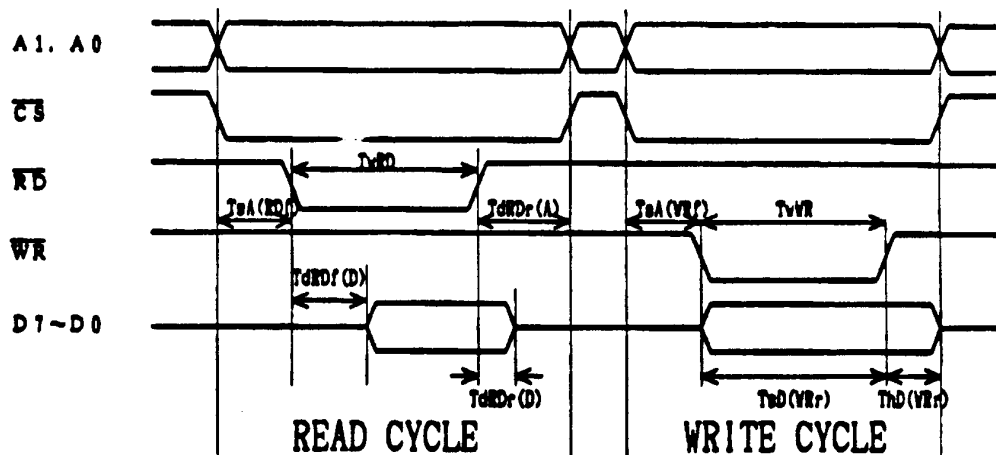


TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TC35180F



MPU Bus AC Timing

UNIT : ns

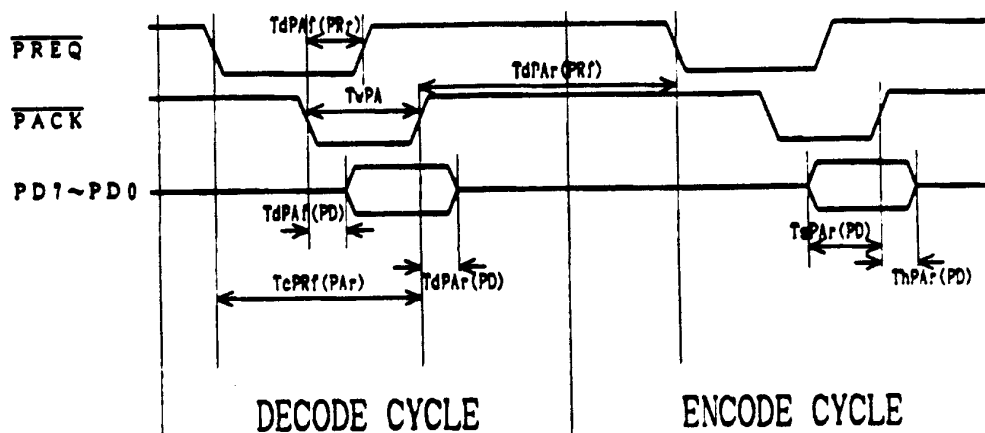
Item	Notes	Minimum	Typical	Maximum
$T_{sA}(RD)$	Address Set-up Time till $\overline{RD} = 'L'$	70		
$T_{dRD}(D)$	$\overline{RD} = 'L'$ to Data Valid		75	
$T_{dRD}(A)$	Address Recovery Time from $\overline{RD} = 'H'$	30		
$T_{dRD}(D)$	$\overline{RD} = 'H'$ to Output Data High-Z	0		
T_{wRD}	$\overline{RD}$ Signal Input Pulse Width	150		
$T_{sA}(WR)$	Address Set-up Time to $\overline{WE} = 'L'$	70		
$T_{sD}(WR)$	Data set-up Time for $\overline{WE} = 'H'$	140		
$T_{hD}(WR)$	Data Hold Time for $\overline{WE} = 'H'$	30		
T_{wWR}	$\overline{WE}$ Signal Input Pulse Width	150		

TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F



PIX Bus AC Timing

UNIT : nS

Item	Meaning	Minimum	Typical	Maximum
TcPRf(PAr)	'PREQ'='L' to 'PACK'='H'	2T*		
TdPAf(PRF)	'PACK'='L' to 'PREQ'='H'			60
TdPAf(PD)	'PACK'='L' to Output Data Valid			80
TdPAr(PD)	'PACK'='H' to Output Data='High-Z'	0		
TdPAr(PRF)	'PACK'='H' to 'PREQ'='L'	20		
TSPAr(PD)	Data Set-up Time for 'PACK'='H'	60		
ThPAr(PD)	Data Hold Time for 'PACK'='H'	20		
TwPA	'PACK' Input Pulse Width	120		

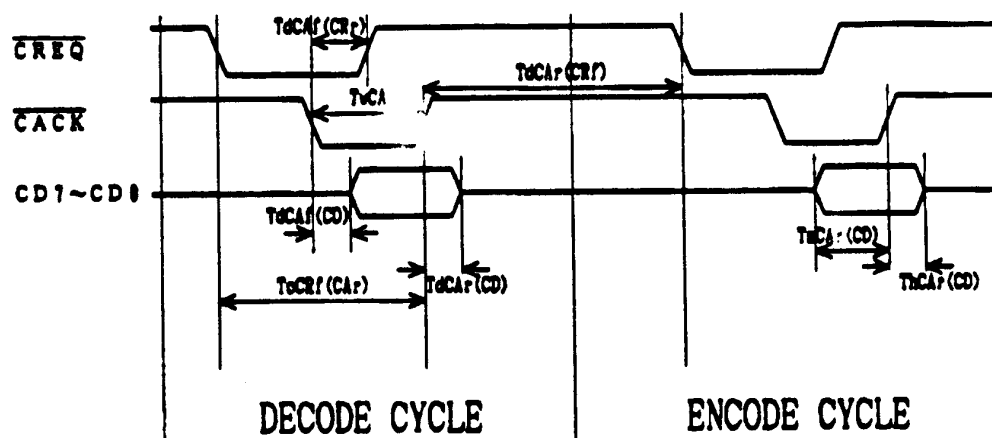
(注) * : 'T' denotes one cycle time of VCEC input clock.

TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TC35180F



Code Bus AC Timing

UNIT : ns

Item	Meaning	Minimum	Typical	Maximum
$T_{dCRf}(CAr)$	'CREQ' = 'L' to 'CACK' = 'H'	5T ¹		
$T_{dCAf}(CRf)$	'CACK' = 'L' to 'CREQ' = 'H'			80
$T_{dCAf}(CD)$	'CACK' = 'L' to Output Data Valid			80
$T_{dCAr}(CD)$	'CACK' = 'H' to Output Data = 'High-Z'	0		
$T_{dCAr}(CRf)$	'CACK' = 'H' to 'CREQ' = 'L'	20		
$T_{sCAr}(CD)$	Data Set-up Time for 'CACK' = 'H'	80		
$T_{hCAr}(CD)$	Data Hold Time for 'CACK' = 'H'	20		
T_{wCA}	'CACK' Input Pulse Width	120		

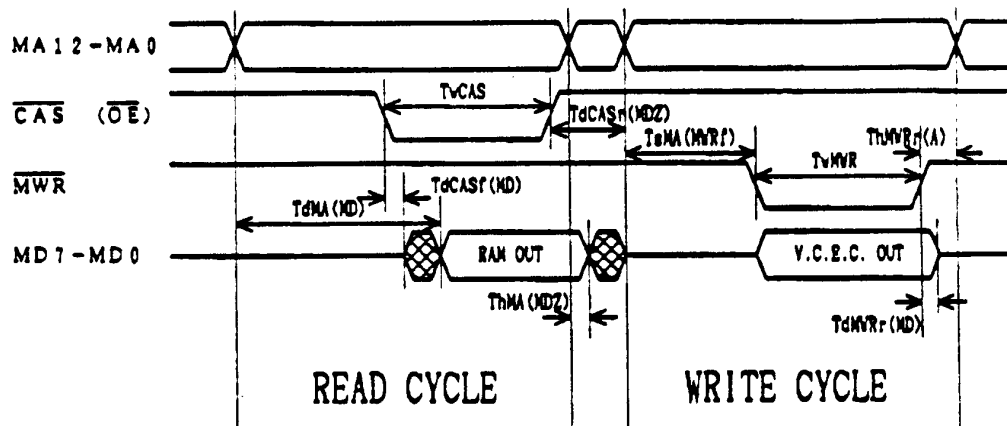
1) * : 'T' denotes one cycle time of VCHC input clock.

TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F



Line Memory AC Timing

UNIT : ns

Item	Meaning	Minimum	Typical	Maximum
$T_{dMA} (MD)$	Memory Address Valid to Data Valid			$3T-30^*$
$T_{dCAS} (MD)$	'CAS' = 'L' to Data = 'Low-Z'			T^*
$T_{hMA} (MDZ)$	Data Hold Time after Address Change	0		
$T_{dCASr} (MDZ)$	'CAS' = 'H' to Data = 'High-Z'	80		T^*
T_{wCAS}	'CAS' Signal Input Pulse Width		$2T^*$	
$T_{dMA} (MWR)$	Address Set-up Time Prior to 'MWR' = 'L'	10		
$T_{dMWR} (MD)$	'MWR' = 'H' to Data = 'High-Z'	T^*		
$T_{hMWR} (A)$	Address Recovery Time for 'MWR' = 'H'	T^*		
T_{wMWR}	'MWR' Signal Input Pulse Width		$2T^*$	

(注) * : 'T' denotes one cycle time of VCEC input clock.

TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TC36190F

ELECTRICAL CHARACTERISTICS

Supply Voltage : 4.75 ~ 5.25 V Operating Temperature : 0 ~ 70 °C

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V _{IH}	V _{DD} = 5.25V	2.4			V
Input Low Voltage	V _{IL}	V _{DD} = 4.75V			0.8	V
Input Current (High)	I _{IH}	V _{IH} = 5.25V			±10	μA
Input Current (Low)	I _{IL}	V _{IL} = 5.25V			±10	μA
High-Level Output Voltage	V _{OH1}	V _{DD} = 4.75V / I _{OH} = -1.5mA				V
	V _{OH2}	V _{DD} = 4.75V / I _{OH} = -1.0mA	4.0			
Low-Level Output Voltage	V _{OL1}	V _{DD} = 4.75V / I _{OL} = 2.0mA				V
	V _{OL2}	V _{DD} = 4.75V / I _{OL} = 2.0mA			0.4	
Output High Current	I _{OH1}	V _{DD} = 4.75V / V _{OH} = 4.85V	-1.5			mA
	I _{OH2}	V _{DD} = 4.75V / V _{OH} = 4.85V	-1.0			
Output Low Current	I _{OL1}	V _{DD} = 4.75V / V _{OL} = 0.40V	2.0			mA
	I _{OL2}	V _{DD} = 4.75V / V _{OL} = 0.40V	2.0			
Standby Current	I _{QD}	V _{DD} = 5.25V			1	mA
Operating Supply Current	I _{DD}	V _{DD} = 5.25V / f _{cp} = 8MHz		50	100	mA
		V _{DD} = 5.25V / f _{cp} = 16MHz		70	120	
		V _{DD} = 5.25V / f _{cp} = 24MHz		100	160	
		V _{DD} = 5.25V / f _{cp} = 32MHz		150	200	
Maximum Clock Frequency	f _{cp}	Duty 40-60 % / Dynamic RAM	8		8/16/	MHz
		Duty 40-60 % / Static RAM			24/32	

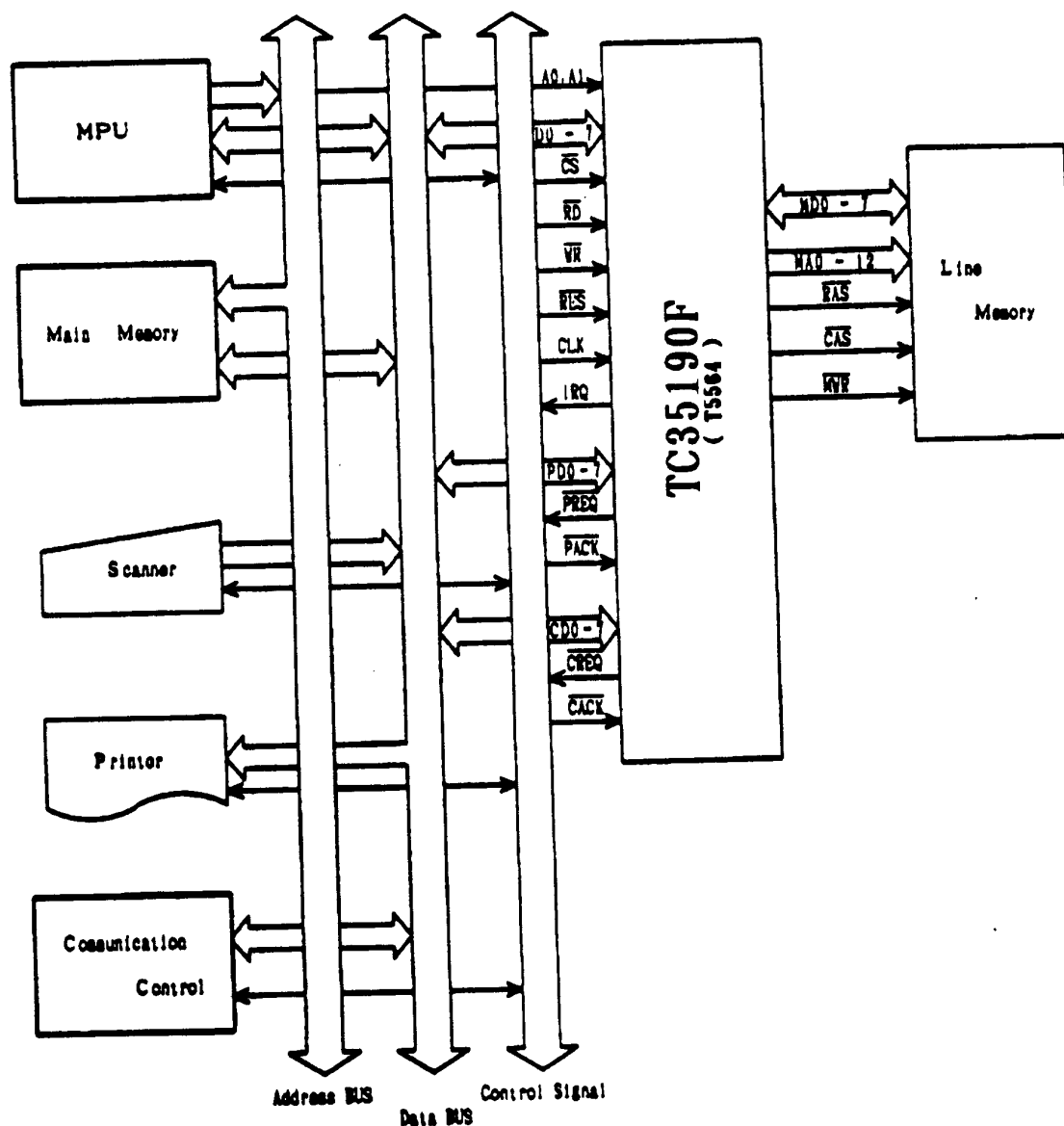
NOTE) V_{OH1}, V_{OL1}, I_{OH1}, I_{OL1} : D7~0, PD7~0, CD7~0, MD7~0 TERMINALS
V_{OH2}, V_{OL2}, I_{OH2}, I_{OL2} : OTHERS

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

Example of Application



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BUS Combined Type (For Small-Size Facsimile)

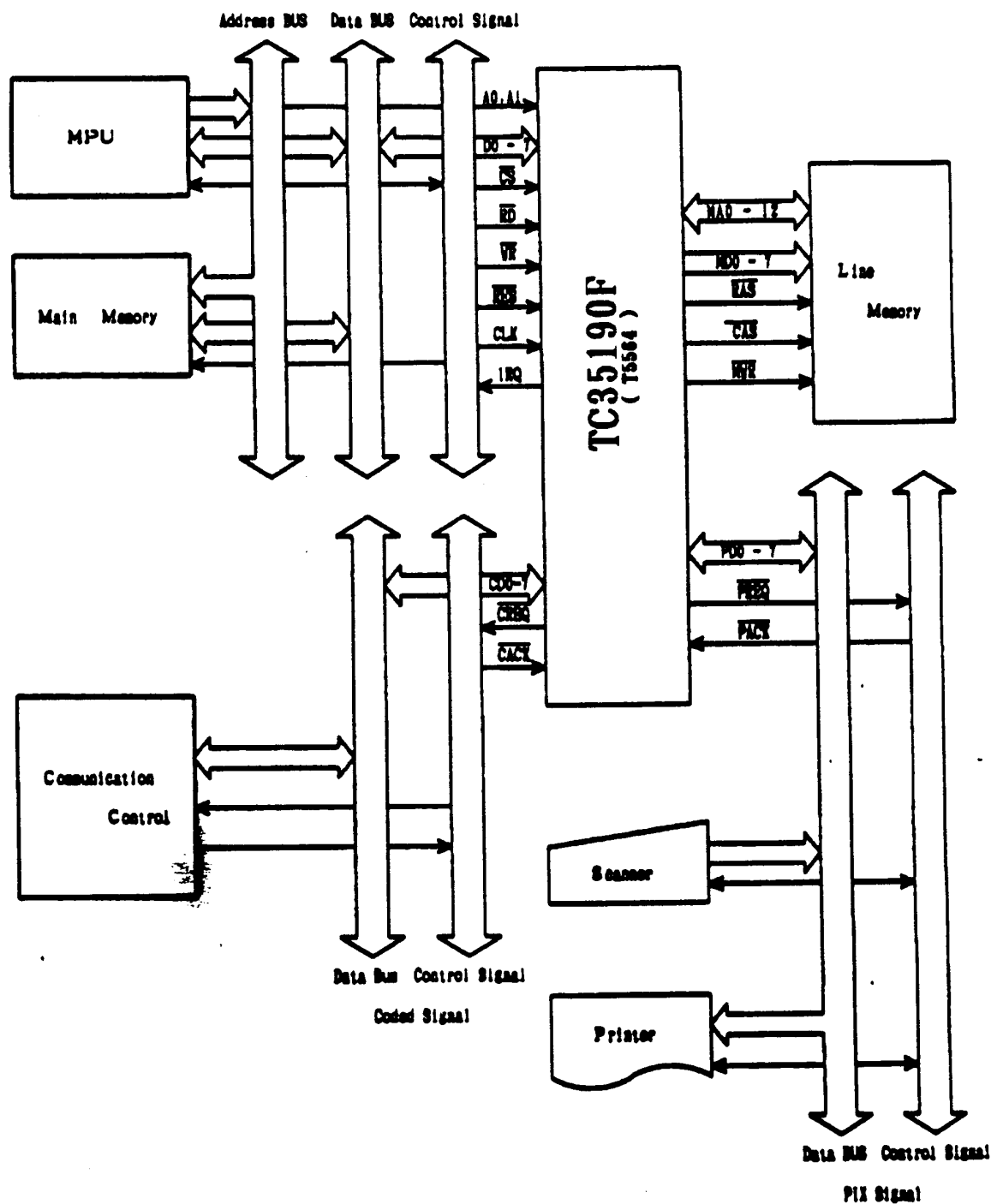
30

TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F



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BUS Separate Type (For High-Speed Facsimile)

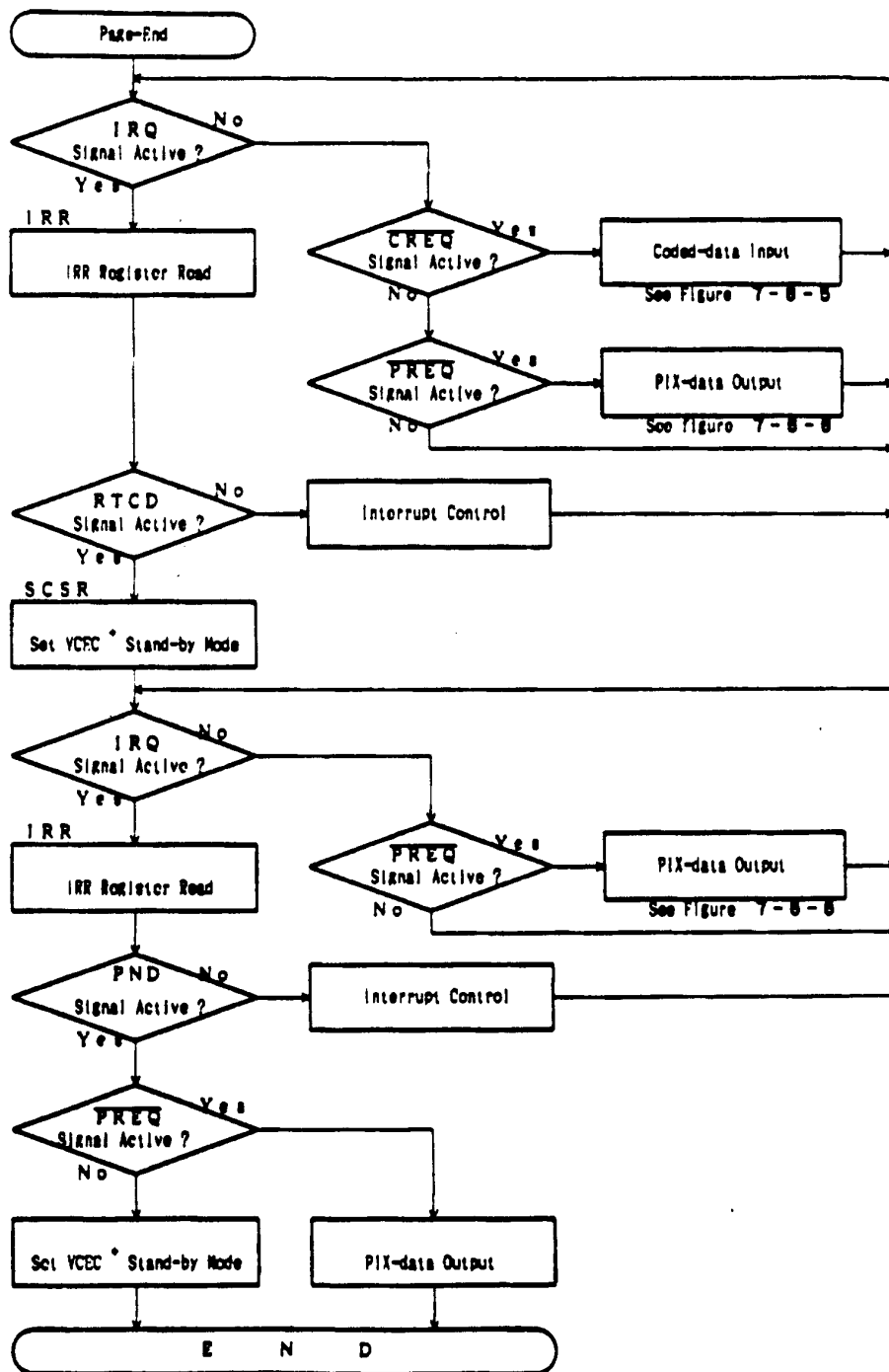
TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

7. 8. 7 Page-End [Decoding]



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FIG 7-8-7 Page-End FLOW [Decoding]

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

7. 6. 5 Coded-data Input [Decoding]

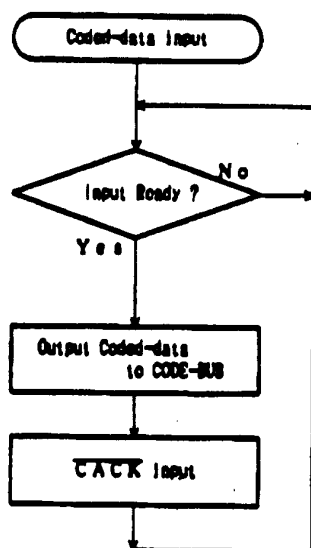


Figure 7-6-5 Coded-data Input FLOW

7. 6. 6 PIX-data output [Decoding]

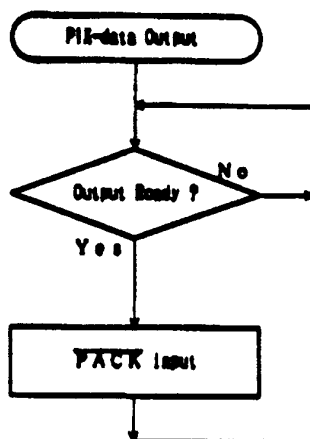


Figure 7-6-6 PIX-data output FLOW

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

7. 6. 4 Interrupt Item Reading [Decoding]

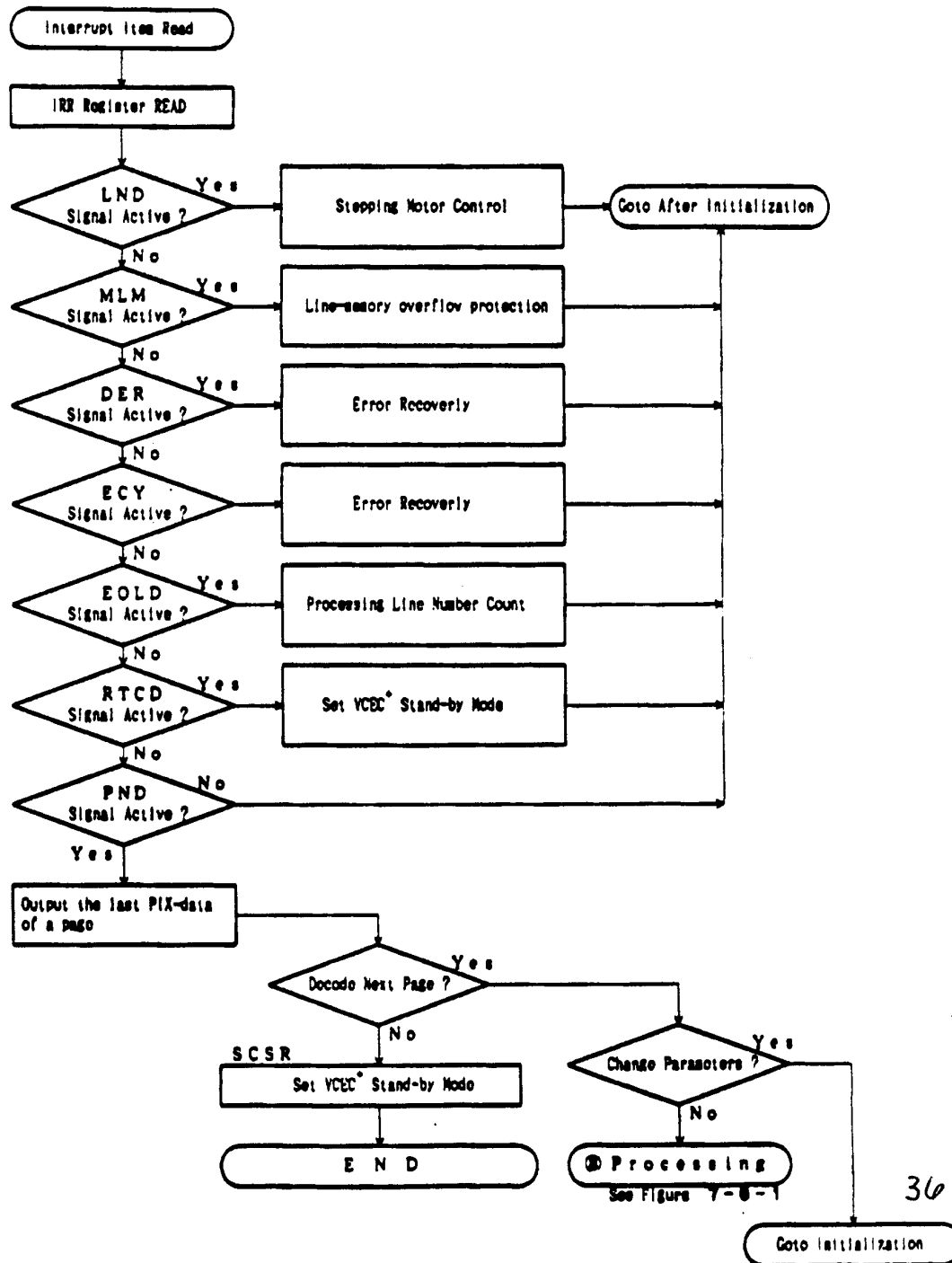


図7-6-4 Interrupt Item Read POW

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35100F

7. 6. 3 After Initialization (II) [Decoding]

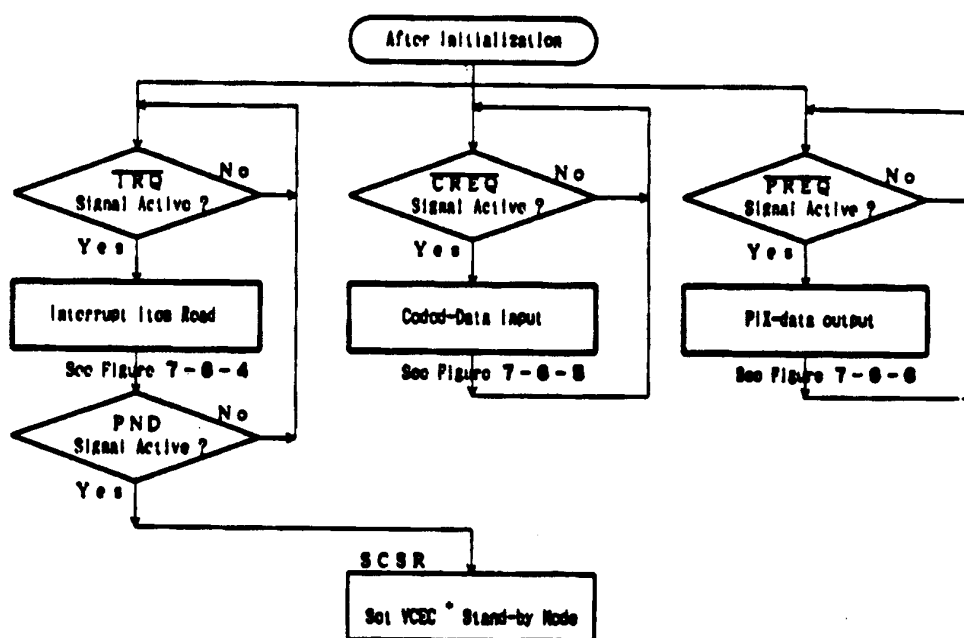


Figure 7-6-3 BUS Separate Type (For High Speed Facsimile) Decoding FLOW

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35180F

7. 6. 2 After Initialization (1) [Decoding]

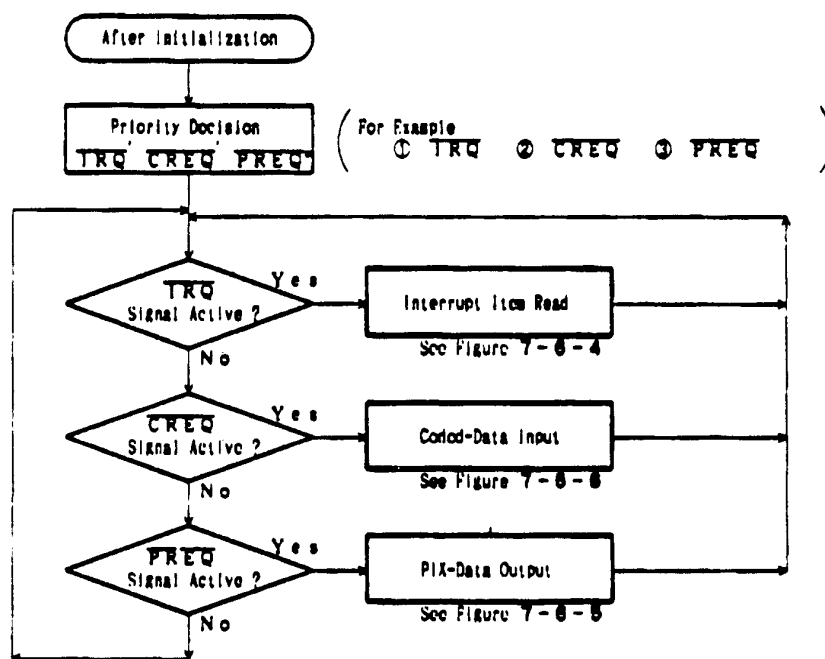


Figure 7-6-2 BUS Combined Type (For Small Size Facsimile) Decoding FLOW

TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

7. 8. 1 Initialization

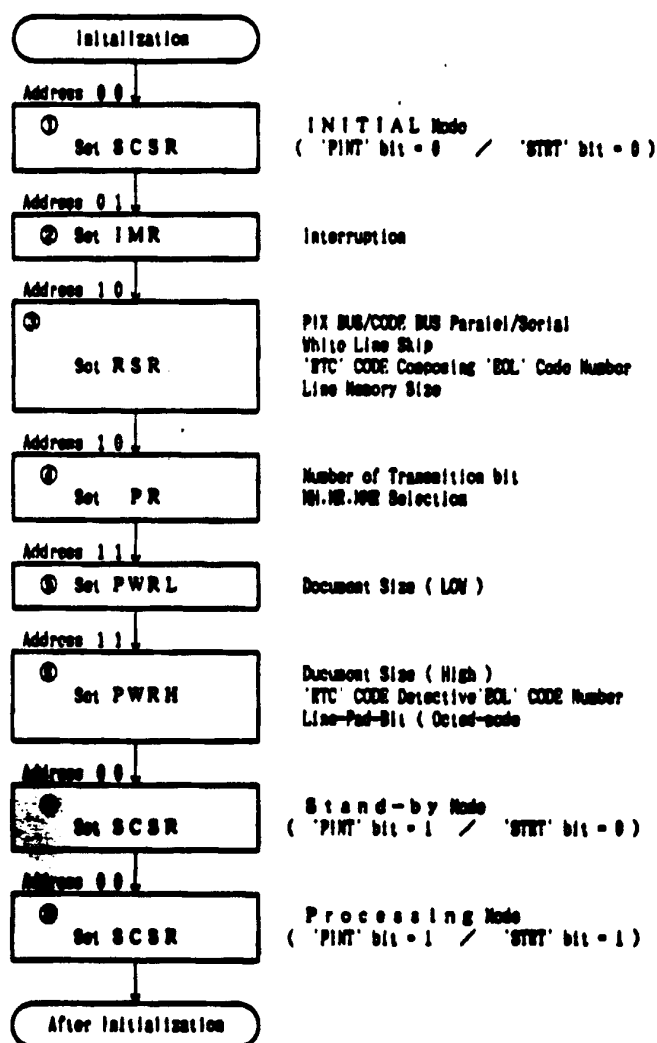


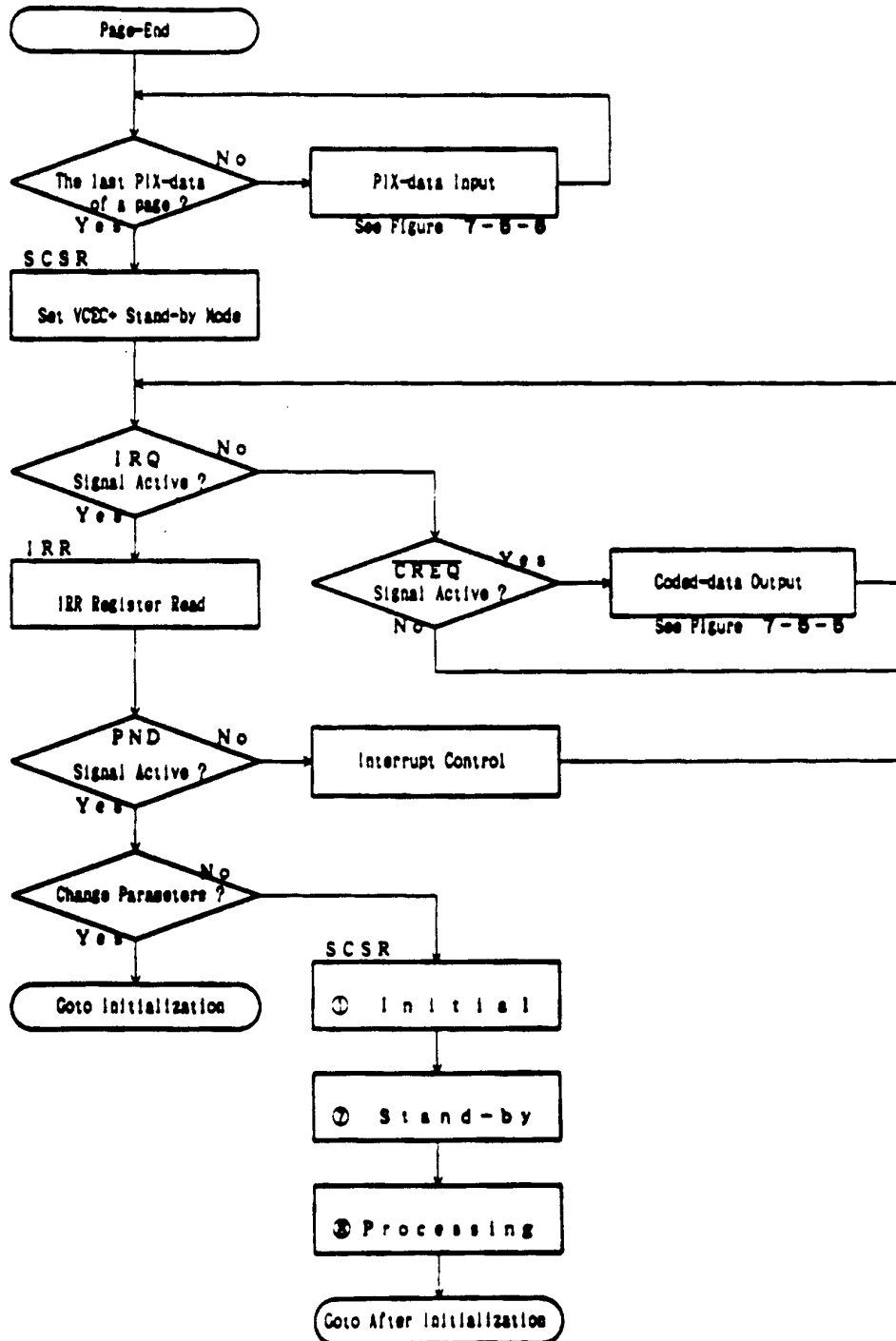
Figure 7-8-1 Initialization FLOW

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

7. 5. 8 Page-End (Re-Start) [Encoding]



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Figure 7-5-8 Page-End (Re-Start) FLOW

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35180F

7. 5. 7 Page-End [Encoding]

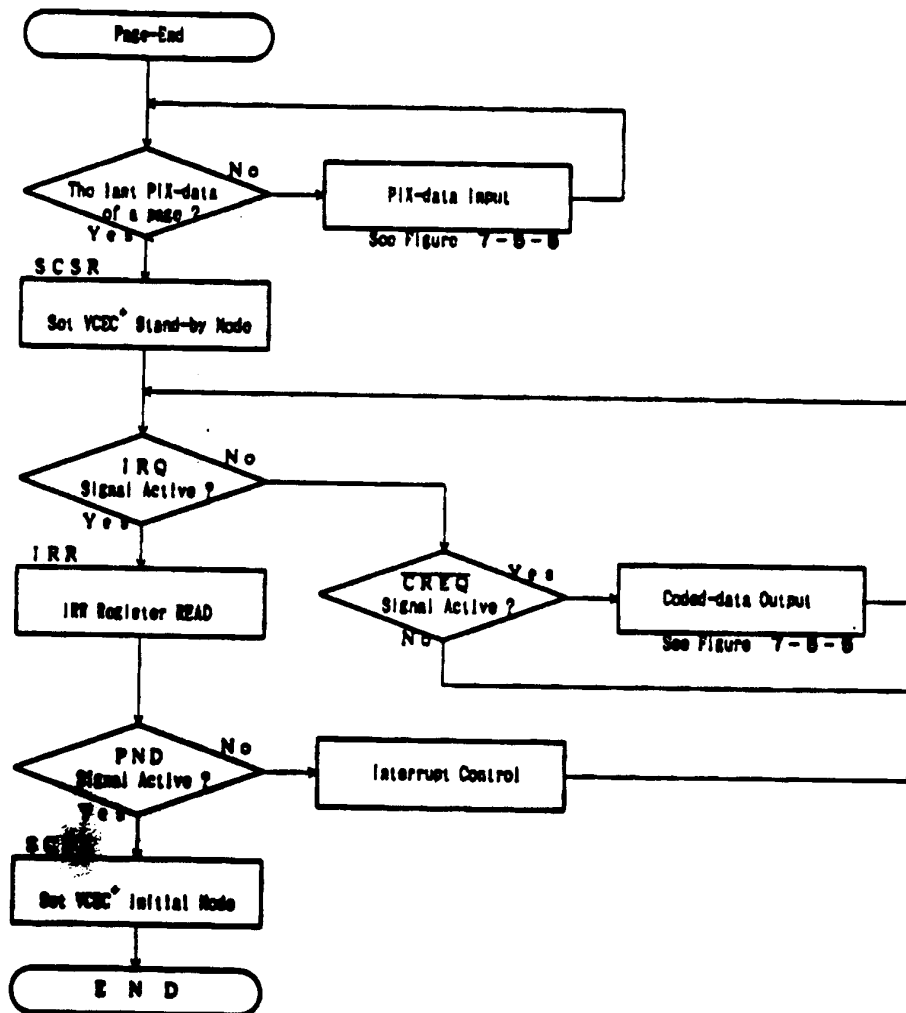


Figure 7-5-7 Page-End FLOW [Encoding]

7. 5. 5 Coded-data output [Encoding]

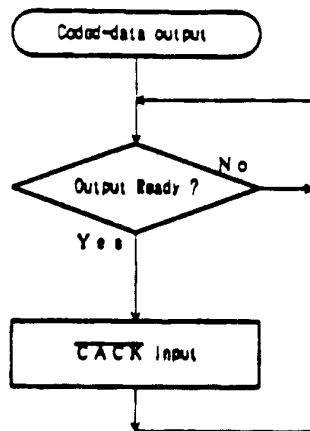


Figure 7-5-5 Coded-data output FLOW

7. 5. 6 PIX-data Input [Encoding]

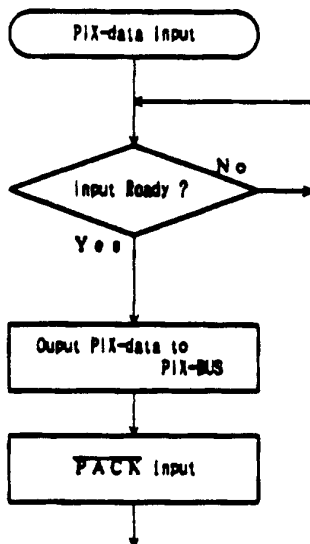


Figure 7-5-6 PIX-data Input FLOW

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35180F

7. 5. 4 Interrupt Item Reading [Encoding]

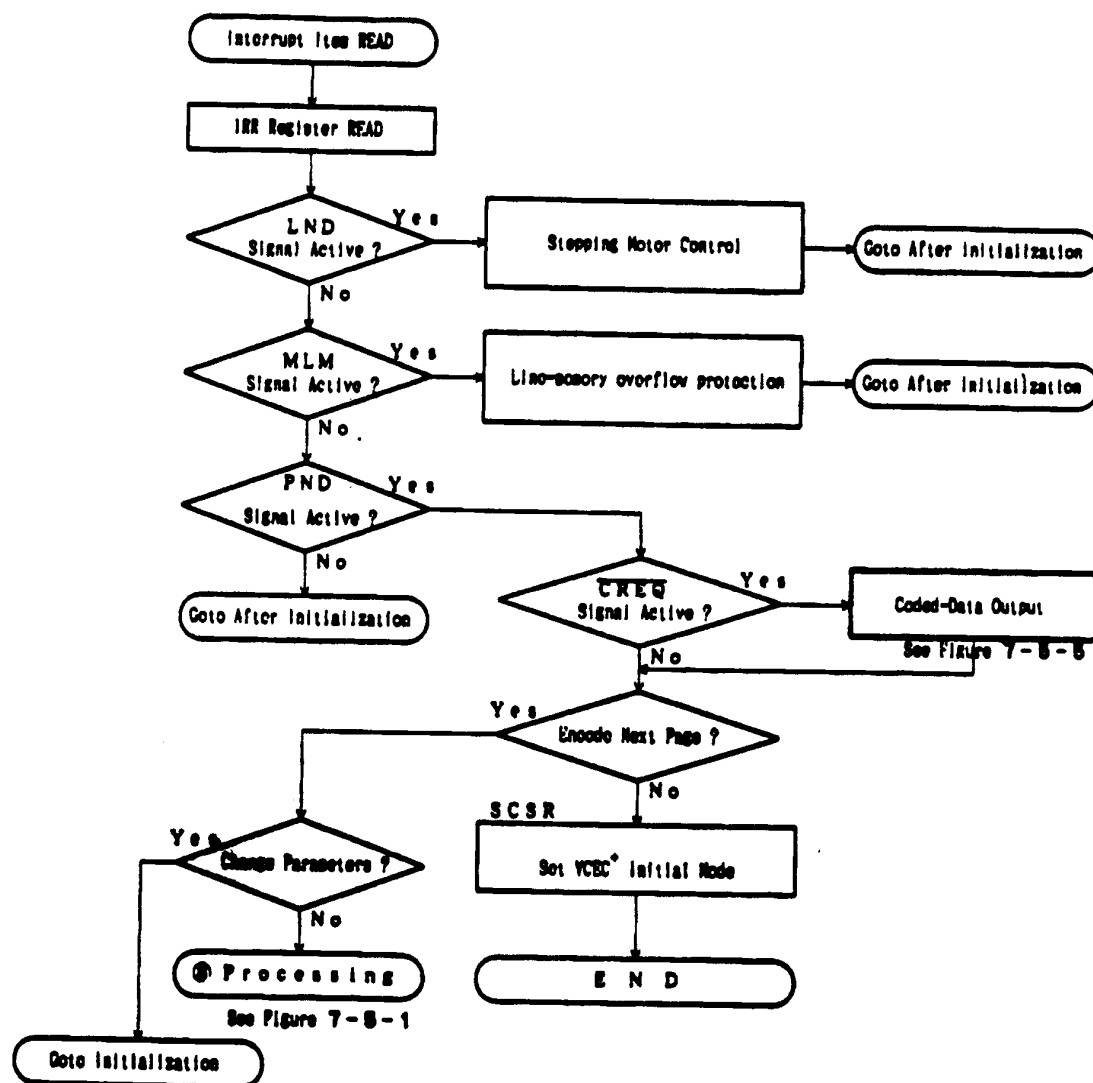


Figure 7-5-4 Interrupt Item Read FLOW

7. 5. 3 After Initialization (2) [Encoding]

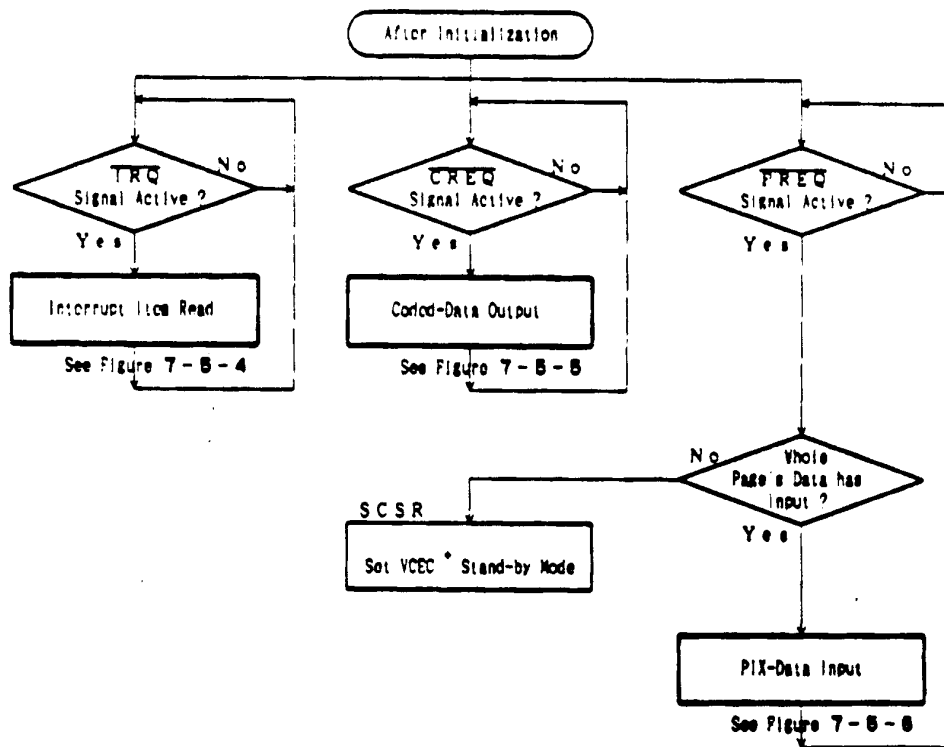


Figure 7-5-3 BUS Separate Type (For High Speed Facsimile) Encoding FLOW

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

7. 5. 2 After Initialization (1) [Encoding]

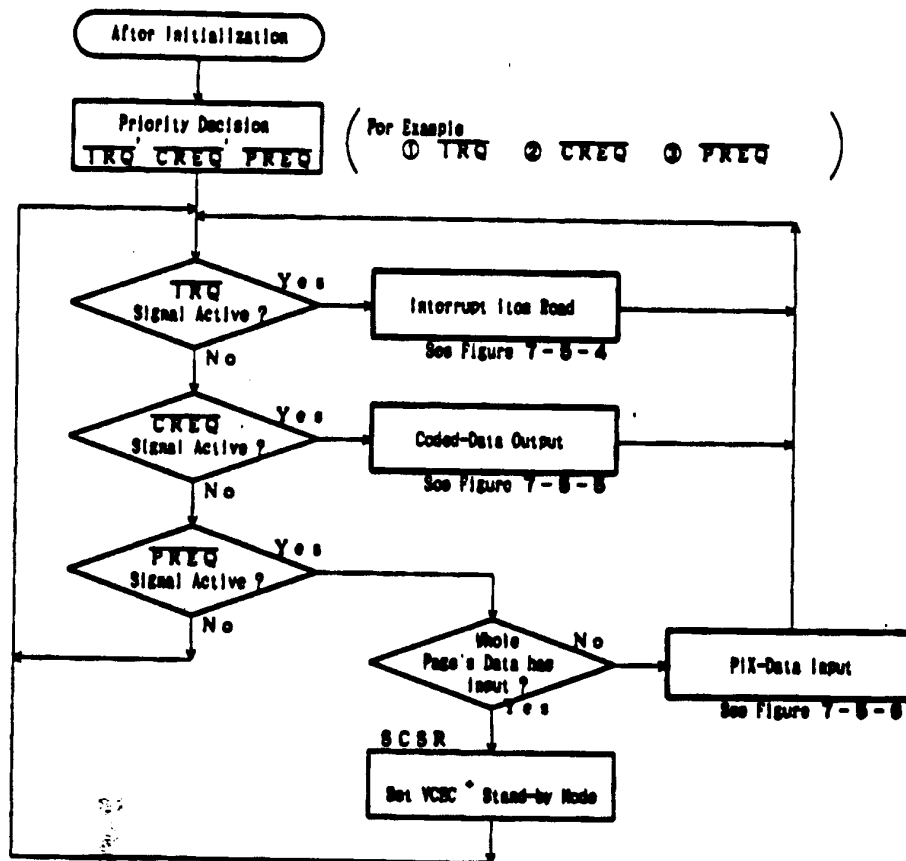


Figure 7-5-2 BUS Combined Type (For Small Size Pacelatte) Encoding FLOW

7. 5. 1 Initialization

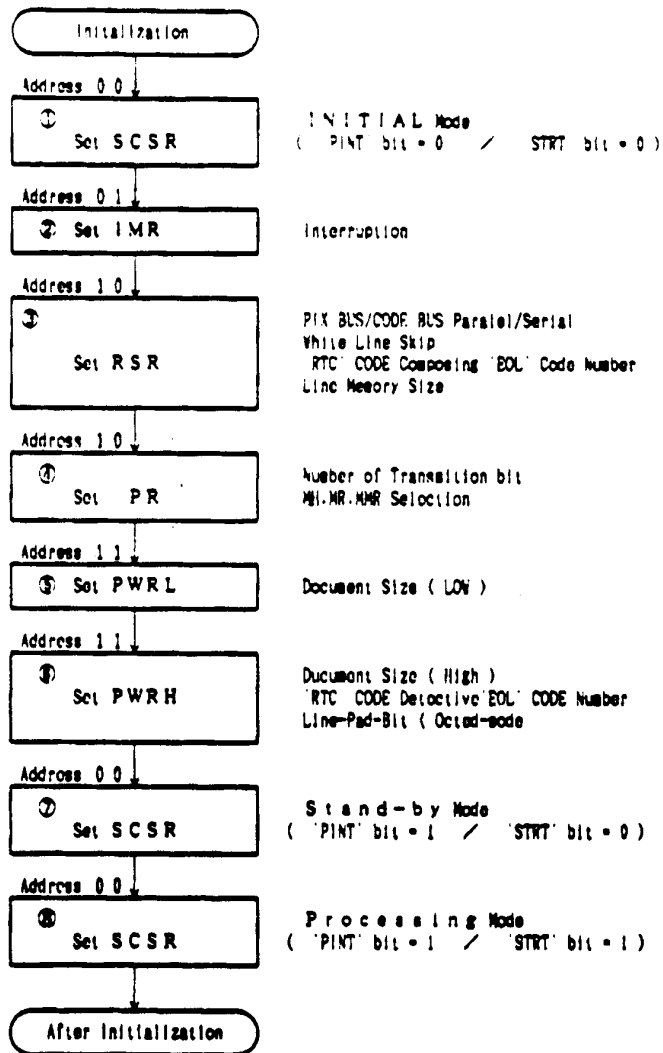


Figure 7-5-1 Initialization FLOW

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35190F

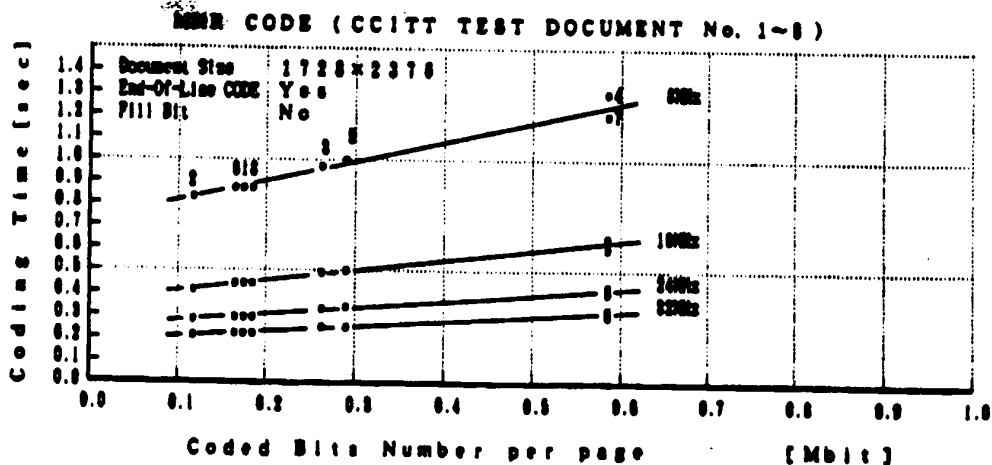
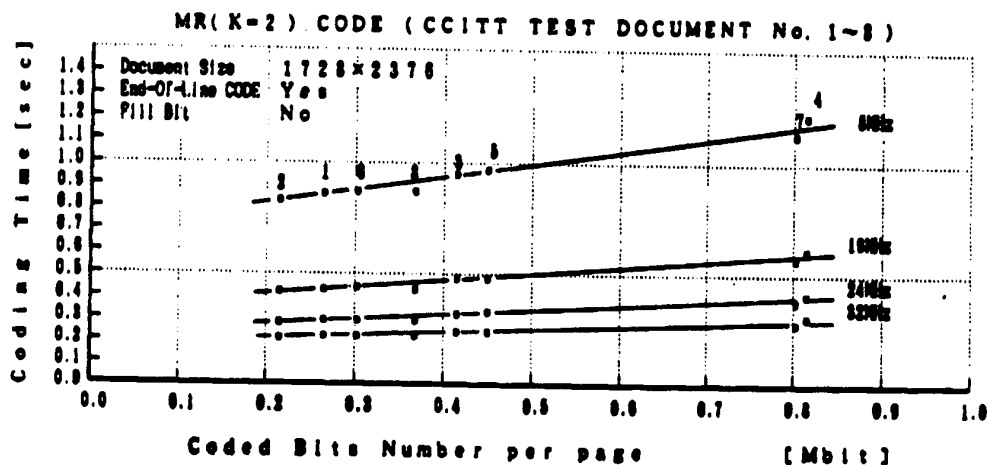
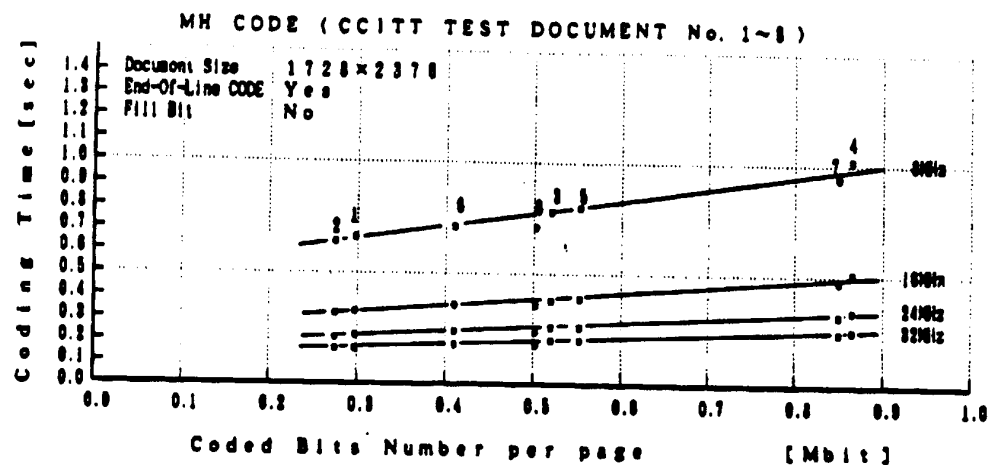


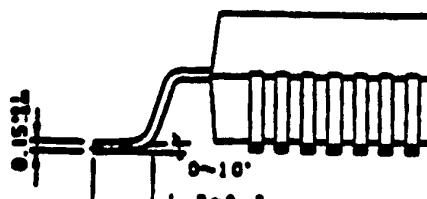
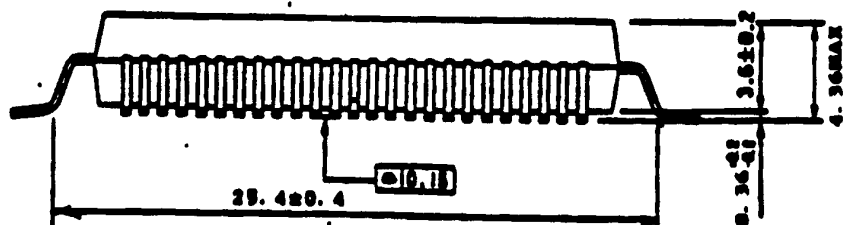
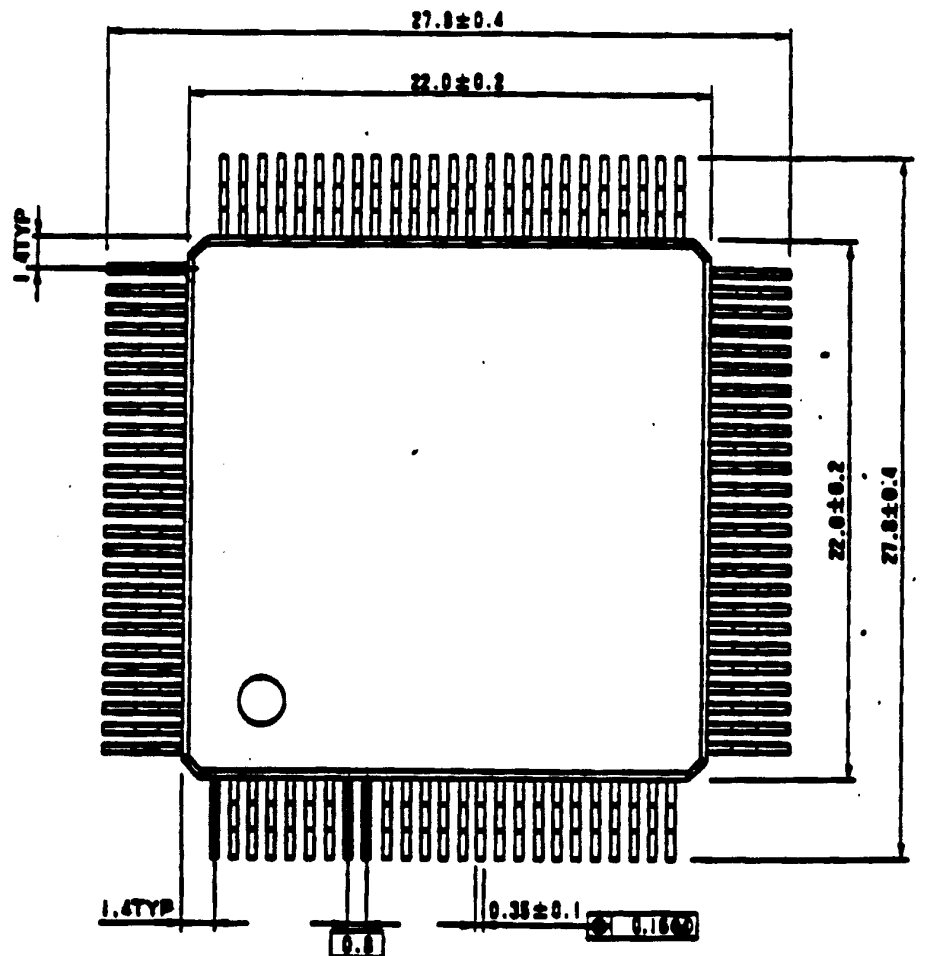
Figure 1-3-1 Encoding Time

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TC35180F

100 Pin Plastic Flat Package UNIT (mm)



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