AlliedSignal
AEROSPACE
Microelectronics and Technology Center

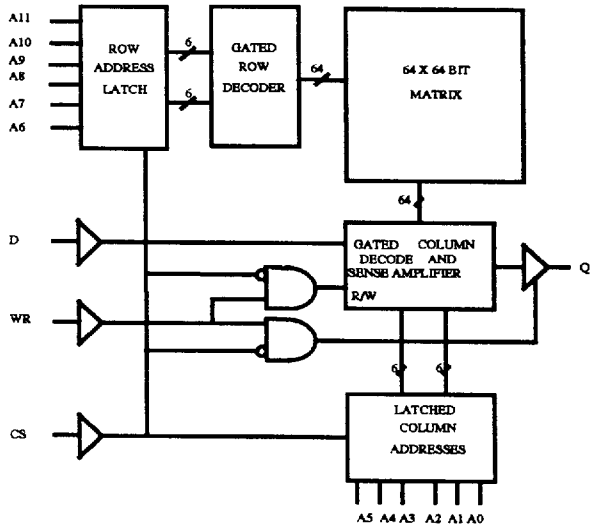
SRAM4

Radiation Hardened 4K x 1 CMOS/ SOI Static Ram

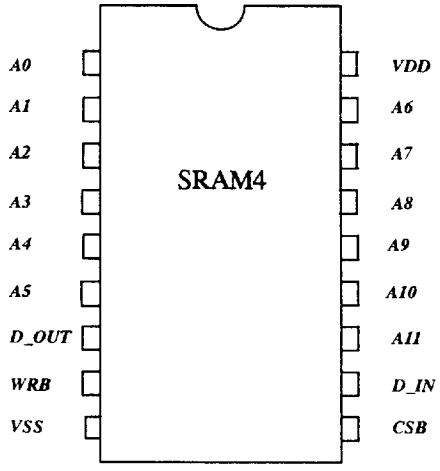
Features

- 1.2um Radiation Hardened SOI CMOS
  - Total Dose > 100k RAD (Si)
  - Transient 3 x 10^{10} RAD (Si)/s
  - Survivability > 1 x 10^{12} RAD (Si)/s
- Latch-Up Free
- Low Voltage Backup Mode
- Low Standby Current
- Fully Static Design
- Six Transistor Bit Cell
- TTL on all Inputs, CMOS Outputs
- 5 Volt Supply
- Standard JEDEC DIP Pinout
- Full Mil Temp (-55 to 125°C)

Functional Diagram



18 Pin Dip



Description

The AlliedSignal SRAM4 is a Radiation Hardened industry standard 4096 x 1 bit static random access memory. It is fabricated using AlliedSignal's proprietary 1.2um CMOS/SOI process which exhibits a high tolerance to radiation and temperature. The RAM operates as specified over full military temperature and requires a single 5 V(+/- 10%) supply and retains data down to 2.0 volts.

TRUTH TABLE

CSB	WRB	MODE	OUTPUT
H	X	NOT SELECTED	HIGH Z
L	L	WRITE	INPUT
L	H	READ	DATA OUT

CAUTION: *These devices are sensitive to electrostatic discharge. Users should follow I.C. handline procedures.*

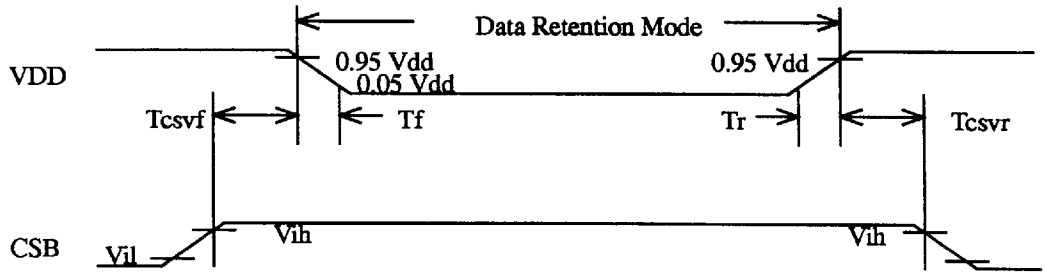
DC ELECTRICAL CHARACTERISTICS						
Test	Symbol	$-55^{\circ}C \le T_C \le +125^{\circ}C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Input Voltage Low	VIL		1,2,3	VSS - 0..7	0.8	V
Input Voltage High	VIH		1,2,3	VDD/2	VDD + 0.7	V
Output Voltage Low	VOL	Vdd = max, Iol = 0.0 mA	1,2,3		VSS + 0.1	V
Output Current Low	IOL	Vdd=min, Vol=0.4	1 2,3		3.5 2.5	ma
Output Voltage High	VOH	Vdd = min, Iol = 0.0 mA	1,2,3	V_{DD} - 0.1		V
Output Current High	IOH	Vdd=min, Voh=Vdd-0.4	1 2,3		-2.5 -2.0	
Input Leakage Current	IL	Vdd = max, Vin = Hi	1 2,3		+/- 2 +/- 10	ma
High Z State Output	IIZ	Vdd = max, Vin = GND	1 2,3		+/- 5 +/- 10	ma
Quiescent Current	IDD	CSB=HI, WRB=HI	1 2,3		0.1 1.0	ma
Operating Current	IOPRO	CSB=HI, WRB=HI	1 2,3		0.15 1.0	ma
Operating Current	IOPR	CSB=HI, WRB=HI	1,2,3		5.0	ma
Input Capacitance	CI	Guaranteed but not tested	4		5	pf
Input Capacitance	CO	Guaranteed but not tested	4		5	pf

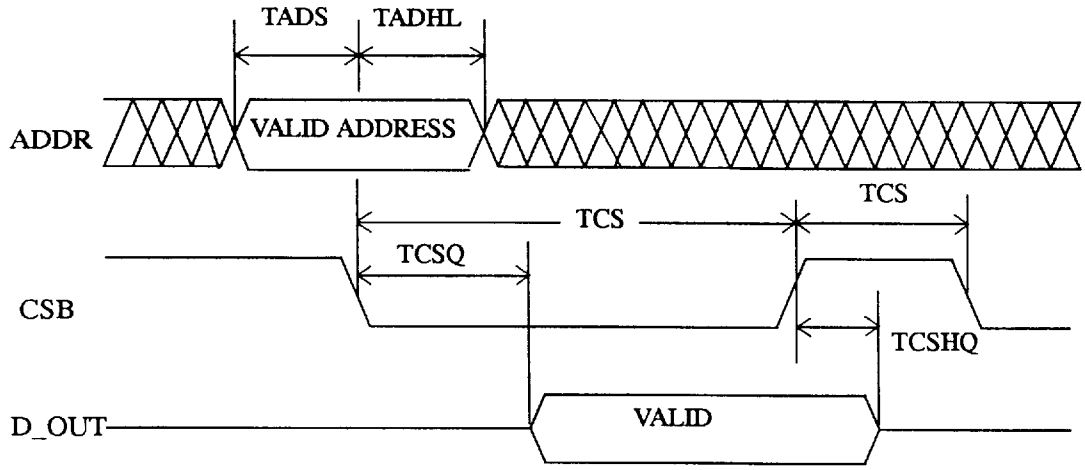
Notes: Notes: _/1 Measured using a 1MHz cycle rate with the outputs loaded with 50pf.

AC ELECTRICAL CHARACTERISTICS						
Test	Symbol	$-55^{\circ}C \le T_C \le +125^{\circ}C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Read Access	TCSQV	Figure 1	9		70	ns
			10,11		80	
CS High to Q Hi Z	TCSHQZ	Figure 1	9		20	ns
			10,11		30	
CS High	TCSH	Figure 1	9	30		ns
			10,11	40		
Address Setup	TADSU	Figure 1,2	9	10		ns
			10,11	15		
CS Low	TCSL	Figure 2	9	85		ns
			10,11	95		
Address Hold	TADHLD	Figure 1,2	9	10		ns
			10,11	15		
Write Low to CS High	TWRLCSH	Figure 2	9	60		ns
			10,11	70		
Write Low	TWRM	Figure 2	9	60		ns
			10,11	70		
Data Setup	TDSU	Figure 2	9	50		ns
			10,11	60		
Data Hold From Write High	TDHLD	Figure 2	9	10		ns
			10,11	15		

CHARACTERISTICS (DATA RETENTION)

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{DD} \leq 5.5\ V$ unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Minimum data Retention Voltage	VDR		9		2.0	V
			10,11		2.5	
Data retention Quiescent Current	$I_{DD}DR$		9		40	ua
			10,11		70	
CSB to VDD Rise and Fall Time	T_R,Tf TCSVF, TCSVR	$-55°C < T_A < +125°C$	9,10,11		1	us

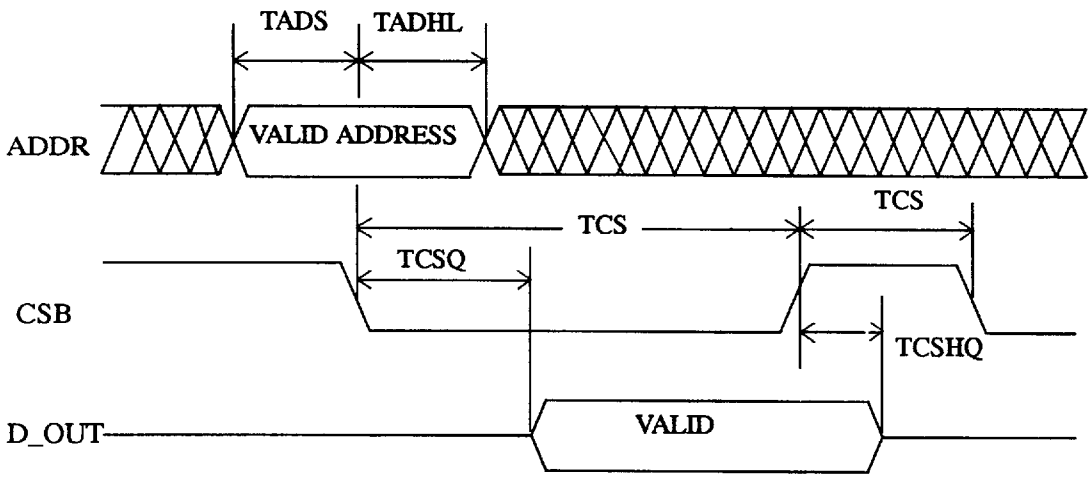




READ CYCLE

FIGURE 1

NOTE: ALL "AC" INPUT PARAMETERS MEASURED WITH RESPECT TO VDD/2.



READ CYCLE

FIGURE 2

NOTE: ALL "AC" INPUT PARAMETERS MEASURED WITH RESPECT TO VDD/2.